Flash Memory Summit

HeatWatch

Improving 3D NAND Flash Memory Device Reliability by Exploiting Self-Recovery and Temperature Awareness

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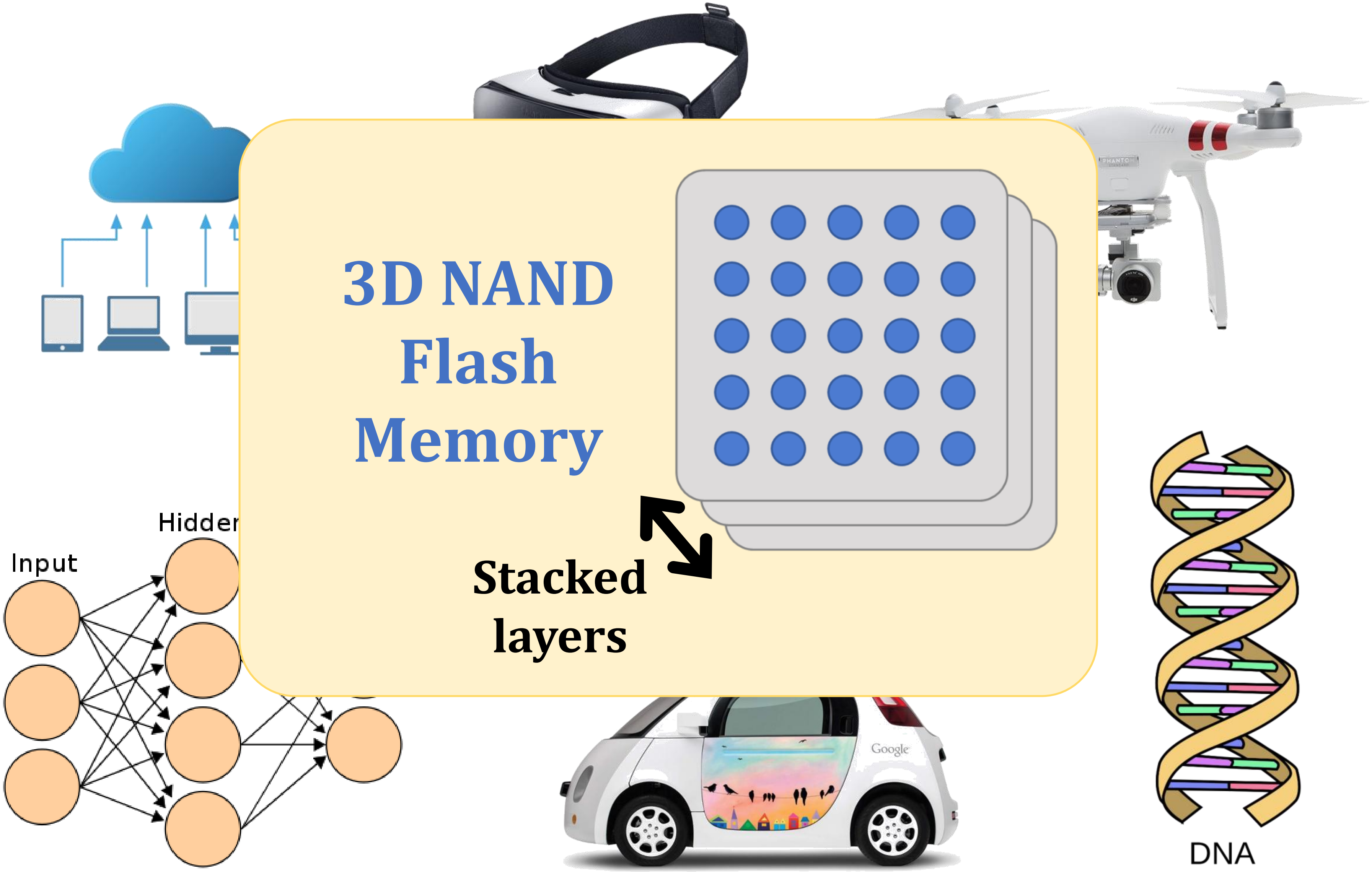
SAFARI SEAGATE

Storage Technology Drivers - 2018



3D NAND Flash Memory

Stacked layers

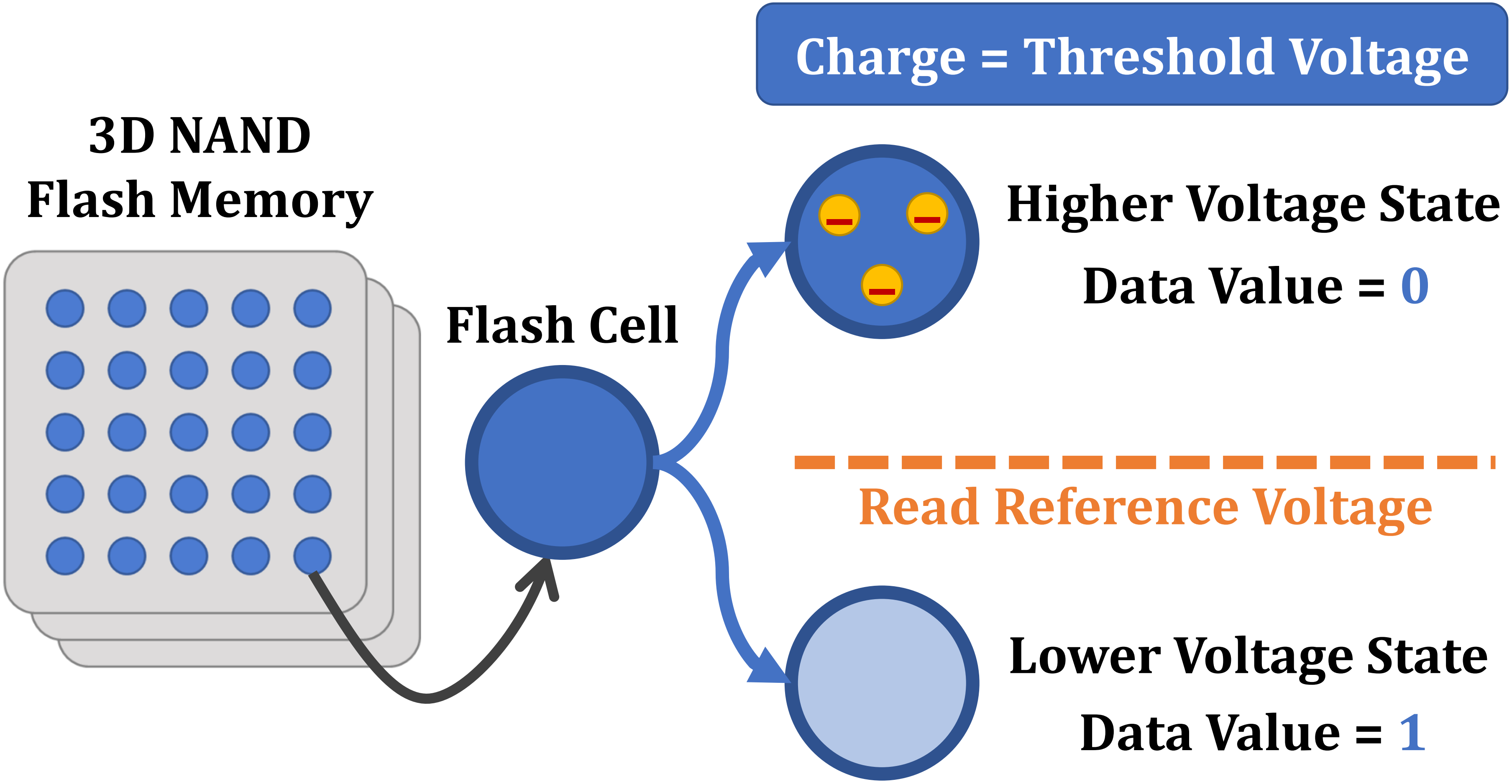
Executive Summary

- 3D NAND susceptible to **early retention errors**
  - Charge leaks out of flash cell quickly after programming
  - Two unreported factors: ***self-recovery* and *temperature***
- We study *self-recovery* and *temperature* effects
  - **Experimental characterization** of *real* 3D NAND chips
  - **Unified Self-Recovery and Temperature (URT) Model**
    - Predicts impact of retention loss, wearout, self-recovery, temperature on **flash cell voltage**
    - **Low prediction error rate: 4.9%**
- We develop a new technique to improve flash reliability
  - **HeatWatch**
    - Uses URT model to find optimal read voltages for 3D NAND flash
    - **Improves flash lifetime by 3.85x**

Outline

- Executive Summary
- **Background on NAND Flash Reliability**
- Characterization of Self-Recovery and Temperature Effect on Real 3D NAND Flash Memory Chips
- URT: Unified Self-Recovery and Temperature Model
- HeatWatch Mechanism
- Conclusion

3D NAND Flash Memory Background



Charge = Threshold Voltage

3D NAND
Flash Memory

Flash Cell

Higher Voltage State

Data Value = 0

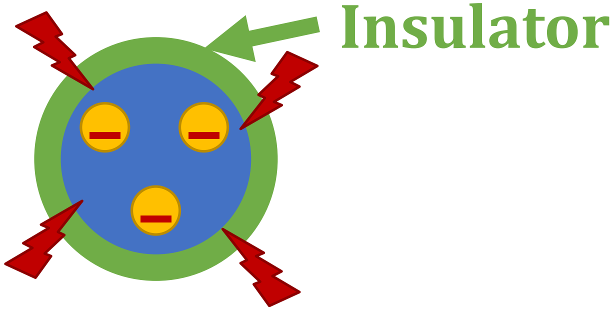
Read Reference Voltage

Lower Voltage State

Data Value = 1

Flash Wearout

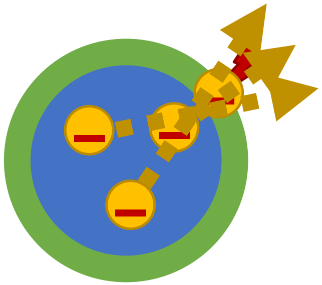
Program/Erase (P/E) → Wearout



Wearout Effects:

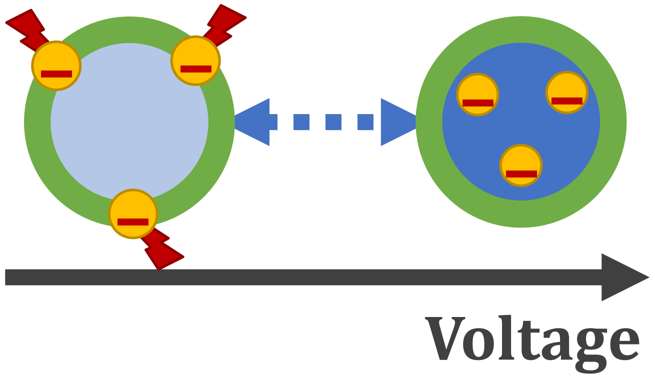
1. Retention Loss

(voltage shift over time)



2. Program Variation

(init. voltage difference b/w states)



Wearout Introduces Errors

Improving Flash Lifetime

Errors introduced by wearout
limit flash lifetime
(measured in P/E cycles)

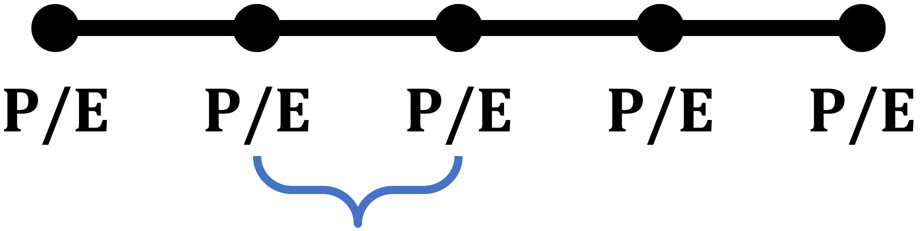
Two Ways to Improve Flash Lifetime →

Exploiting the Self-Recovery Effect

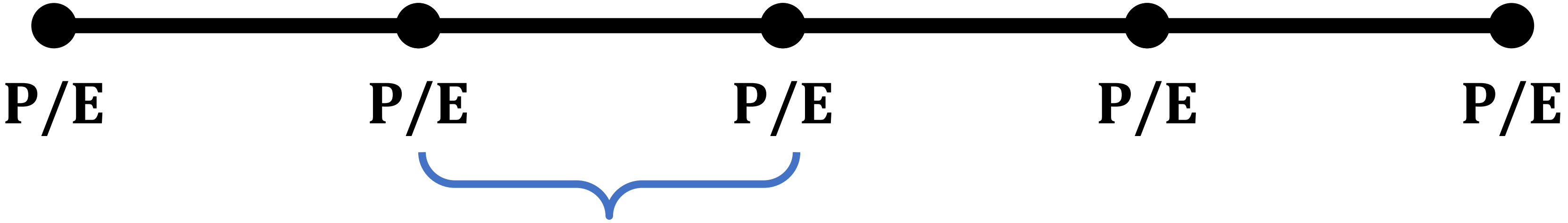
Exploiting the Temperature Effect

Exploiting the Self-Recovery Effect

Partially repairs damage due to wearout


P/E P/E P/E P/E P/E

Dwell Time: Idle Time Between P/E Cycles

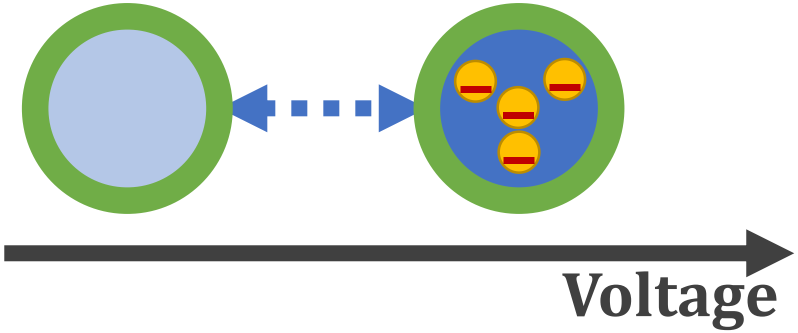

P/E P/E P/E P/E P/E

Longer Dwell Time: More Self-Recovery

Reduces Retention Loss

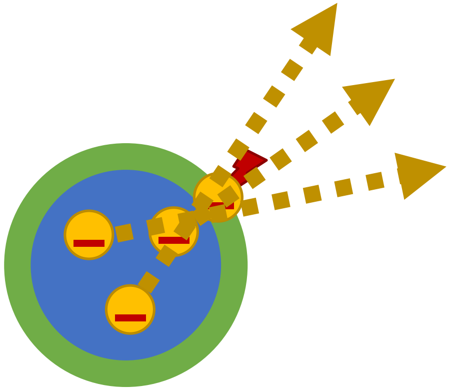
Exploiting the Temperature Effect

High Program Temperature



Increases Program Variation

High Storage Temperature



Accelerates Retention Loss

Prior Studies of Self-Recovery/Temperature

	Planar (2D) NAND	**3D NAND**
Self-Recovery Effect	✓ Mielke 2006	✗
Temperature Effect	✓ JEDEC 2010 (no characterization)	✗

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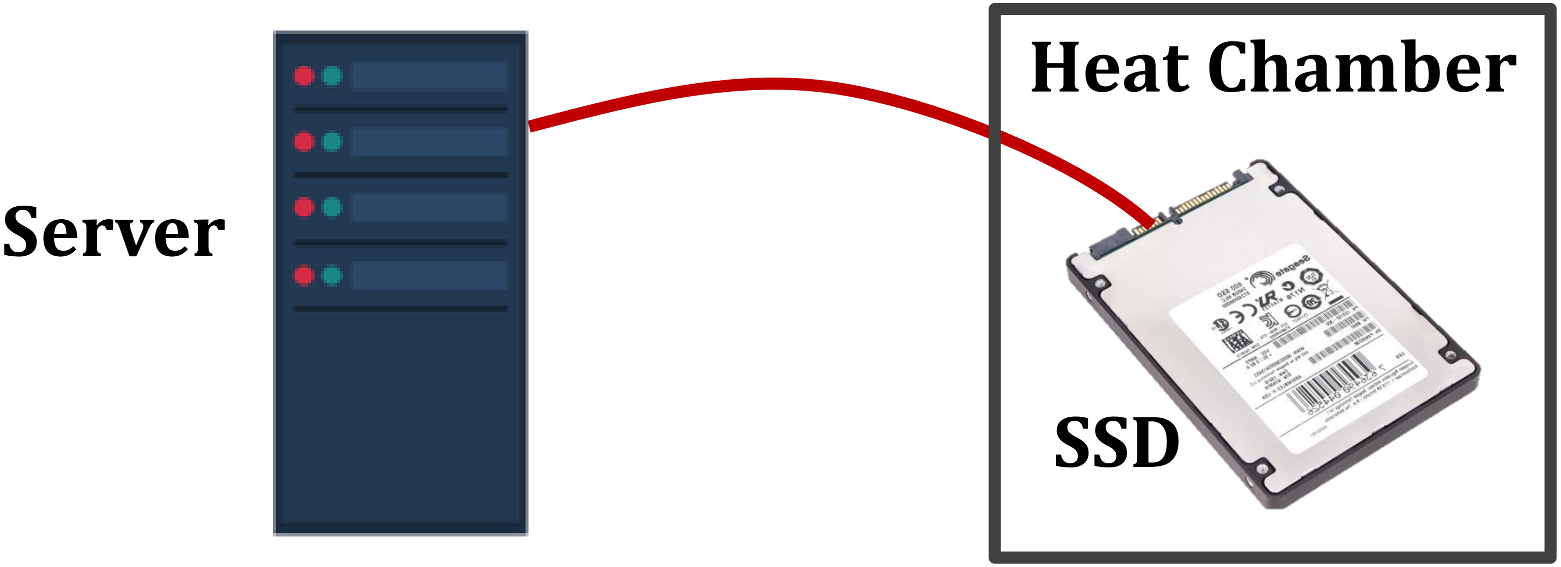
- **Characterization of Self-Recovery and Temperature Effect on Real 3D NAND Flash Memory Chips**
- URT: Unified Self-Recovery and Temperature Model
- HeatWatch Mechanism
- Conclusion

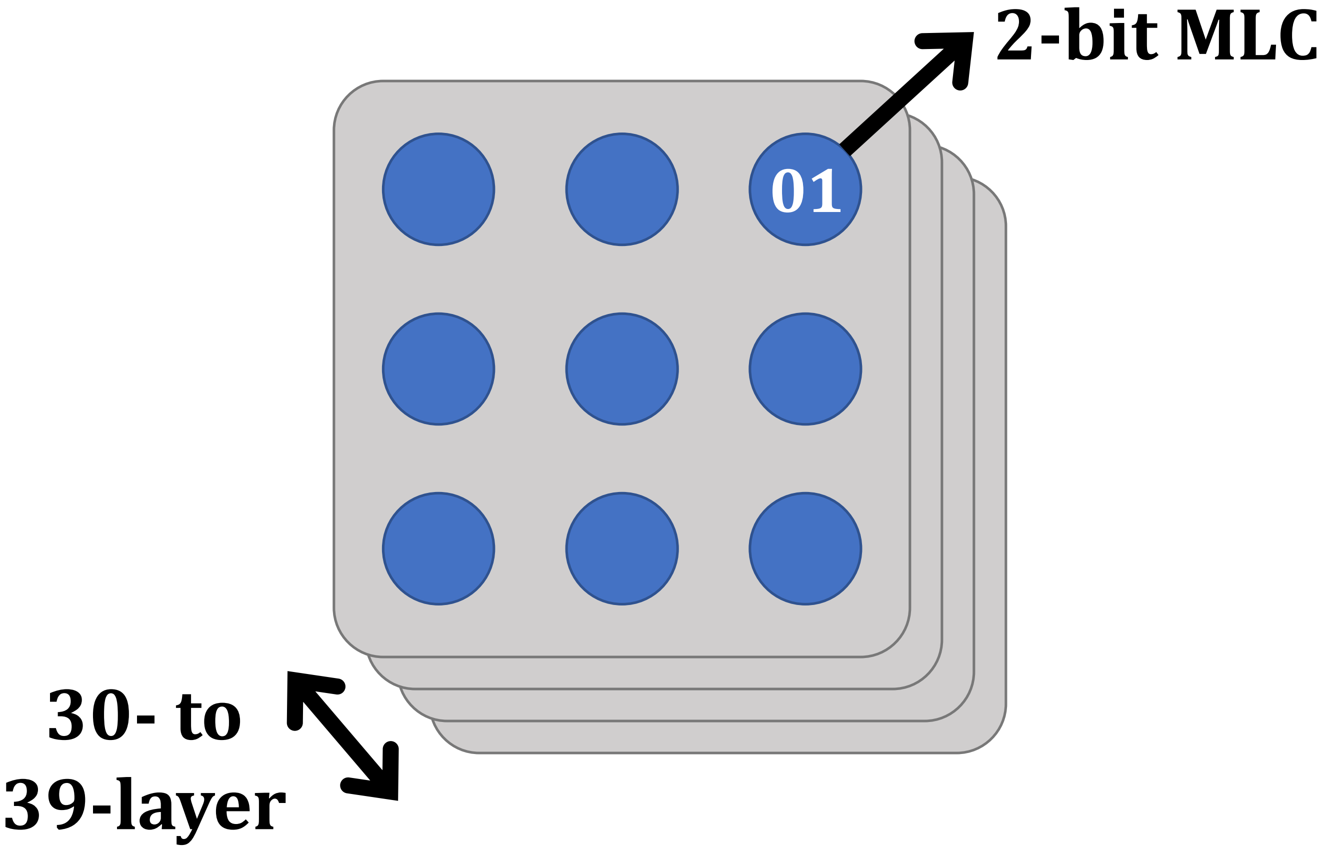
Characterization Methodology

- Modified firmware version in the flash controller
  - Control the read reference voltage of the flash chip
  - Bypass ECC to get raw NAND data (with raw bit errors)
- Control temperature with a heat chamber

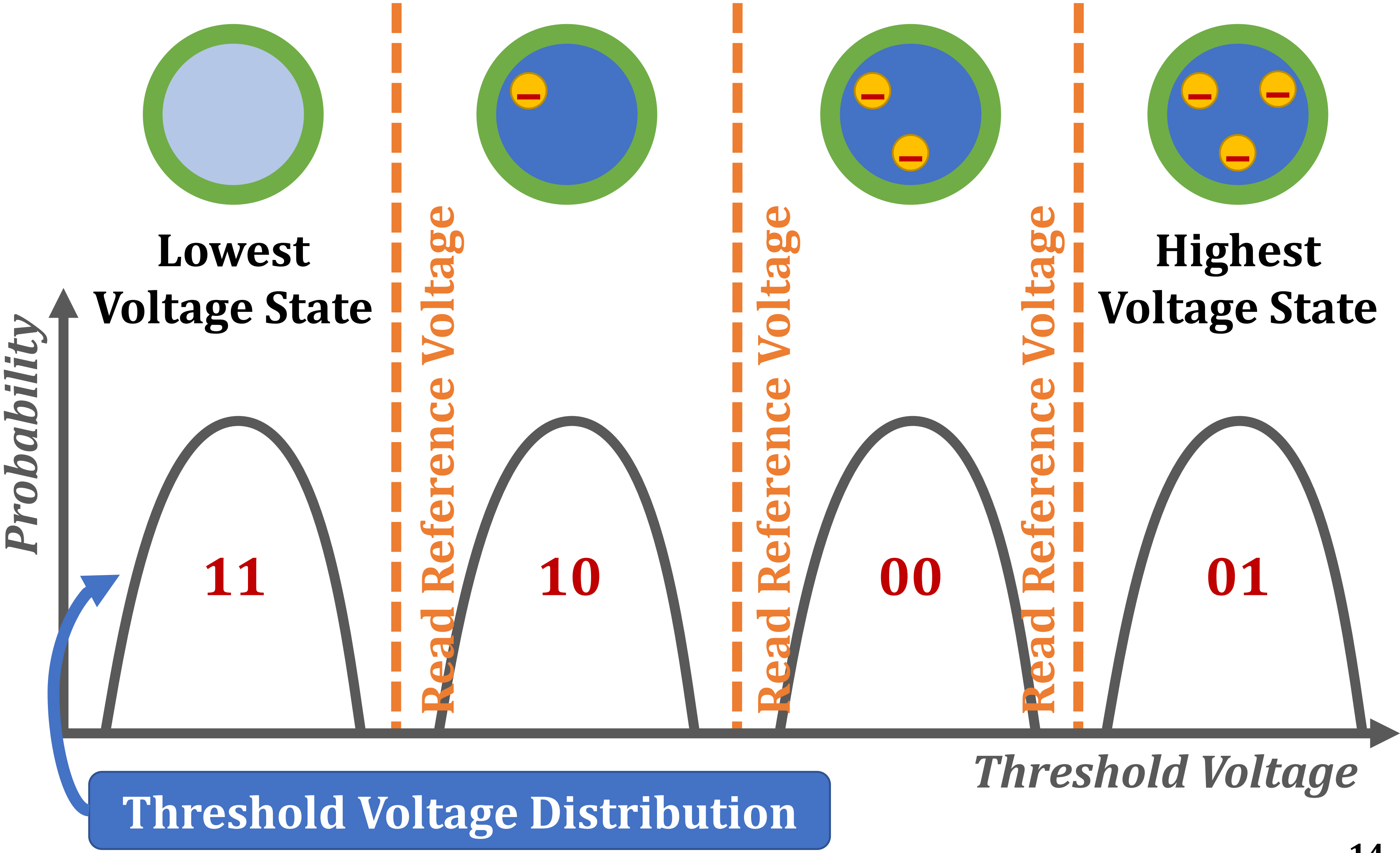


Characterized Devices

Real 30-39 Layer 3D MLC NAND Flash Chips

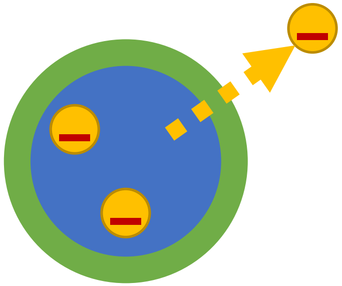


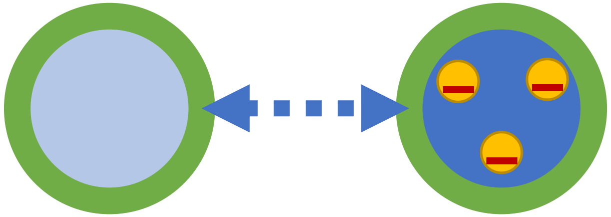
MLC Threshold Voltage Distribution Background



Characterization Goal

Characterized Metrics





Retention Loss Speed

(how fast voltage shifts over time)

Program Variation

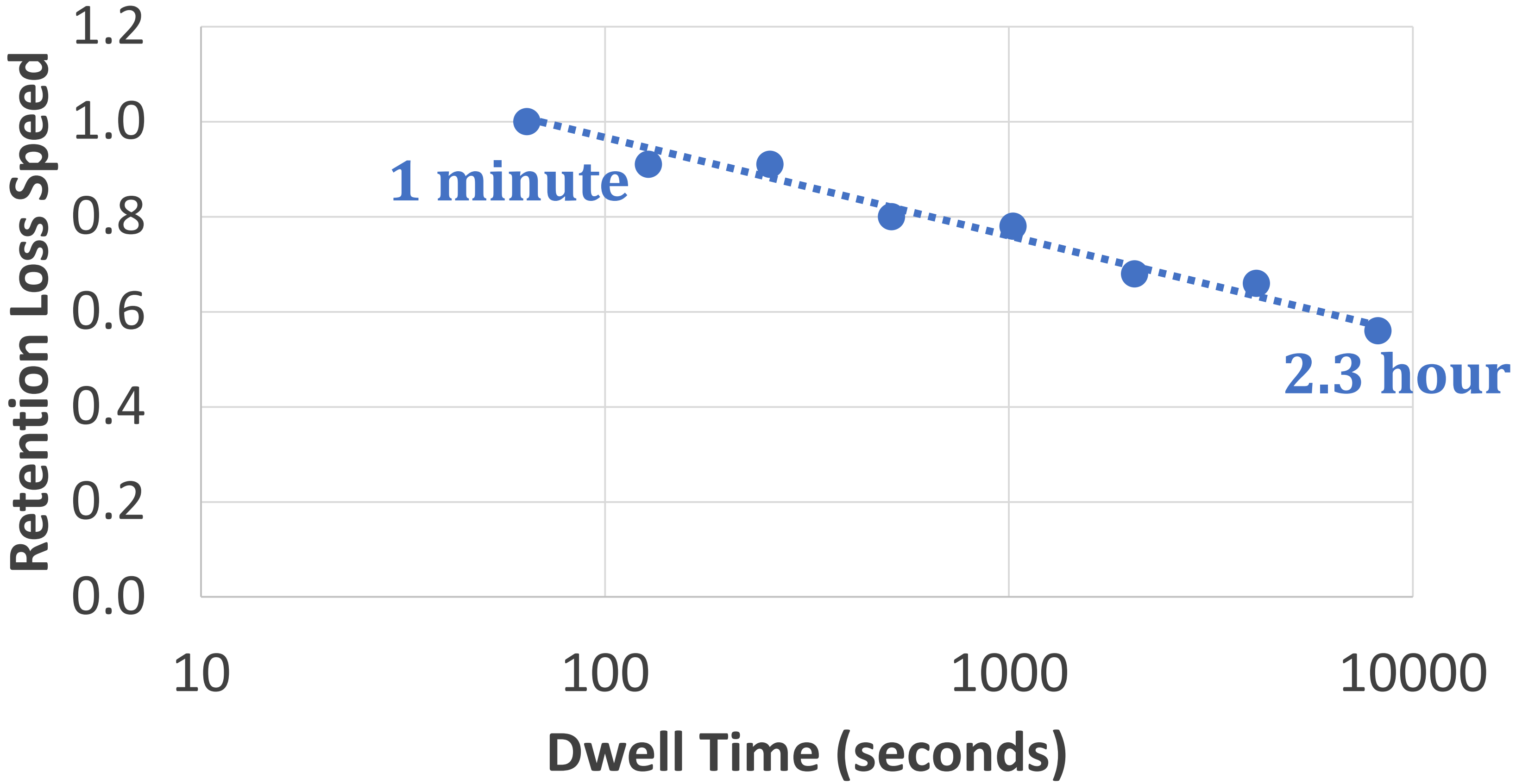
(initial voltage difference between states)

Characterized Phenomena

Self-Recovery Effect

Temperature Effect

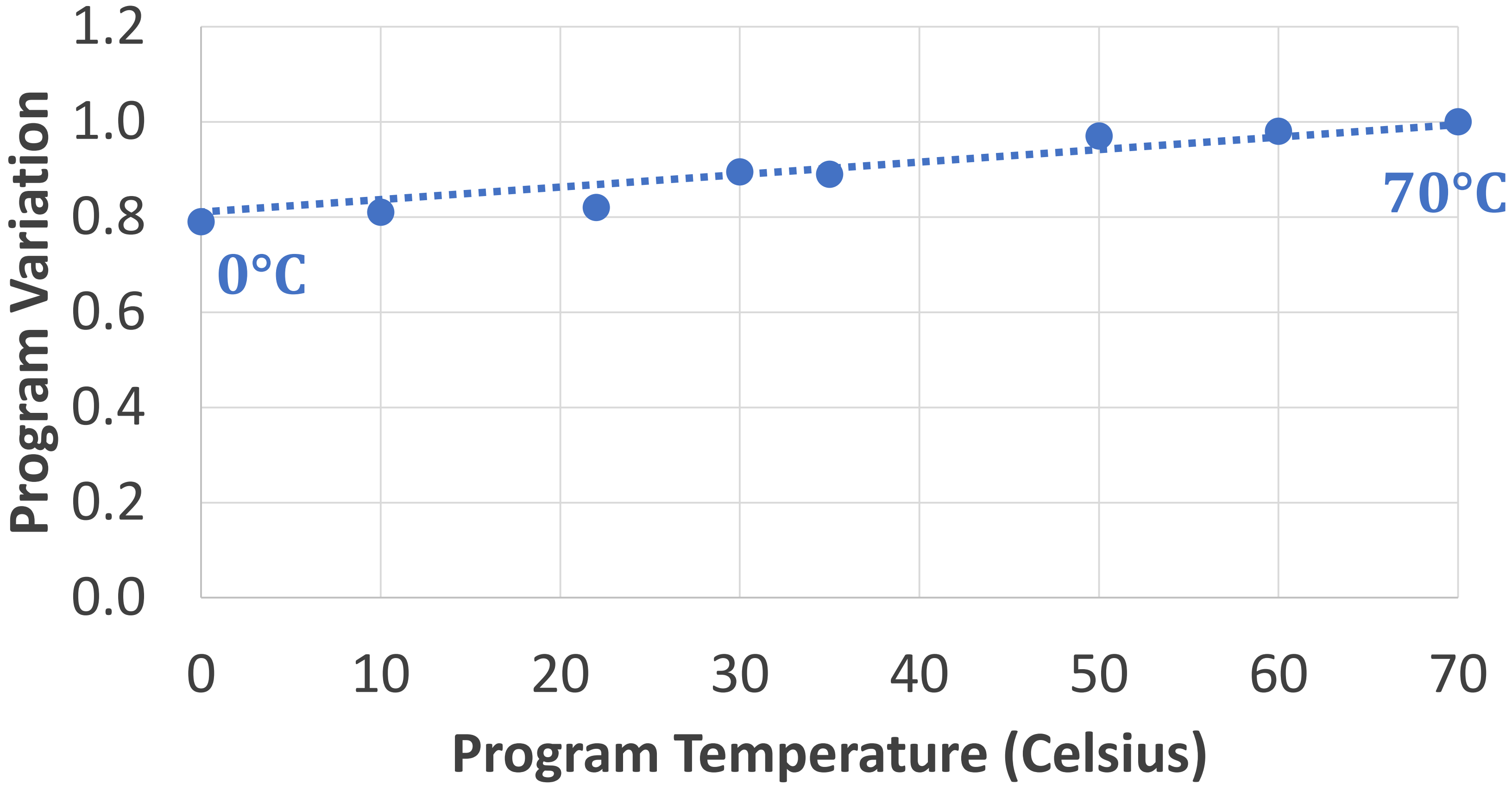
Self-Recovery Effect Characterization Results



Dwell time: Idle time between P/E cycles

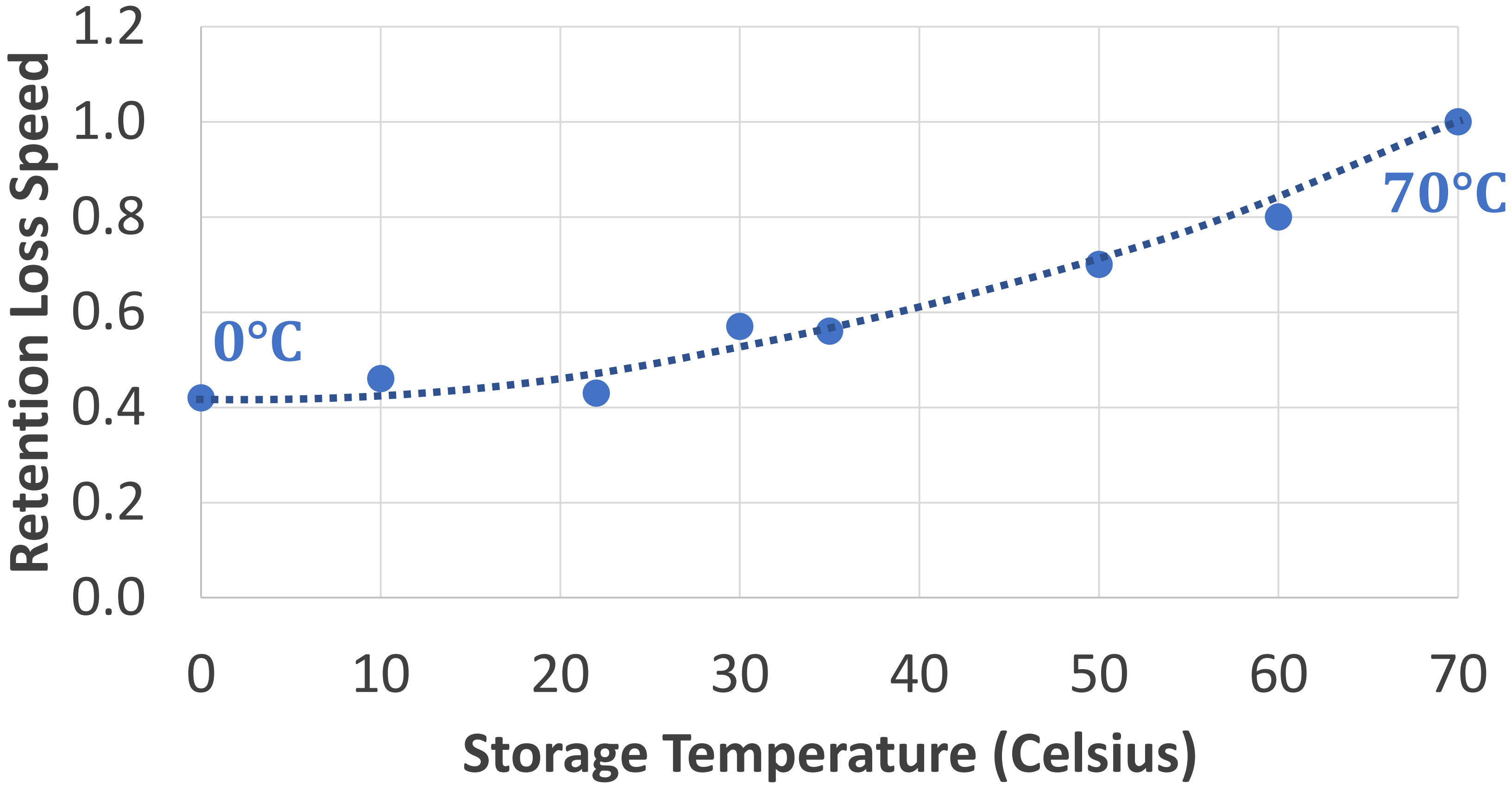
Increasing dwell time from 1 minute to 2.3 hours slows down retention loss speed by 40%

Program Temperature Effect Characterization Results



Increasing program temperature from 0°C to 70°C improves program variation by 21%

Storage Temperature Effect Characterization Results



Lowering storage temperature from 70°C to 0°C slows down retention loss speed by 58%

Characterization Summary

Major Results:

- *Self-recovery* affects retention loss speed
- Program *temperature* affects program variation
- *Storage temperature* affects retention loss speed

Unified Model

Other Characterizations Methods in the Paper:

- More detailed results on self-recovery and temperature
  - Effects on error rate
  - Effects on threshold voltage distribution
- Effects of recovery cycle (P/E cycles with long dwell time) on retention loss speed

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- **URT: Unified Self-Recovery and Temperature Model**
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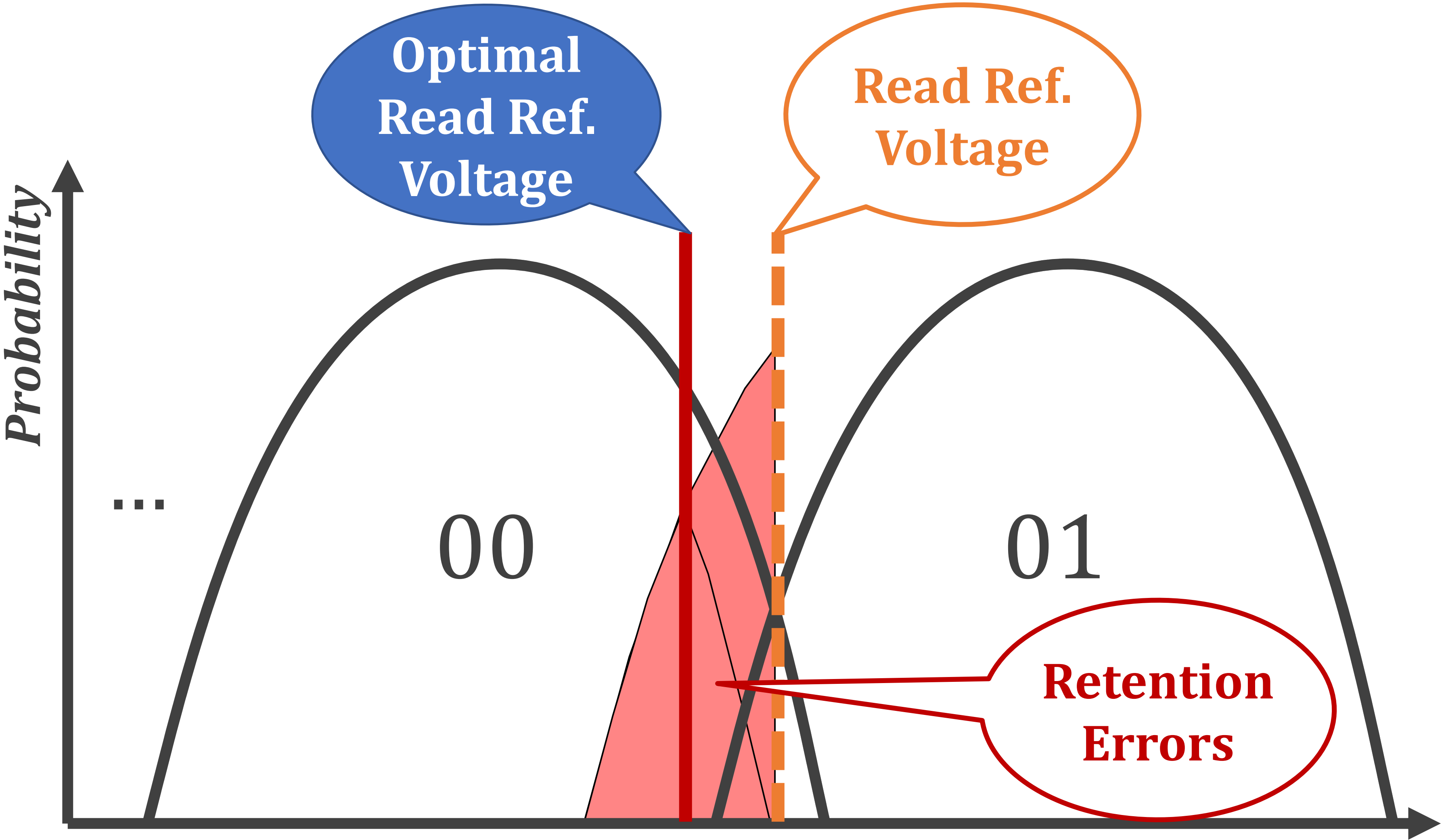
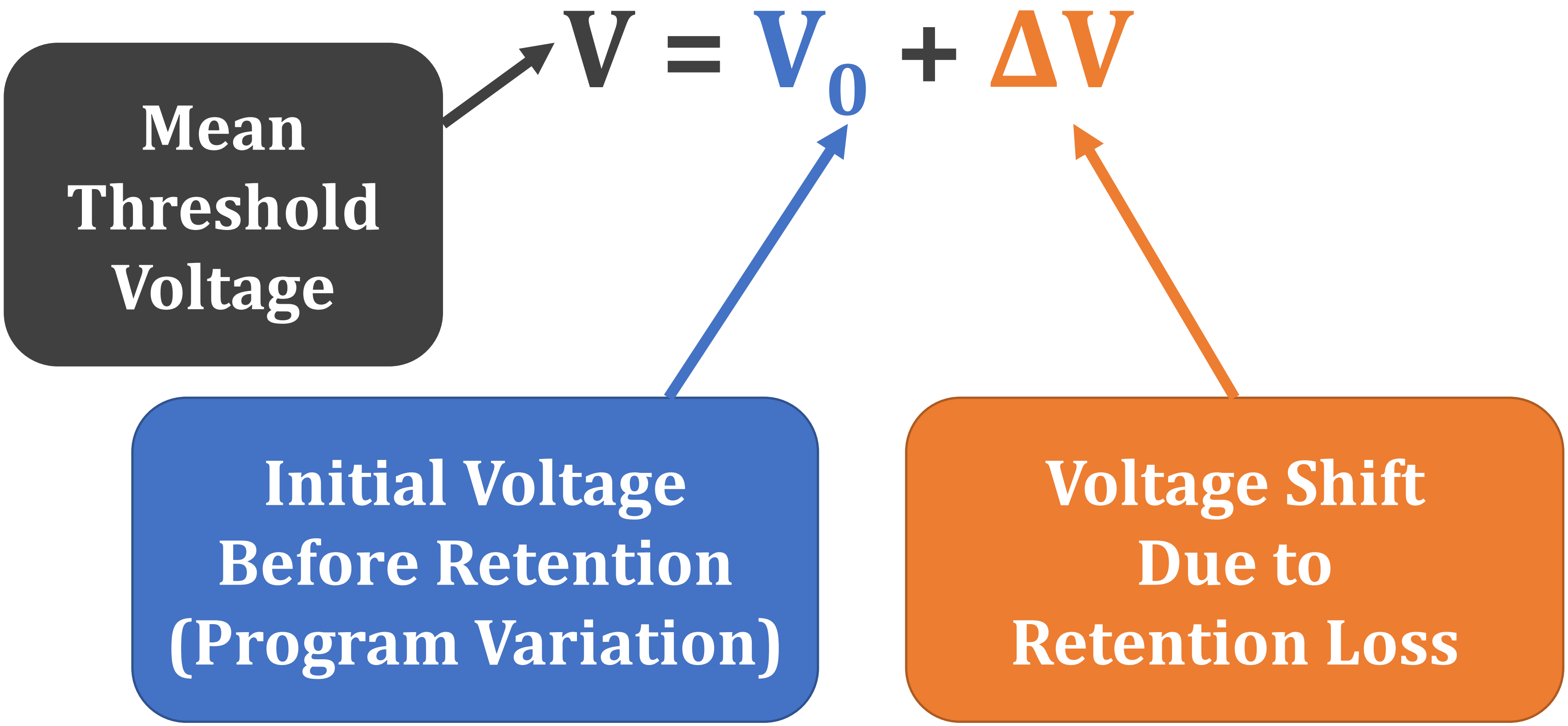
Minimizing 3D NAND Errors



Optimal read reference voltage minimizes 3D NAND errors

Predicting the Mean Threshold Voltage

Our URT Model:



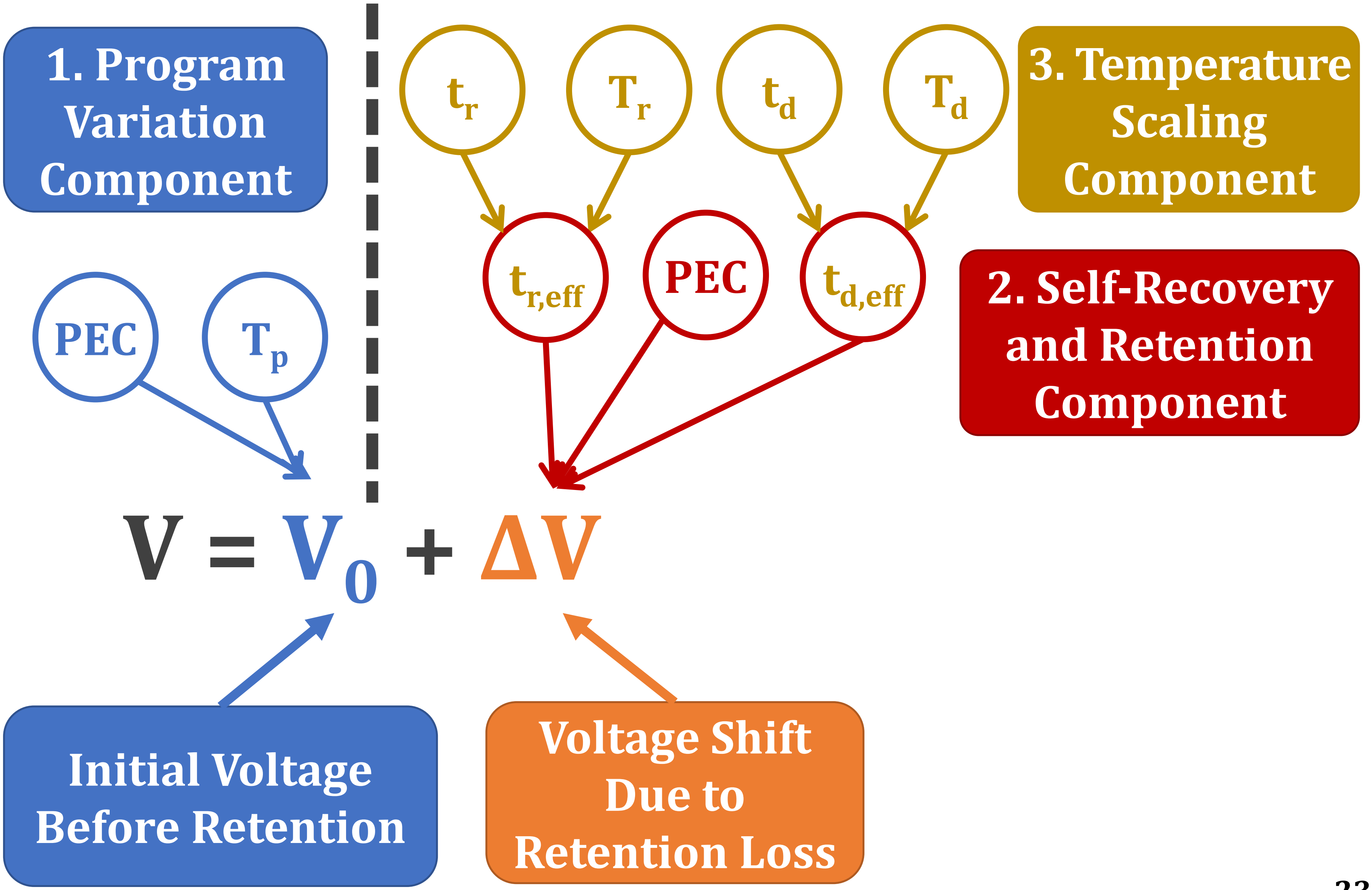
$$V = V_0 + \Delta V$$

Mean Threshold Voltage

Initial Voltage Before Retention (Program Variation)

Voltage Shift Due to Retention Loss

URT Model Overview



1. Program Variation Component

PEC

T_p

t_r

T_r

t_d

T_d

3. Temperature Scaling Component

$t_{r,eff}$

PEC

$t_{d,eff}$

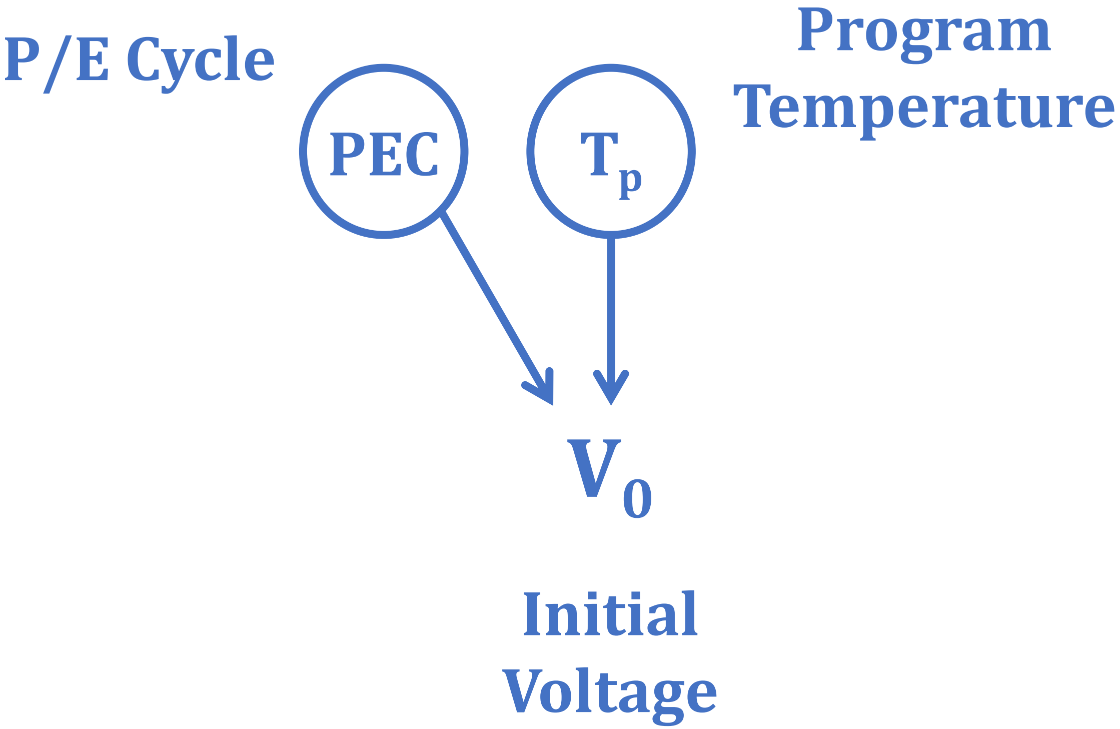
2. Self-Recovery and Retention Component

$$V = V_0 + \Delta V$$

Initial Voltage Before Retention

Voltage Shift Due to Retention Loss

1. Program Variation Component



P/E Cycle

PEC

T_p

Program Temperature

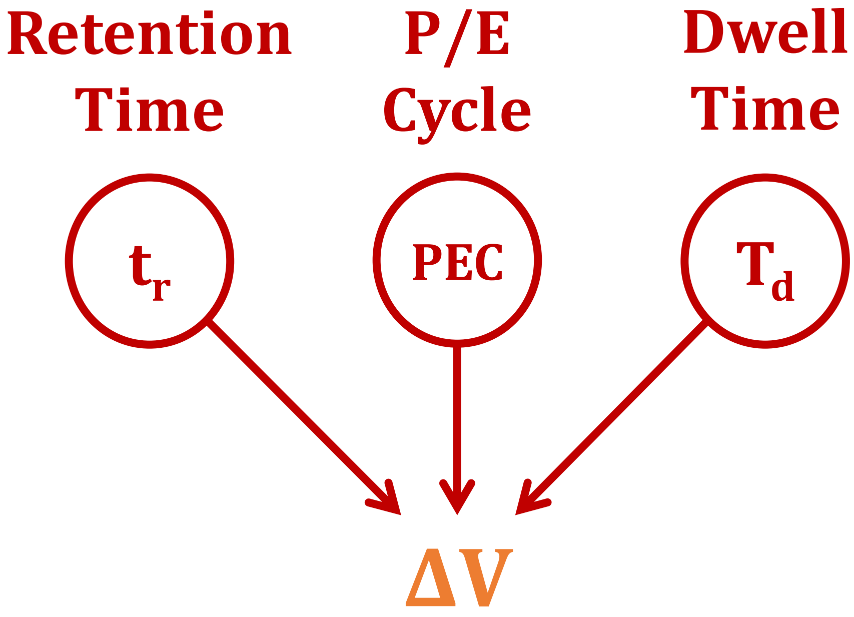
V_0

Initial Voltage

$$V_0 = A \cdot T_p \cdot PEC + B \cdot T_p + C \cdot PEC + D$$

Validation: R^2 = 91.7%

2. Self-Recovery and Retention Component



Retention Time

P/E Cycle

Dwell Time

t_r

PEC

T_d

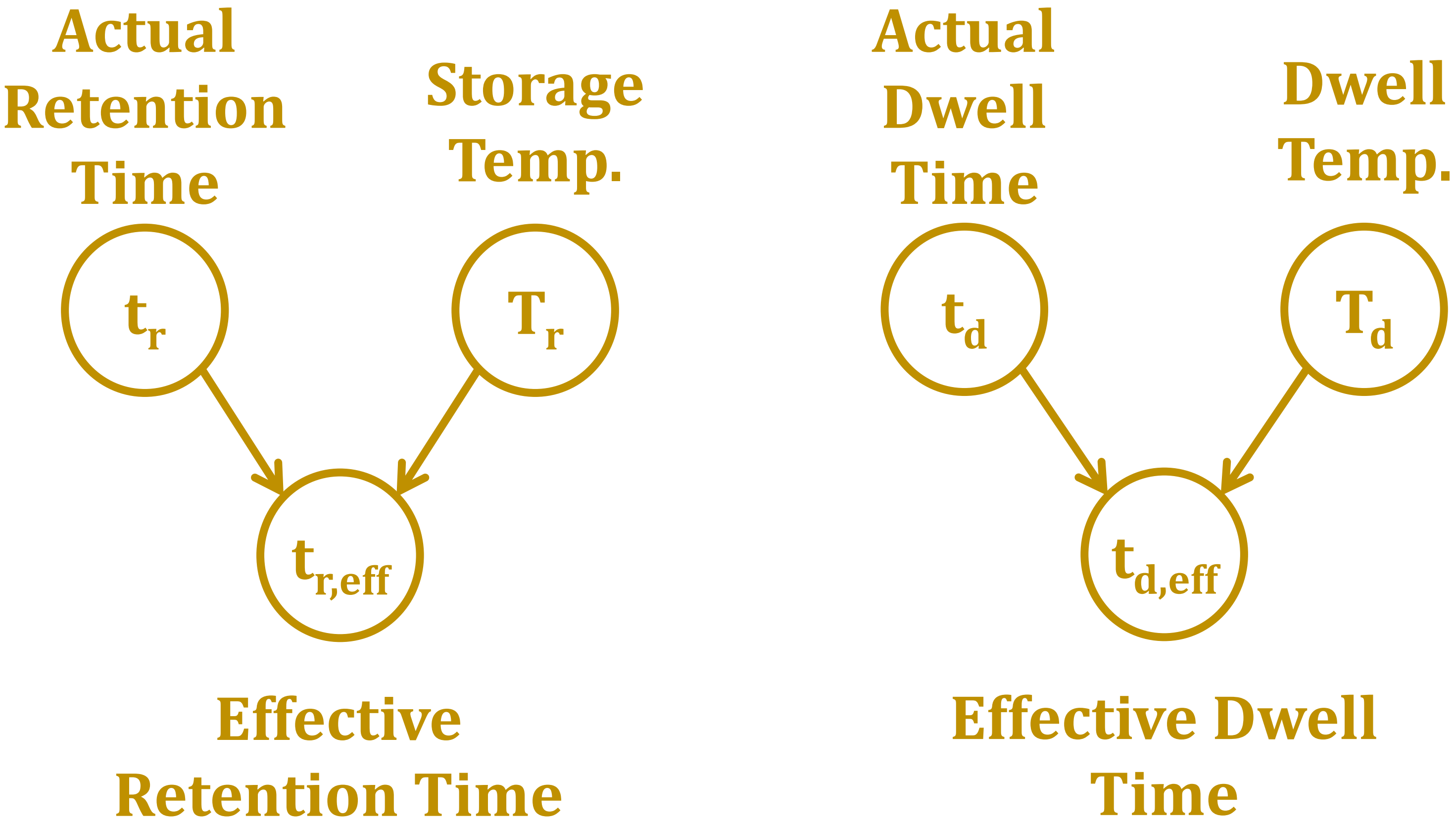
ΔV

Retention Shift

$$\Delta V\left(t_{er}, t_{ed}, PEC\right) = b \cdot (PEC + c) \cdot \ln\left(1 + \frac{t_{er}}{t_0 + a \cdot t_{ed}}\right)$$

Validation: 3x more accurate than state-of-the-art model

3. Temperature Scaling Component



Actual Retention Time

Storage Temp.

t_r

T_r

$t_{r,eff}$

Effective Retention Time

Actual Dwell Time

Dwell Temp.

t_d

T_d

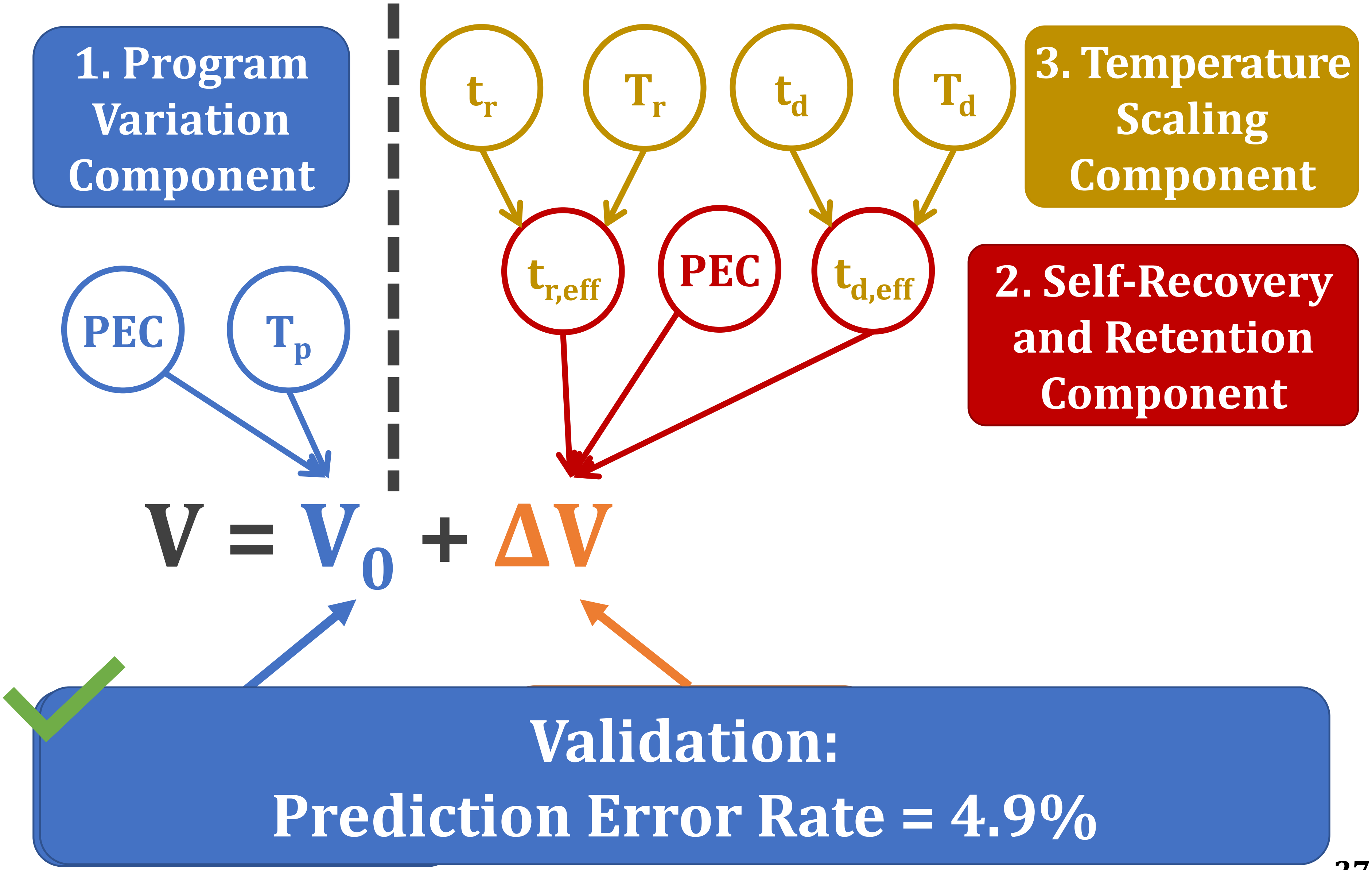
$t_{d,eff}$

Effective Dwell Time

Arrhenius Equation: $$AF = \frac{t_{real}}{t_{room}} = \exp\left(\frac{E_a}{k_B} \cdot \left(\frac{1}{T_{real}} - \frac{1}{T_{room}}\right)\right)$$

Validation: Adjust an important parameter, E_a, from 1.1 eV to 1.04 eV

URT Model Summary



1. Program Variation Component

3. Temperature Scaling Component

2. Self-Recovery and Retention Component

$$V = V_0 + \Delta V$$

Validation:
Prediction Error Rate = 4.9%

Outline

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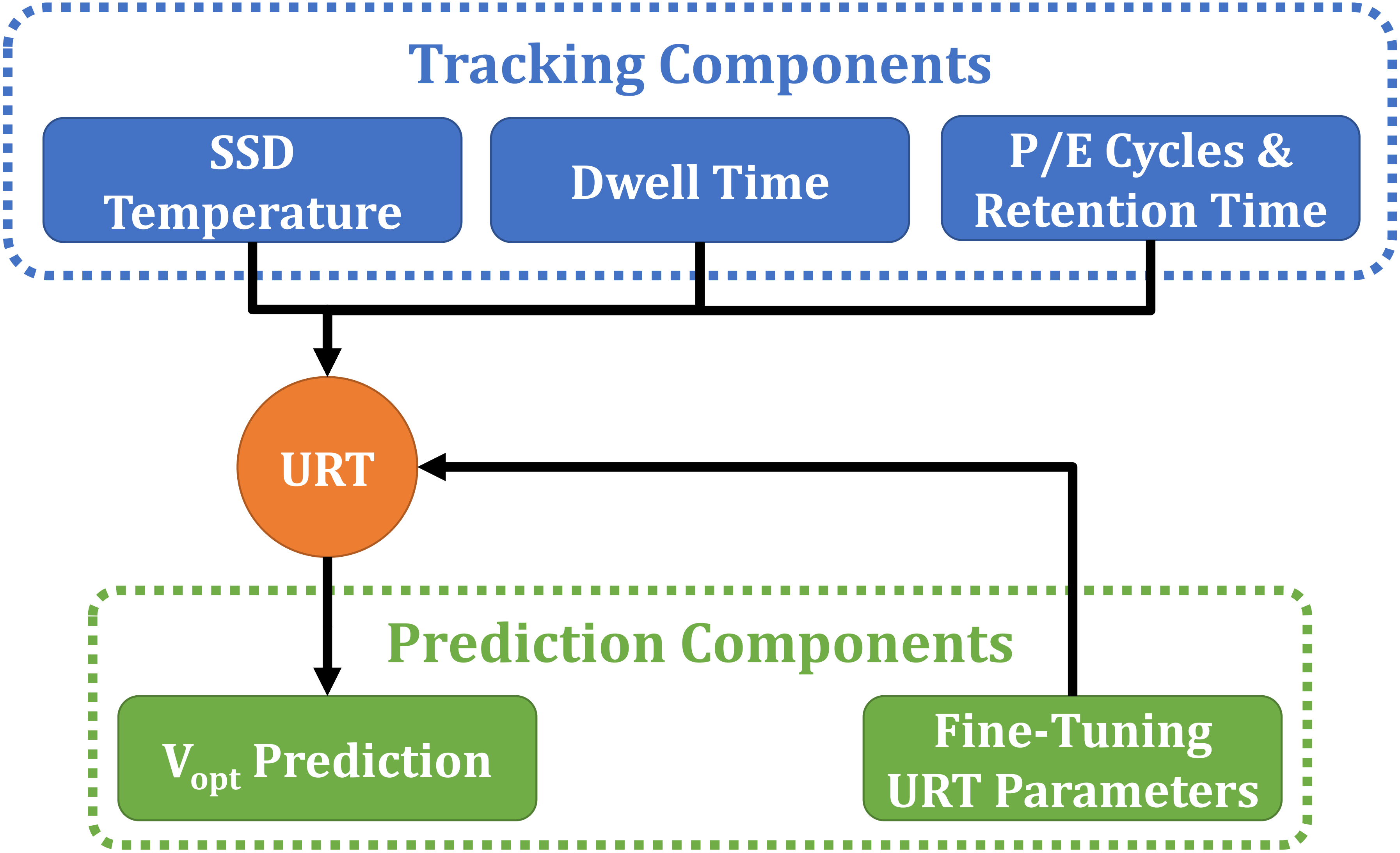
- Conclusion

HeatWatch Mechanism

- **Key Idea**
  - **Predict change in threshold voltage distribution** by using the URT model
  - **Adapt read reference voltage to near-optimal** (V_{opt}) based on predicted change in voltage distribution

HeatWatch Mechanism Overview



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

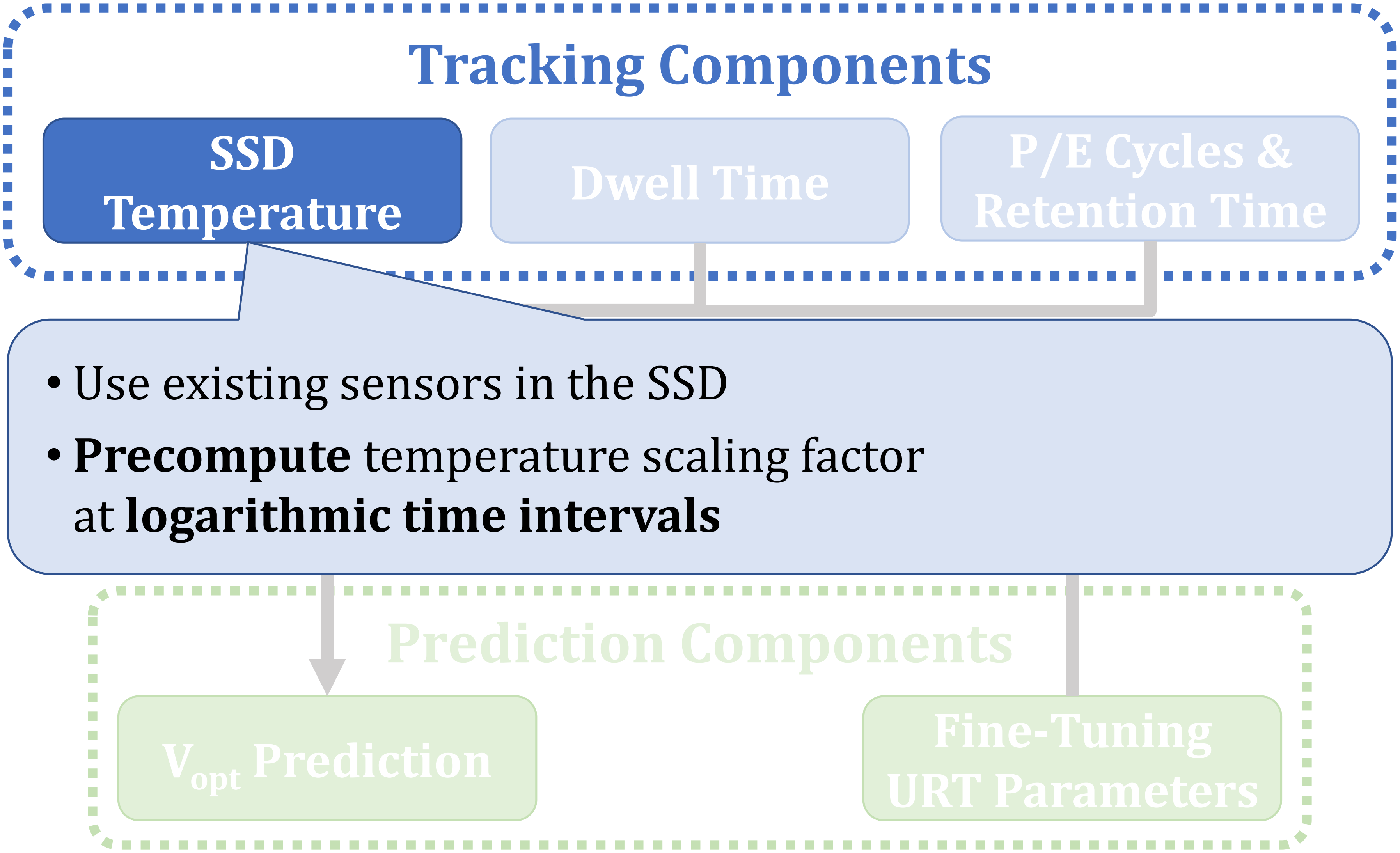
URT

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

Tracking SSD Temperature



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

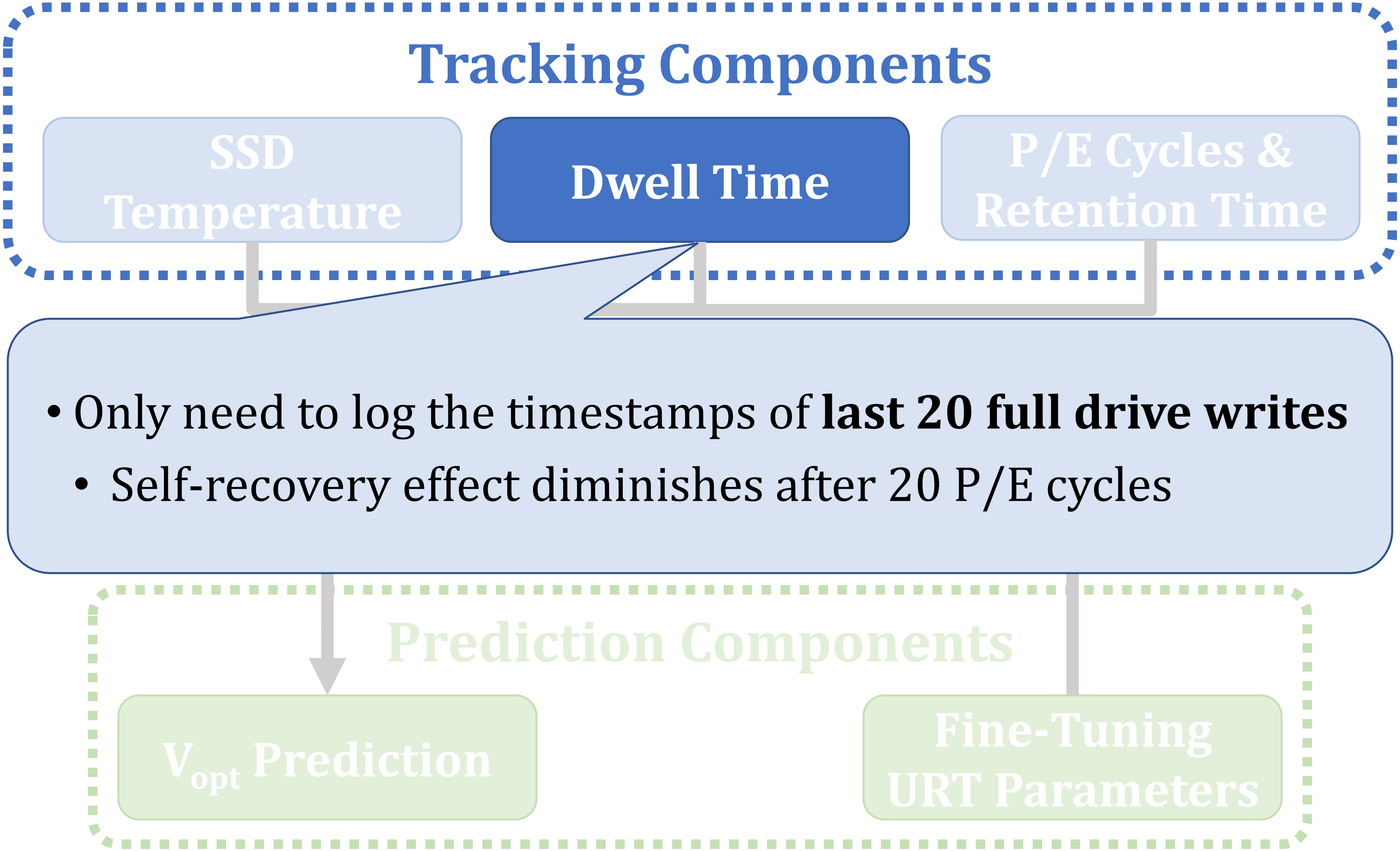
- Use existing sensors in the SSD
- **Precompute** temperature scaling factor at **logarithmic time intervals**

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

Tracking Dwell Time



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

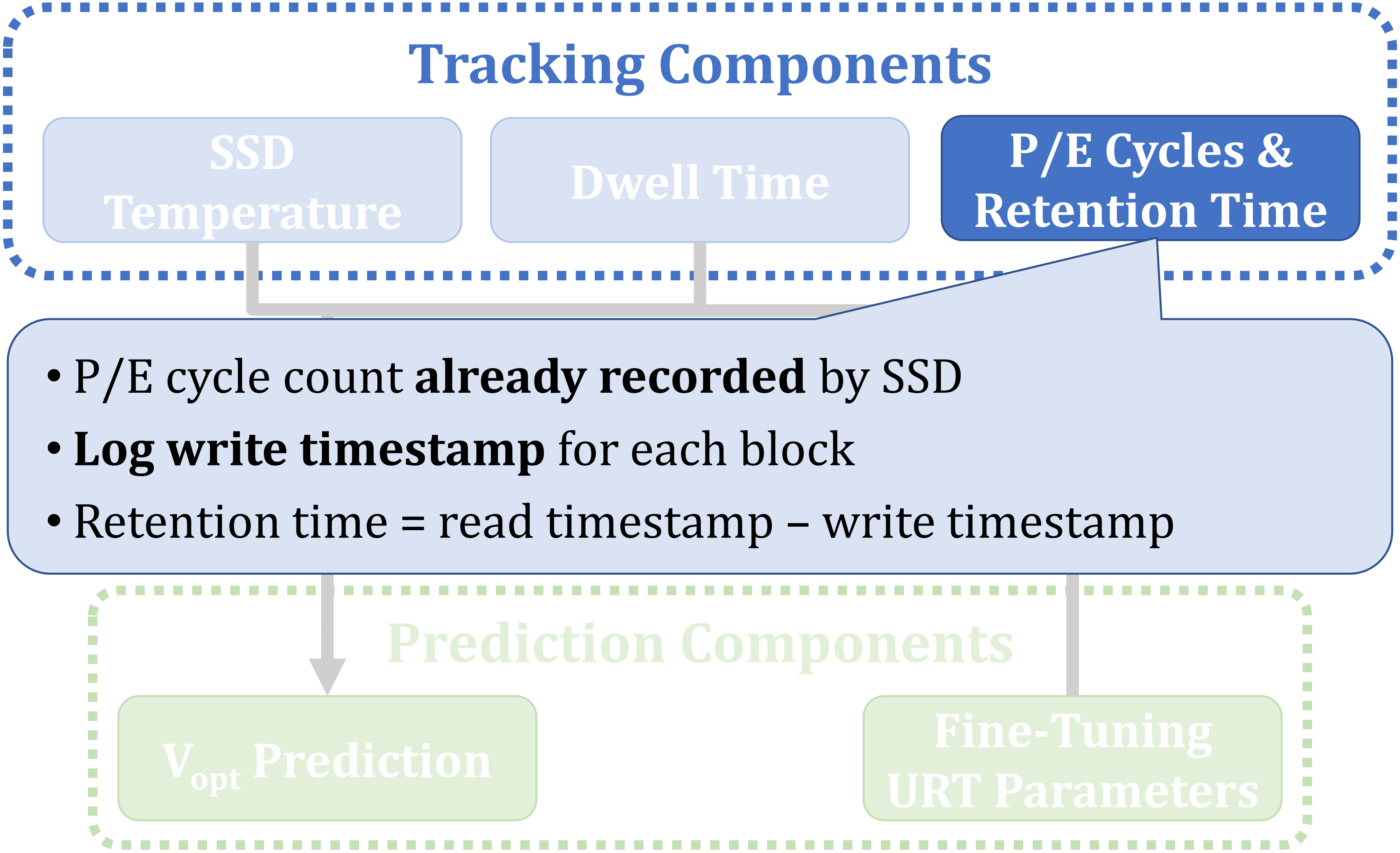
- Only need to log the timestamps of **last 20 full drive writes**
  - Self-recovery effect diminishes after 20 P/E cycles

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

Tracking P/E Cycles and Retention Time



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

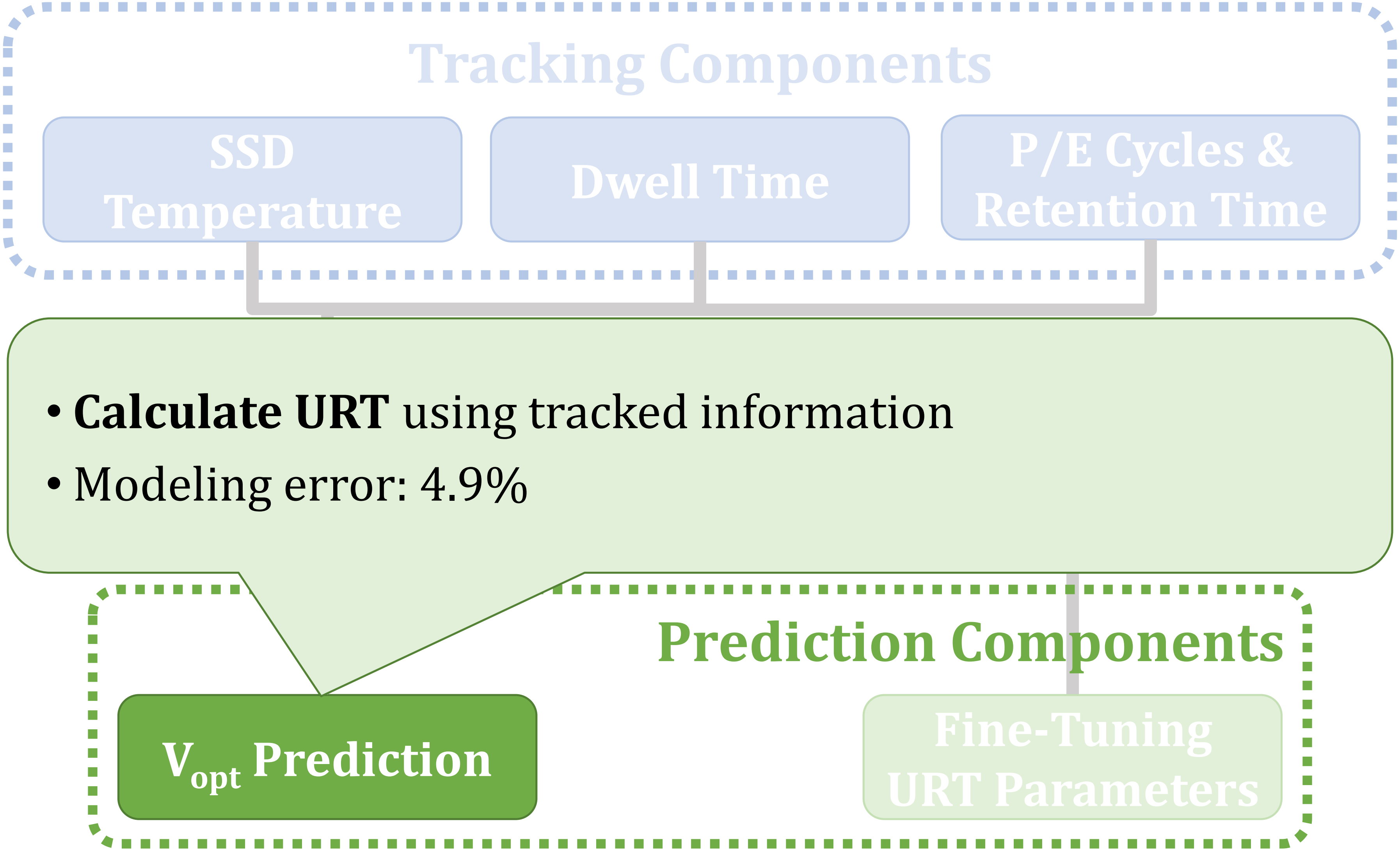
- P/E cycle count **already recorded** by SSD
- **Log write timestamp** for each block
- Retention time = read timestamp – write timestamp

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

Predicting Optimal Read Reference Voltage



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

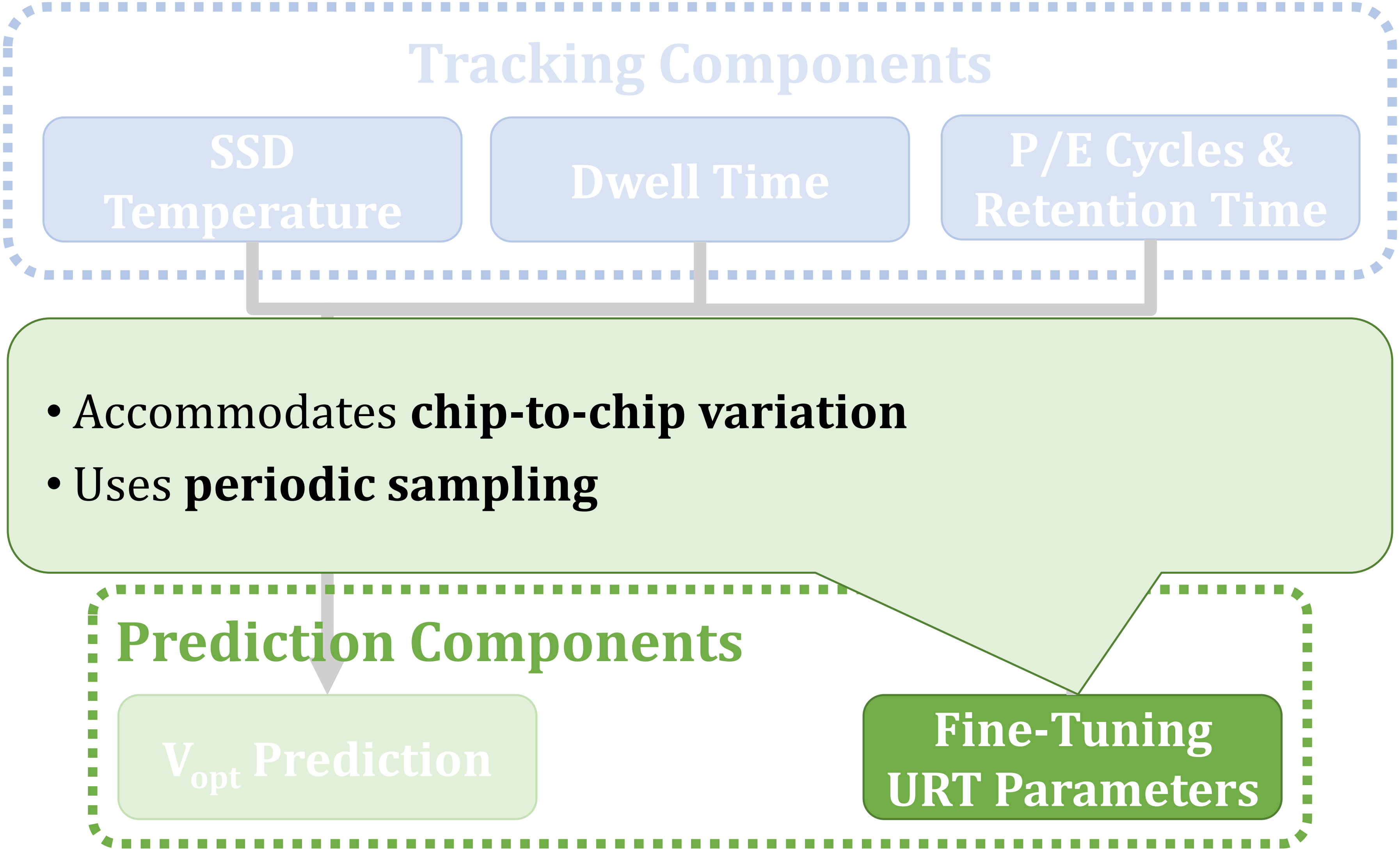
- **Calculate URT** using tracked information
- Modeling error: 4.9%

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

Fine-Tuning URT Parameters Online



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

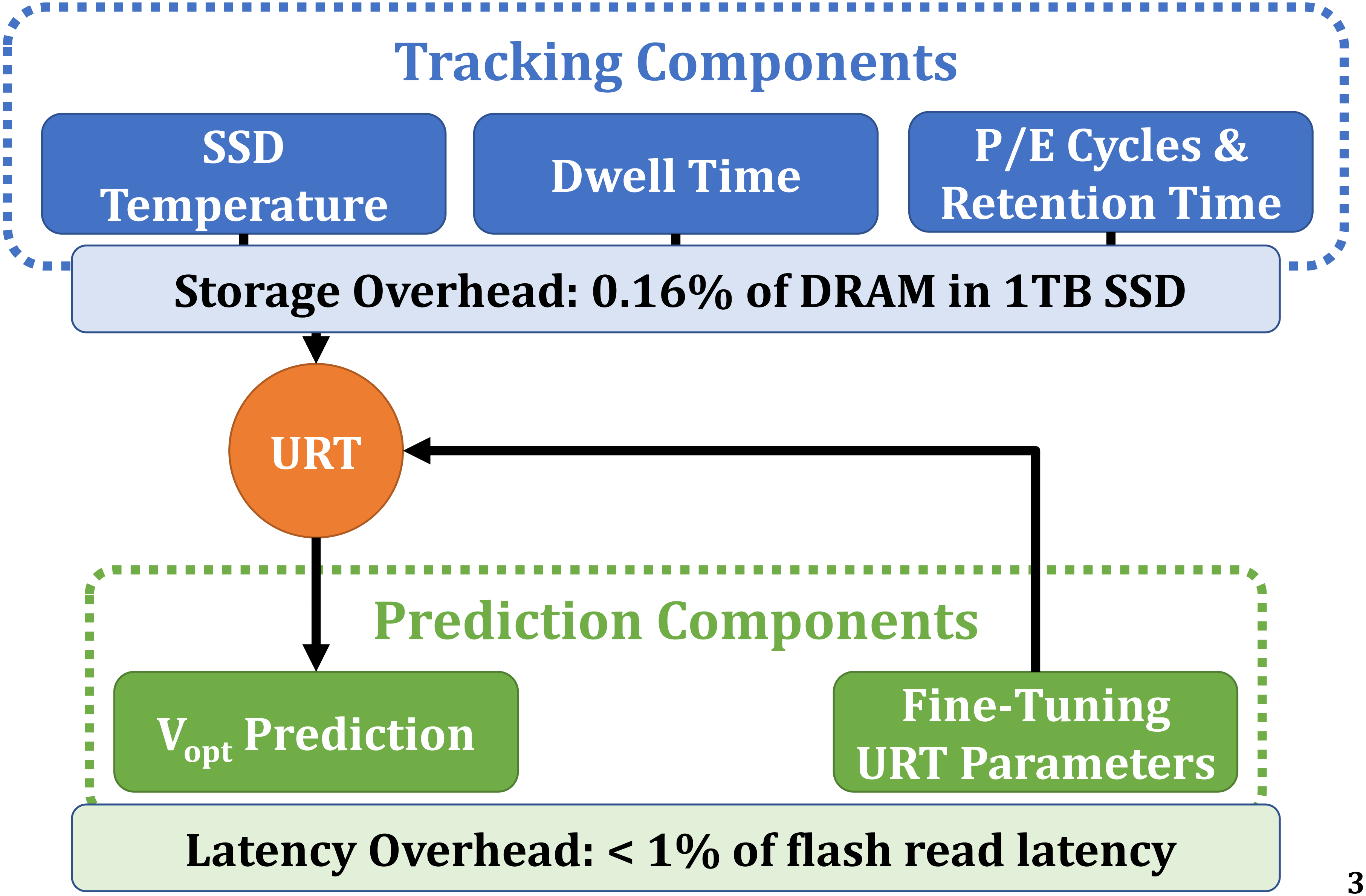
- Accommodates **chip-to-chip variation**
- Uses **periodic sampling**

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

HeatWatch Mechanism Summary



Tracking Components

SSD Temperature

Dwell Time

P/E Cycles & Retention Time

Storage Overhead: 0.16% of DRAM in 1TB SSD

URT

Prediction Components

V_{opt} Prediction

Fine-Tuning URT Parameters

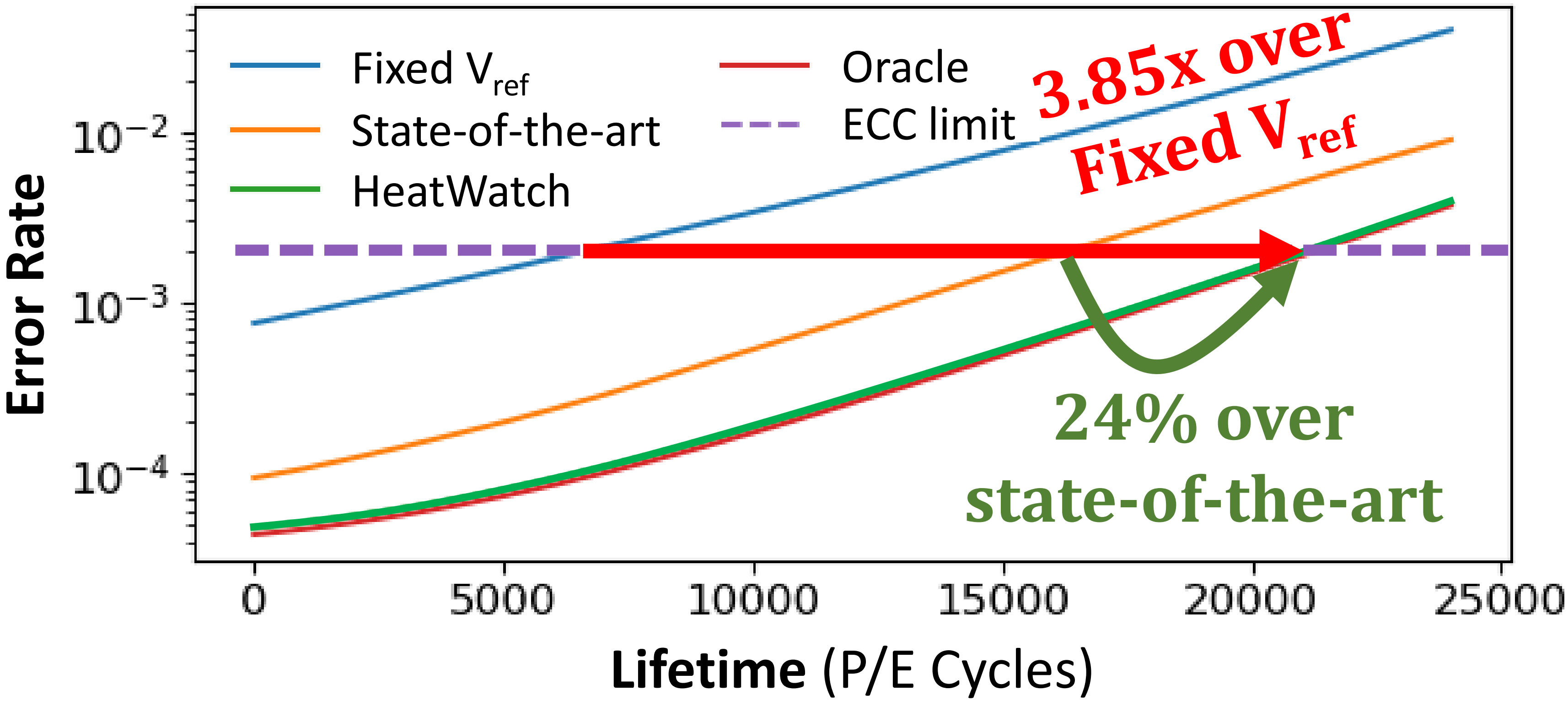
Latency Overhead: < 1% of flash read latency

HeatWatch Evaluation Methodology

- **28 real workload storage traces**
  - MSR-Cambridge
  - We use **real dwell time, retention time values** obtained from traces

- **Temperature Model:**
  Trigonometric function + Gaussian noise
  - Represents periodic temperature variation in each day
  - Includes small transient temperature variation

HeatWatch Greatly Improves Flash Lifetime



HeatWatch improves lifetime by capturing the effect of retention, wearout, self-recovery, temperature

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Conclusion

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    - **Improves flash lifetime by 3.85x**

Flash Memory Summit

HeatWatch

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Paper reference:
"HeatWatch: Improving 3D NAND Flash Memory Device Reliability by Exploiting Self-Recovery and Temperature-Awareness“, HPCA 2018
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Our Flash Memory Works (II)

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- Retention noise study and management
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Our Flash Memory Works (V)

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- Flash errors in the field
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Referenced Papers and Talks

- All are available at
  - https://www.ece.cmu.edu/~safari/pubs.html
  - https://www.ece.cmu.edu/~safari/talks.html

- And, many other previous works on
  - Challenges and opportunities in memory
  - NAND flash memory errors and management
  - Phase change memory as DRAM replacement
  - STT-MRAM as DRAM replacement
  - Taking advantage of persistence in memory
  - Hybrid DRAM + NVM systems
  - NVM design and architecture