

## Wayne State University Dept of Electrical & Computer Engineering Brammer Lecture Series, 3 Oct. 2007

# Towards Speech Recognition in Silicon: The Carnegie Mellon In Silico Vox Project

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## Speech Recognition Today: Software



## Quality = OK Vocabulary = large



## Quality = poor Vocab = small

The Toshiba UT103, 4 languages,
~3000 phrases, 35 hours on 2AA batteries,
runs on 75MHz Toshiba processor



No way...

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## Today's Best Software Speech Recognizers

### Best-quality recognition is computationally hard

For speaker-independent, large-vocabulary, continuous speech

#### 1-10-100-1000 rule

- ▼ For **~1X** real-time recognition rate
- ▼ For **~10%** word error rate (90% accuracy)
- Need ~100 MB memory footprint
- Need ~100 W power
- Need ~1000 MHz CPU

#### But, this is ~1000X away from what we need

## **About This Talk**

## Some philosophy

Why silicon? Why now? Why us (CMU)?

### A quick tour: How speech recognition works

What happens in a recognizer

#### A silicon architecture

Stripping away all CPU stuff we don't need, focus on essentials

#### Results

- Silicon version: Simulation results
- **FPGA** version: Live, running hardware-based recognizer

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## **Compelling Next-Generation Applications...**

...want to go fast. Very fast. Faster than realtime.

**Example: Audio Mining** 



Fast forward your DVD FIND: "Hasta la vista, baby!"

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## **Compelling Next-Generation Applications...**



#### 3 years after 9/11, FBI still had **123,000** hrs of untranslated foreign audio

...could use speech→text @ 100X -1000X realtime

(Text→text translation also exists—diff problem)

Could we triage these huge media streams to allocate scarce human intel assets?

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## **Compelling Next-Gen Applications...**





## Want low power Very low

- Cell phone has 3W total power budget
- ▼ You get ~300mW for a new feature

1<sup>st-</sup> gen solns still software...

## Doesn't Moore's Law Just Save Us (*Eventually*)?

Yes (sort of...): Transistors keep getting smaller
No (uh oh...): Moore's Law is running out of gas



## **Problems with Moore's Law Scaling**

#### Limits on device size

- Already at atomistic dimensions
- Can't scale forever when devices are already ~100 atoms wide



#### Limits on device speed

- Small devices leak (switches draw a little current when off)
- **¬** Power dissipation  $\alpha$  clk frequency
- → Can't get more performance by just upping GHz on next chip

### Emphasis now on design

- ▼ More parallel architectures...
- ...with clocks running slower
- ...to get performance, but not melt



3-D content<sup>3</sup>
Up to 8MB of L2 cache and 1066 MHz Front Side Bus for an unrivaled multitasking exp

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## Still: Lots of Software-Based Next-Gen Work

### Video indexing

#### The New York Times

Millions of Videos, and Now a Way to Search Inside Them



#### Speech on cellphone



## The Carnegie Mellon In Silico Vox Project

- Our thesis: It's time to liberate speech recognition from the current limitations of software, because we can always do it better in custom silicon
- Our solution: Speech recognition in silicon



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## Aside: About the Name "In Silico Vox"

#### In Vivo

Latin: an experiment done in a living organism...

#### In Vitro

Latin: an experiment done in an artificial lab environment....

#### In Silico

(Not real Latin): an experiment done via computation only....

■ Vox

■ Latin: voice, or word ······









## Why Silicon? Why Now?

### **Why?** Two reasons:

### History

▼ We have some successful **historical** examples of this migration

#### Performance

- Compelling apps need 100X 1000X more performance, now
- Silicon always better than software on speed/power

## **History: Graphics Engines**

#### Nobody paints pixels in software anymore!

▼ Too limiting in max performance. Too inefficient in power.



http://www.nvidia.com

...and on your cellphone too



http://www.mtekvision.com

## Silicon Solution: Speed and Power Wins

#### A famous graph from Prof. Bob Brodersen of Berkeley

- Study looked at 20 designs published at ISSCC, from 1997-2002
- In slightly older technologies, relative to today: 180nm 250nm
- Dedicated designs up to 10,000X better energy efficiency (MOPS/mW)



## Silicon Speed/Power Win: Why?

### Programmability (flexibility) is not free

- Lots of extra overhead for hardware you don't need for every app
- ▼ Baggage to fetch, decode, run instructions, one (or a few) at a time

#### Functional units not well customized to your app

- ▼ If you can use, say, 75 floating point units, or 36 FFT units too bad
- ▼ You still get 8 arithmetic units...

#### MHz/GHz to deliver speed to all users not optimal

- Microprocessors run fast clocks so all apps see good performance
- $\checkmark$  Your app may be able to run a much slower clock  $\rightarrow$  much less power

## **Recent Example: Parallel Radio Baseband DSP**

### 90nm CMOS: adaptive DSP for multipath MIMO channel

- Power efficiency = 2.1GOPS/mW
- Area efficiency = 20GOPS/mm<sup>2</sup>



(Source: Prof. Dejan Markovitz, UCLA)



Measured 34mW @ VDD=385mV

## Why Us...?

### 1 site (Carnegie Mellon), 3 areas of deep expertise

Impossible to do projects like this without cross-area linkages



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## Us: the CMU In Silico Vox Team

Manchu Dragon

From left: Kai Yu, Rob Rutenbar, Edward Lin, Richard Stern, Tsuhan Chen, Patrick Bourke (not shown: Jeff Johnston)

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**What happens in a recognizer** 

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## **How Speech Recognition Works**



## (1) Acoustic Frontend



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## (2) The Scoring Stage

#### Feature vec is a point in high-dimensional space

 Assume each atomic sound we can recognize is also characterized as one a "perfect" point in high-dim (n=39) space



We used to do this using normalized distance as the metric for "likelihood"

#### Problem with using distance

 Space "occupied" by each atomic sound not well modeled as a point



We need to model the shape of the region that defines each sound

## (2) Scoring Stage

### Each feature still a point in high-dimensional space

- But each "atomic sound" is a region of this space
- **Score** each atomic sound with Probability(*sound matches feature*)



Note: (sounds) X (dimensions) X (Gaussians) = BIG

## (3) Search: Speech Models are Layered Models

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## **Context Matters:** At Bottom -- *Triphones*

English has ~50 atomic sounds (phones) but we recognize ~50x50x50 context-dependent triphones

Because "I" sound in "five" is different than the "I" in "nine"



## Also Context at Top: N-gram Language Model



## **Good Speech Models are BIG**



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## Where Does Software Spend its Time?

SPHINX III Execution Time Breakdown



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## Memory Usage? SPHINX 3.0 vs Spec CPU2000

#### Cache sizes

- L1: 64 KB, direct mapped
- DL1: 64 KB, direct mapped
- ▼ UL2: 512 KB, 4-way set assoc

#### **So**...

- Terrible locality (no surprise, graph search + huge datasets)
- Load dominated (no surprise, reads a lot, computes a little)
- Not an insignificant footprint

	SPHINX 3.0	Gcc	Gzip	Equake	
Cycles	53 B	55B	15 B	23 B	
IPC	0.69	0.29	1.05	0.7	
Instruction Mixes					
Loads	0.27	0.25	0.2	0.27	
Stores	0.05	0.15	0.09	0.08	
Branch's	0.14	0.2	0.17	0.12	
Branch Misprediction Rates					
	0.025	0.07	0.08	0.02	
Cache Miss Rates					
DL1	0.04	0.02	0.02	0.03	
L2	0.48	0.06	0.03	0.30	
Memory Footprint					
	64 MB	24 MB	186 MB	42 MB	

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## This Talk: How to Get to Fast...

#### **Audio-mining**

- Very fast recognizers much faster than realtime
- App: search large media streams (DVD) quickly

#### FIND: "Hasta la vista, baby!"



#### Hands-free appliances

- Very portable recognizers high quality result on << 1 watt</p>
- App: interfaces to small devices, cellphone dictation



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## Speech: Complex Task to do in Silicon



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## A Silicon Architecture: Breakdowns



## **Essential Implementation Ideas**

#### Custom precision, everywhere

Every bit counts, no extras, no floating point – all fixed point

### (Almost) no caching

- Like graphics chips: fetch from SDRAM, do careful data placement
- (Little bit of caching for bandwidth filtering on big language models)

#### Aggressive pipelining

If we can possibly overlap computations – we try to do so

#### Algorithm transformation

- ▼ Some software computations are just bad news for hardware
- Substitute some "deep computation" with hardware-friendly versions

## **Example: Aggressive Pipelining**

#### Pipelined Get-HMM/Viterbi and Transition stages



#### Pipelined non-LanguageModel and LanguageModel stages

Fetch Word	Fetch HMM/ Viterbi	Transition/ Prune/Writeback	Language Model		
	Fetch Word	Fetch HMM/ Viterbi	Transition/ Prune/Writeback		
			Fetch HMM/ Viterbi	Transition/ Prune/Writeback	

## **Example: Algorithmic Changes**

#### Acoustic-level pruning threshold

- **Software**: Use best score of *current* frame (after Viterbi on Active HMMs)
- **Silicon**: Use best score of *previous* frame (nixes big temporal bottleneck)

### Tradeoffs

Less memory bandwidth, can pipeline, little pessimistic on scores



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## Design Flow: C++ Cycle Simulator $\rightarrow$ Verilog

- Our benchmark: 5K-word "Wall Street Journal" task
- Cycle sim results:
  - No accuracy loss; not quite 2X @ 125MHz ASIC clock
  - ▼ Backend search needs: ~1.5MB SRAM, ~30MB DRAM

Recognizer Engine	Word Error Rate (%)	Clock (GHz)	Speedup Over Real Time (bigger is better)
Software: Sphinx 3.3 (fast decoder)	7.32%	1 GHz	0.74X
Software: Sphinx 4 (single CPU)	6.97%	1 GHz	0.82X
Software: Sphinx 4 (dual CPU)	6.97%	1 GHz	1.05X
Software: Sphinx 3.0 (single CPU)	6.707%	2.8 GHz	0.59X
Hardware: Our Proposed Recognizer	6.725%	0.125 GHz	1.67X



## Aside: Bit-Level Verification Hurts (A Lot)

- Common source of designer headache for silicon designs that handle large media streams
  - ◄ Generating these sort of tradeoff curves: CPU days → weeks Speedup Vs Frames (330 WSJ Utterances)



## Aside: Pieces of Design = Great Class Projects

 CMU student team: Patrick Chiu, David Fu, Mark McCartney, Ajay Panagariya, Chris Thomas



Area	11.16 mm <sup>2</sup> core / 16.09 mm <sup>2</sup> chip			
Effective Utilization	53.32%			
Cell Rows	657			
Cells	67354			
Pins	225358			
IO Pins	94			
Nets	79382			
Avg. Pins/Net	2.84			
Nets				
(Internal)	77977			
(External)	94			
Connections				
(Internal)	146621			
(External)	188			
Total net length	6.00 m			
(X)	2.59 m			
(Y)	3.40 m			
Power Supply	1.98 V			
Average Power	19.8 mW			
(switching)	11.78 mW			
(internal)	7.98 mW			
(leakage)	0.036 mw			
Power by clock domain				
Frontend	2.018 mW			
Gaussian	14.25 mW			
DRAM	2.57 mW			
Unclocked	0.96 mW			
Power by cell category				
Core	19.5 mW			
Block	0.29 mW			
IO	0 mW			
Worst IR drop	0.012 V			
<b>Final State</b>				
rinai Siais				

Slide 42

## A Complete Live Recognizer: FPGA Demo



In any "system design" research, you reach a point where you just want to see it work – *for real* 

Goal: Full recognizer 1 FPGA + 1 DRAM

- A benchmark that fits on chip
  - **1000-word** "Resource Mgt" task
  - Slightly simplified: no tri-grams
  - ◄ Slower: not real time, ~2.3X slower
  - Resource limited: slices, mem bandwidth

## System Block Diagram



## **FPGA Experimental Results**

Aside: as far as we know, this is the most complex recognizer architecture ever fully mapped into a running hardware-only form



## Performance

- Benchmark: 1K-word "Resource Management" task
- Results:
  - No accuracy loss
  - ~ 2x slower than real-time, but ~30X slower clock frequency
  - Limited by DRAM access time and available FPGA resources.

Recognizer Engine	Word Error Rate (%)	Clock (GHz)	Speedup Over Real Time (bigger is better)	<b>Efficiency</b> (Speedup/GHz)
Software: CMU Sphinx 3.0 (single CPU)	10.88%	2.8 GHz	3.7X	1.32
Hardware: Our FPGA Recognizer	10.9%	0.05 GHz	0.5X	10

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## Aside: How To Tell You're Doing Something Cool...



## Summary

#### Software is too constraining for speech recognition

- Evolution of graphics chips suggests alternative: Do it in silicon
- Compelling performance and power reasons for silicon speech recog

#### Several "*in silico vox*" architectures in design

- Custom silicon and FPGA versions
- ~10X realtime and low-power mobile architectures in progress at CMU

#### Reflections

Some of the most interesting experiences happen when you get people from very different backgrounds – silicon + speech – on same team

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