Carnegie Mellon University
Department of Electrical and Computer Engineering

18-100                                                                  Spring 2002

Introducton to Electrical and Computer Engineering

Course Syllabus

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Course Web Page and Bboard

Primary Course Web Page:  http://www.ece.cmu.edu/~ee100

We will also have a Blackboard web page for this course. Although the above web page will be the primary page, you should check the Blackboard page regularly as well, as certain things like announcements, email to the full class, etc. are more easily done on the Blackboard. Go to www.cmu.edu/blackboard. Log in and look for the S02-Introduction to ECE page.

Students are responsible for any information conveyed via announcements made in lecture (regardless of whether you attended that day or not!) and/or on the course web pages.
Textbook

Introduction to Electrical and Computer Engineering, 2nd edition, by L. Richard Carley and Pradeep Khosla

Lab Manual

Accompanying GPS Lab Manual for the text

Course Meeting Info:

Lectures:

Tuesday and Thursday, 3:00 pm – 4:20 pm, PH 100

Recitations and labs:

You can attend any recitation that you like, but you **MUST** go to your assigned Laboratory Section!

Section A:  Lab T  6:30 - 9:20 pm, HH A101  Recitation M 11:30 am - 12:20 pm, SH 324
Section B:  Lab W 1:30 - 4:20 pm, HH A101  Recitation M 12:30 pm - 1:20 pm, SH 324
Section C:  Lab W 6:30 - 9:20 pm, HH A101  Recitation M  2:30 pm - 3:20 pm, SH 324
Section D:  Lab R 6:30 - 9:20 pm, HH A101  Recitation M  3:30 pm - 4:20 pm, OSC 203

Homework:

Doing homework is integral to understanding the course material. Please take the time to do your homework each week. It is weighted fairly high in this course (equivalent to the weight of one exam) to encourage you to work on it. Exams will be difficult if you haven't worked the homework problems. Weekly problem sets will be available on the web page (primarily) on Tuesday's and will be due at the beginning of lecture on the following Tuesday. **No late homework will be accepted** (a "late" homework is one that is turned in more than 10 minutes after the scheduled beginning of lecture on the due date), as solutions will be posted to the web page the day the set is due. Please don't ask me to accept homework at the end of class, or if your friend forgot to turn yours in, or you didn't get back from break on time, etc.

Graded homework will be placed in folders by Lab Section in the 18-100 file cabinet near the secretary's office within one week of the date they are turned in. Please show some respect for your classmates by not shifting around the contents of the folders and making a mess out of the cabinet. It is not the secretary's job to straighten out this cabinet, so if it gets disorganized, you have only your classmates to blame. Requests to re-grade homework must be made to the instructor (Tom) within two weeks of the turn-in date for the homework (this gives you at least a week after it is placed in the cabinet to get it re-graded). Any homework turned in for a re-grade is subject to having the entire set re-graded (which could potentially result in a lower score on the set if we find overlooked mistakes).
Exam Dates:

Three 80-minute exams will be given during the lecture periods on the following dates, please reserve them in your schedule!:

Thursday, February 14
Thursday, March 21
Thursday, April 25

There will also be a comprehensive 3-hour final examination given during the final examination period.

Laboratory:

Each week you will meet in the lab and perform an experiment in which you will construct, analyze, and test another sub-circuit for your GPS receiver. Groups will work in pairs in the lab. Each student (not each group) must keep a lab notebook where results of experiments must be kept neatly and legibly. Your grade for the lab may be effected by your ability to produce data and explanations of results at any time by your lab teaching assistant.

Your lab grade will consist of three components:

1) A pre-lab write-up due at the beginning of lab which consists of an outline of the laboratory exercise(s) that you are to perform in the lab that day and drawings of any circuits you are to build and test. This must be completed by each lab member and you will be graded individually on this work.

2) A proto-board that you have wired prior to coming to lab with the circuits that you will test that day in the lab. As there only needs to be one proto-board per group, this will be graded on a per-group basis and both group members will receive the same score for this component.

3) A post-lab quiz that will be given to each group member individually.

You must attend lab to pass the course. Failure to attend a lab session will result in a score of zero for the lab that week. Missing lab twice will result in failing the course.

A separate document outlining what will be required of you for the laboratory portion of this course will be available on the web page prior to the first lab session.

A laboratory schedule is available at the end of this syllabus.
**Course Grading:**

Your grade will be calculated using the following two methods (both yield a total score of 100%). The highest score of the two will be used to assign your final grade.

<table>
<thead>
<tr>
<th>Method A</th>
<th>Method B</th>
</tr>
</thead>
<tbody>
<tr>
<td>16% Homework</td>
<td>16% Homework</td>
</tr>
<tr>
<td>(lowest score dropped)</td>
<td>(lowest score dropped)</td>
</tr>
<tr>
<td>20% Lab</td>
<td>20% Lab</td>
</tr>
<tr>
<td>(lowest score dropped)</td>
<td></td>
</tr>
<tr>
<td>32% Exams</td>
<td>48% Exams</td>
</tr>
<tr>
<td>(lowest score dropped)</td>
<td>(all exams included)</td>
</tr>
<tr>
<td>32% Final Exam</td>
<td>16% Final Exam</td>
</tr>
<tr>
<td>(weighted as two exams)</td>
<td>(weighted as one exam)</td>
</tr>
</tbody>
</table>

While lower cutoffs may be used, the following cutoffs are guaranteed:

- >90 A
- >80 B
- >70 C
- >60 D

**Exam Taking and Grading Policy(s)**

All exams are to be taken during the scheduled exam date and time. Make-up exams are highly discouraged and will only be given in cases of severe illness or emergency. Not feeling well the day of the exam is **NOT** a cause for an exam make-up. We build in the ability to drop an exam in the course grading for just such an occasion. It is up to you to determine if you are up to taking the exam and doing the best you can, or just accepting a zero as a drop score.

If you are unable to take an exam at the scheduled time (for a valid reason), you must contact the instructor (Tom) **immediately** to schedule a make-up exam, else you will receive a zero for that exam. Make-ups will be given at the convenience of the instructor and will generally be more difficult than the originally scheduled exam. The format of the make-up exam is up to the instructor.

The Final Exam will not be rescheduled under any circumstances. Anyone failing to take the final exam will either receive a grade of zero for that exam, or, if an emergency situation caused the exam to be missed, an incomplete will be given for the course and you may take the final at the regularly scheduled time the next time the course is offered. This score will then be used to compute your final grade for the course.

If you have special circumstances approved by the Disabled Student Services office, it is up to you to make arrangements with the instructor (Tom) **at least** 72 hours before the scheduled exam time. Failure to do so will result in you taking the exam in the same place and at the same time (and for the same length of time) as the rest of the class. It is your responsibility to remind the instructor (Tom) before every exam and to be proactive in obtaining your special circumstances.
Cheating:

Any student caught cheating in this course (on any aspect of the course...homework, labs, exams, etc.) will receive an R and the facts of the case and the penalty will be reported to the Dean of Student Affairs. While students may work in groups to discuss homework assignments, copying from someone else’s homework, lab write-up, or exam or allowing another student to copy his/her work, will be considered as cheating. Please refer to the Carnegie Mellon University Student Handbook for the University policy on cheating.
**Topics in order of course coverage and tentative course schedule**

Week 1:
Tuesday: Introduction, discussion of engineering systems and sub-systems  
Thursday: Introduction to communications and GPS, Lab overview

Week 2:
Tuesday: Basic electricity, voltage, current, resistance, power, circuit schematic symbols  
Thursday: Power dissipation, Ohm's law

Week 3:
Tuesday: Kirchoff’s Voltage and Current Laws, introduction to Nodal Analysis  
Thursday: Problem solving using Nodal Analysis

Week 4:
Tuesday: Series and parallel resistances and combinations, solving circuits using equivalent resistances  
Thursday: Thevenin and Norton Equivalents, Superposition

Week 5:
Tuesday: Review for Exam I  
Thursday February 14: Exam I: Chapters 1-4

Week 6:
Tuesday: Introduction to Operational Amplifiers, open and closed loop gain, op-amp assumptions, inverting amplifier circuit.  
Thursday: Non-inverting op-amp circuit, summing circuit, difference circuit, comparator

Week 7:
Tuesday: Introduction to diodes, basic diode operation, piecewise linear model (PWL) for diodes  
Thursday: Solving diode circuits with one or more diodes

Week 8:
Tuesday: Introduction to transistors, basic transistor operation, piecewise linear model for NPN transistors, common emitter transistor circuit.  
Thursday March 7: No class, mid-semester break.

Week 9:
Tuesday: Transistor circuits: Common collector circuit, common base circuit, circuits with both emitter and collector resistors, biasing.  
Thursday: Transistor circuits: loads on transistor circuits, Darlington pairs, PNP transistors

Week 10:
Tuesday: Review for Exam II  
Thursday March 21: Exam II: Chapters 5-8
Week 11:
Tuesday: Transistors in digital logic circuits, inverters, noise margins, fan out
Thursday: Capacitors, sketching charging and discharging capacitor waveforms, time constant

April 1-5 Spring Break, No class.

Week 12:
Tuesday: Introduction to digital circuits, Boolean algebra, Boolean expressions, DeMorgan's theorems, logic gates
Thursday: Combinational logic circuits, truth tables, digital circuit schematics, two-level circuit representation

Week 13:
Tuesday: Karnaugh maps, feedback in logic circuits, SR flip-flops
Thursday: D flip-flops, master-slave edge-triggered flip-flops, begin sequential logic

Week 14:
Tuesday: Review for Exam III.
Thursday April 25: Exam III: Chapters 9-11, Appendix A

Week 15:
Tuesday: more sequential logic, state diagrams, state transition tables, design of counters
Thursday: Output mapping, sequential logic circuits with external inputs, course wrap-up.

Laboratory schedule:

Week 1: no lab
Week 2: Section D (Thursday lab) Lab 1, no lab for all others.
Week 3: Lab 1 (all others), Section D Lab 2
Week 4: Lab 2 (all others), Section D Lab 3
Week 5: Lab 3 (all others), Section D Lab 4
Week 6: Lab 4 (all others), Section D Lab 5
Week 7: Lab 5 (all others), Section D Lab 6
Week 8: Lab 6 (all others) Section D doesn't meet, mid-semester break on Thursday, March 7.
Week 9: Lab 7 all sections
Week 10: Lab 8 all sections
Week 11: Lab 9 all sections
Week 12: Lab 10 all sections
Week 13: No labs this week. Carnival on Thursday...take a break.
Week 14: Lab 11 all sections
Week 15: Lab 12 (sectional GPS competitions)

The final GPS competition (top winners from each sections will compete for big prizes!) will be held on Reading Day, Wednesday, May 8, at noon. Place TBA.