Overview of Digital Integrated Circuits

Fall 2003  18-322

Objectives

• Design a Digital IC of small complexity (several thousand transistors) from behavioral/algorithmic level to circuit and layout level
  – optimize logic for performance or power
  – optimize layout for compactness and performance
• Analyze Digital IC at behavioral, structural, and circuit level
  – Active devices and parasitics
• Learn efficient hand analysis techniques to analyze digital IC timing performance including parasitics
• Size transistors to optimize performance or power
Introduction to CMOS Circuits

• Digital Systems
• Transistors
• Logic Design with Switches

Basic CMOS Design

• MOSFETs as switches
  – Ideal switches & Boolean operations

• CMOS logic gates
  – Basic/complex functions

• Transmission gates
  – Pass transistors
Intro to CMOS Processes II

- Generic Complimentary Metal-Oxide-Semiconductor (CMOS) Process:
  - Processing steps
  - N-well process flow
  - Lithographic masks
  - 3-D structures

MOSFET & SPICE Models

- MOSFET Structure
- MOSFET Operation
- I-V Characteristic
- SPICE Model:
  - Diode
  - MOSFET
Layout Design

- **Physical Structure of IC’s**
  - Design rules
  - Basic gates layout
- **Stick Diagrams**
  - Basic rules
  - Examples
- **CADENCE (Virtuoso)**

Layout Design II

- Handout: Virtuoso
- Design Verification
  - DRC: Design Rule Check
  - LVS: Layout versus Schmatic
- Design in the large…
  - How do designers design ICs now
## Transistor sizing
The logical effort

- Static CMOS circuit design
  - Transistor sizing
    - For symmetrical response
    - For performance
  - Large Fanin gates
  - Chains of Fanin gates
- Logical effort introduction

## Interconnect (1)

- Interconnect parameters
  - Capacitance
  - Resistance
    - Inductance
- Electrical wire models
  - Lumped RC model
  - Elmore delay
Sequential Logic

• The third dimension: Sequential systems
  – Memory function
    • Static (positive feedback)
    • Dynamic
  – Memory elements
    • Latches
    • Flip-flops

Timing Issues and Clock Distribution

• Timing issues & clock distribution
  – System Performance Determination
  – Pipelining
  – Clock skew. Register timing
  – Counter clock skew
RTL Design

- Design Automation
- RTL Design

Interconnect II

- Electrical wire models
  - Lumped RC model
  - Distributed rc line
- Designing gates for performance
  - Progressive sizing
  - Input re-ordering
- Driving large capacitances
  - Buffering techniques
- Addressing Coupling Capacitance, Resistance, and Inductance
CMOS Power Consumption

- Low-power design
  - Motivation
  - Sources of power dissipation in CMOS
  - Power modeling
  - Optimization Techniques (a survey)

Alternative CMOS Design Styles

- Pass-Transistor Logic
- Pseudo n-MOS Logic
- Cascade Voltage Switch Logic
- Dynamic CMOS Logic
- CMOS Domino Logic
Intro to CMOS Process I

• IC Manufacturing Process Steps:
  – Lithography
  – Oxidation
  – Deposition
  – Epitaxy
  – Wet Etching
  – Dry Etching
  – Diffusion
  – Ion Implantation

Intro to CMOS Processes II

• Generic Complimentary Metal-Oxide-Semiconductor (CMOS) Process:

  • Processing steps
  • N-well process flow
  • Lithographic masks
  • 3-D structures
PN Junctions and Diodes

- Operation Principle
- I-V Characteristics

MOSFET & SPICE Models

- MOSFET Structure
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- SPICE Model:
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CMOS Inverter: VTC and Delay

- Ideal Inverter
- MOS Transistors’ Characteristics
- Simplest Inverter DC Characteristic
- Noise Margins
- CMOS Inverter Switching

CMOS Gates: Sizing and Delay

- Load Capacitance
- Fall and rise time analysis
- Analytical models
- Propagation delay analysis
- Fall and rise time formulas
- Transistor sizing
- Multi-input gates
Layouts: The Good, the Bad, and the Ugly

- Compact
  - Less capacitance
  - Less bigness
- Uniform
  - Cell Height
  - Plan to abut cells to neighboring cells
- Structured
  - Layers can have “functions”
  - Layers can have “directions”

Beyond the Basic Gates

- How to make larger blocks
  - Rotating/mirroring cells
  - Abutment & Power/ground rails
  - Substrate contacts
- Floorplanning
  - Routing channels
  - Block porosity
  - Metal layer allocation
- Buffering
  - Large Loads
  - Long Lines
  - Folding Transistors
Bipolar Junction Transistor

- NPN Cross-section and Masks
- BJT Notation
- Hand Analysis Models
- NPN Modes of Operation
- Ebers - Moll Model
- BJT Inverter

Emitter Coupled Logic

- ECL Inverter
- Voltage Transfer Characteristics
- ECL NOR Gate
<table>
<thead>
<tr>
<th>Memory I: Read Only Memory (ROM)</th>
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<tr>
<td>• Random Access Memories</td>
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<td>• ROMs:</td>
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<tr>
<td>– ROM</td>
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<tr>
<td>– Decoders</td>
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<td>– EEPROM</td>
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<td>• CMOS Static Memory</td>
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<td>– Memory architecture</td>
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<td>– Read/Write circuitry</td>
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<td>• RMOS Static Memory</td>
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<td>– Four transistor memory cell</td>
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<tr>
<td>– Technology</td>
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<td>– Memory cell layout</td>
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Memory III: Dynamic Random Access

• Memory Classification
• DRAM Basics
  – Single transistor memory cell
  – Memory architecture
• DRAM Circuitry
  – Read/refresh operation
  – Charge sharing
  – DRAM design trends/limitations

VLSI Testing

• Manufacturing is imperfect
  – No. of good chips on wafer/total No. of chips
  – Yield (Y) depends on technology, chip area and layout
    • Y decreases as the area of chip is increased
    • Defect density (D)
      – Modern technologies yield a value of 1-5 defects/cm²
      – Yield starts out low (~10%) moves up (95%)
• High quality expectation
  – The earlier you detect a fault, the cheaper it is to fix
VLSI Design Flow/Trends

• Questions for:
  • What kind of company are you?
  • What product do you make?
  • How do you design and fab product?
• Three design strategies
  • Full-custom, Semi-custom, Structure ASICs, Programmable Logic
• The Productivity Gap

Future Trends in VLSI/ULSI Technology

• Trends in Semiconductor Manufacturing
• Technology Status and Roadmap
• VLSIC Yield
• Design for Manufacturability
Final Exam

Extremely Likely:
- Transistor level circuit diagram and stick diagram from logic function for any design style
- Cross-sections and circuit/logic extraction from layout
- Path delay with transistor sizing
- Interconnect delay evaluation – Elmore delay
- Sequential circuit analysis: timing and power
- BJT gate hand analysis

Very Likely:
- VTC for CMOS gates