Emitter Coupled Logic & BiCMOS
Emitter Coupled Logic

- ECL Inverter
- Voltage Transfer Characteristics
- ECL NOR Gate
ECL

• **Ultra-high speed (GHz performance)**
  – All fabled supercomputers used ECL
    • CRAY
    • NEC, Fujitsu
• **Lower device count per gate than TTL**
• **Symmetric noise margins**
• **Low noise sources**
The Differential Pair

- Vref: Reference Voltage
- Symmetric Design:
  - Transistors, Resistors, Voltage Supplies
Differential Pair

\[ I_c = \beta I_s \left( e^{\frac{V_{BE}}{\Phi_T}} - 1 \right) \]

\[ \frac{I_{c1}}{I_{c2}} = \frac{\left( e^{\frac{V_{in}-V_x}{\Phi_T}} - 1 \right)}{\left( e^{\frac{V_{ref}-V_x}{\Phi_T}} - 1 \right)} \]

\[ \approx e^{\frac{V_{in}-V_{ref}}{\Phi_T}} \]

\[ \Phi_T = 26\text{mV} \]

Vin - Vref = 60mV -> 10x change
Vin - Vref = 120mV -> 100x change!
Logic Levels

Assume Vin “high”

Output Levels:
\[ V_{out1} = V_{cc} - I_{EE} R_C \quad (V_{OL}) \]
\[ V_{out2} = V_{cc} \quad (V_{OH}) \]

Input Levels:
\[ V_{IL} = V_{ref} - 120\text{mV} \]
\[ V_{OL} = V_{ref} + 120\text{mV} \]
Differential Pair Characteristics

- **Differential Outputs**
  - No time differential between complements
- **Steep Transition region**
  - 240 mV!
  - Centered around Vref
- **Constant Current Drawn**
  - High static power dissipation
- **No Saturation Mode**
Output Stage

- **Problem:** Output Loading Sensitivity
- **Problem:** Logic Level Alignment
- **Solution:** Output stage (emitter-follower)
Logic Levels and VTC

Vcc=5V
300Ω
300Ω
Vout2
Vout1

VEE=0V
Vref
Vx
0V

IEE=3mA
1.5kΩ
1.5kΩ

0V
0V
Logic Levels

Assume Vin >> Vref

\[
\text{Vout}_1 = 1.5k\Omega \cdot (\beta + 1) \cdot I_{B1} \\
300\Omega \cdot (I_{B1} + 3mA) + .7V + \text{Vout}_1 = 5V
\]

\[
\text{Vout}_1 = (V_{OL})
\]

\[
\text{Vout}_2 = 1.5k\Omega \cdot (\beta + 1) \cdot I_{B2} \\
300\Omega \cdot I_{B2} + .7V + \text{Vout}_2 = 5V
\]

\[
\text{Vout}_2 = (V_{OH})
\]
Choosing $V_{\text{ref}}$

To Maximize Noise Margins:

Choose $V_{\text{ref}}$ mid-way between $V_{\text{OL}}$ and $V_{\text{OH}}$.

$V_{\text{ref}} = (V_{\text{OL}} \text{ and } V_{\text{OH}}) / 2 = \quad$
Voltage Transfer Characteristic

![VTC ECL Inverter Graph]
Current Source

In reality, usually a resistor:

$Q_1$ CAN saturate with high $Vin$!
**Current Source Resistor**

\[
I_C = I_E = \frac{(V_{in} - .7V)}{1.2k\Omega}
\]

\[
V_{out} = 4.825V - .25V_{in}
\]

Saturation:

\[
300\Omega \cdot I_C + 1.3k\Omega \cdot I_E = 4.9V
\]
ECL OR-NOR Gate

Is this logically adequate?
Wired-Or Logic

If any base voltage is high, the net is high

What happens if more than one base is high?
Wired-OR

- Construct large input gates
- In negative logic, Wired-AND
ECL Fanout

\[(\beta+1) I_B = 3mA \frac{N}{(\beta+1)} + V_{out}/1.5k\Omega\]
\[300\Omega I_B + .7V + V_{out} = 5V\]

- When does $V_{out} = V_{IH}$?
  - Typical values $\approx 30$
Negative Supply Voltage

- Noise on VCC shows up on signal nets
- VEE much more noise tolerant.
  - Common mode noise to Vin, Vref, etc
- Output shorted to ground

\[ \text{Vcc=5V} \]

\[ 1.5 \text{kΩ} \]

\[ 0V \]
Power Dissipation

• **Dynamic Power:**
  – 10% of the voltage swing of CMOS
    • 100x less power

• **Static Power:**
  – All gates consume static power
    • $3\,\text{mA} \times 5\,\text{V} = 15\,\text{mW}$!

• **High Power**

• **Low noise**
BiCMOS

- Introduction
- System Requirements
- Circuit Technology
- Device Technology
- Process Technology
- Manufacturing Issues
- BiCMOS Projections
INTRODUCTION

BiCMOS Advantages:
- Improved speed & robustness over CMOS
- Lower power dissipation than bipolar
- Flexible I/O’s
- Higher performance analog IC’s
- Latchup robustness

BiCMOS Disadvantages:
- Higher costs
- Longer fabrication cycle time
BiCMOS Role

For μP:

° Reduced delays through critical paths
° Reduced clock skews
° Increased I/O throughput
° Larger, faster on-chip memory
BiCMOS Inverter #1

\[ V_{OH} = V_{CC} - V_{be(on)} \]
\[ V_{OL} = V_{SS} + V_{ce(sat)} \]
BiCMOS Inverter #2

\[ V_{OH} = V_{CC} \quad V_{OL} = V_{SS} \]
BiCMOS NAND Gate

\[ V_{CC} = 5 \text{ V} \]

A

B

NPN

N1

N2

N3

P1

P2

V_{out}

NPN1

NPN2
BiCMOS DEVICES

BJT in p-well CMOS process
BiCMOS Technology
Manufacturing Issues

Main disadvantage of BiCMOS: COST

Cost adders:

° manufacturing cycle time

° defect density

° process control

° design verification