Distinguished Seminar
Thursday, March 25th
Scaife Hall Auditorium
Room 125
4:30 p.m.
Refreshments at 4:00 p.m.

Janak H. Patel
Professor
Electrical & Computer Engineering Department
University of Illinois at Urbana-Champaign

Janak H. Patel is a Research Professor in Coordinated Science Laboratory and Department of Electrical and Computer Engineering at University of Illinois at Urbana-Champaign.

Patel’s research contributions include Pipeline Scheduling, Cache Coherence, Cache Simulation, Interconnection Networks, On-line Error Detection, Reliability analysis of memories with ECC and scrubbing, Design for Testability, Built-In Self-Test, Fault Simulation and Automatic Test Generation. Patel has supervised over 85 M.S. and Ph.D. theses and published over 200 technical papers and listed as a Highly Cited Researcher. He was a founding technical advisor to Nexgen Microsystems that gave rise to the entire line of microprocessors from AMD. He was a founder of successful startup, Sunrise Test, a CAD company for chip testing, now owned by Synopsys.

He received a Bachelor of Science degree in Physics from Gujarat University, India and Bachelor of Technology in Electrical Engineering from the Indian Institute of Technology, Madras, India, and a Master of Science and Ph.D. in Electrical Engineering from Stanford University. He is a fellow of ACM and IEEE and a recipient of the 1998 IEEE Piore Award.

CMOS Process Variations:
A "Critical Operation Point" hypothesis

A brief overview of present and future CMOS process variations will be presented. Prevailing understanding of a chip’s behavior under large process variations with statistical delay assumptions leads one to conclude that a small number of errors are likely as we progress further down on Moore’s Law. This understanding is challenged by a new hypothesis on the behavior of very large CMOS chips in the presence of process variations. A Thought Experiment is presented which leads to the new hypothesis. The new hypothesis states that in every large CMOS chip, there exist critical operations points (frequency, voltage, temperature) such that it divides the 3-D space (F, V, T) into two distinct spaces: 1. Error-free operation and 2. Massive errors (i.e. completely inoperable). Two attempts at disproving this hypothesis with real physical experiments will be described. Some consequences of the hypothesis on power savings in large data centers are also suggested.

ECE Seminar Hosts
Jeyanandh Paramesh
paramesh@ece.cmu.edu
Onur Mutlu
onur@cmu.edu
Gabriela Hug
ghug@ece.cmu.edu