FET Amplifiers

\[ V_{GS} = 5v \]

\[ V_{DS} \]

\[ V_T0 = 1.0V \]
\[ K_p = 2e-5 \ [A/V^2] \]
\[ W = 100 \text{ microns} \]
\[ L = 10 \text{ microns} \]
FET Amplifiers

- A 200mv peak ac input voltage will cause more than a 1v peak ac output voltage
- What would we change to make the voltage gain even larger?

\[ V_{GS} = 5\text{V} \]

\[ v_{gs} \]

\[ R_D = 6.6k\Omega \]

\[ V_{DS} = V_{DD} - R_D i_D \]

\[ \sim 2\text{V} \]
dc Solution of FET Amplifier

- Set the ac source to zero and analyze the dc bias point
- Solution should agree with that from load line approximation

IDS1 = 1.919 mA
VGS1 = 5V
L = 10E-6
W = 100E-6
VD = 7.335 V
RC = 6.6k
VDD = 20V
dc Solution of FET Amplifier

- Response for a 5kHz, 0.2v peak ac input signal
dc Solution of FET Amplifier

- The output signal is somewhat distorted for a 0.4v peak ac input
Small Signal Assumption

- The distortion is due to the nonlinear effects when the ac $v_{gs}$ is too large:

  bias point equations:  
  \[ I_D = K(V_{GS} - V_t)^2 \quad V_D = V_{DD} - R_D I_D \]

  ac & dc equations:  
  \[ v_{GS} = V_{GS} + v_{gs} \quad i_D = K(v_{GS} - V_t)^2 \]
Transconductance -- Gain

- The transconductance, $g_m$, for a MOSFET is much smaller than that for a BJT which uses the same silicon area (BJT approx. 100 times better)

$$g_m = \frac{\partial i_D}{\partial v_{GS}} |_{v_{GS} = V_{GS}}$$
Transconductance -- Gain

- BJT $g_m$’s are independent of area dimensions
- FET $g_m$’s are dependent on channel $W$ and $L$ dimensions

\[
g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{V_{GS} = V_{GS}} = 2K(V_{GS} - V_t) = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)
\]
Small Signal Voltage Gain

\[ v_D = V_{DD} - R_D i_D = V_{DD} - R_D (I_D + i_d) \]

- Under the small signal assumption:

\[ v_d = -R_D i_d = -g_m R_D v_{gs} \]

\[ \frac{v_d}{v_{gs}} = -g_m R_D \]
The small signal model is very similar to that for the BJT amplifier:

- **$r_o$** is the drain-source voltage change with change in $i_{ds}$ due to channel length modulation.
Channel Length Modulation

- Given lambda and the bias point, we can calculate $r_o$.
- For our example, we can estimate $r_o$ from an enlarged view of $I_{DS}$ vs. $V_{DS}$ at the bias point (with $V_{GS}=5\text{v}$).
Small Signal Model

- Short the dc supplies and analyze the small signal equivalent ckt:

\[ V_{GS} = 5v \]

\[ v_{gs} \]

\[ 20v \]

\[ 6.6k\Omega \]

\[ g_m \]

\[ v_{gs} \]

\[ 28k \]

\[ 6.6k \]
Biasing

- Since $I_D$ determines $g_m$ we’d like to bias the transistor so that the small signal gain remains as stable as possible with variations in temperature and process.

$$V_{GG} = V_{DD}\frac{R_{G2}}{R_{G1} + R_{G2}}$$
Negative Feedback Resistor

- $R_S$ provides negative feedback for unwanted changes in $I_{DS}$ due to process variations or temperature fluctuations.
Negative Feedback Resistor

- We can get a similar negative feedback effect with a drain to gate bias resistor
- This resistor guarantees that the transistor is biased in the saturation region -- why?

Find the $R_D$ which establishes a 1mA $I_D$

$K=0.25\text{mA/V}^2$ \hspace{1cm} $V_{DD}=20\text{V}$ \hspace{1cm} $V_t = 2\text{V}$
No negative Feedback Resistor

• What is the change in $I_D$ for the circuit below if the threshold voltage changes from 2V to 3V?

![Circuit Diagram]

$V_{GS} = 4V$

$20\text{v}$

$16k\Omega$
Negative Feedback Resistor

- But this change is much less with negative feedback control