A popular book on parallel processing is “Culler and Singh. *Parallel Computer Architecture: A Hardware/Software Approach.* Morgan Kaufmann, 1999” from which we will draw some background on regular, parallel architectures in later lectures. After talking about existing technology and trends over 934 pages of text, on page 935, in the “Future Directions” chapter, the authors admit that networking technology, memory technology and processor design are “thrown up for grabs” when seriously considering what to do with a billion transistors on a chip.

Admittedly that was 1999. But are things so very different? That is for you to decide through investigation, formulation and just plain thinking. This can be one of those annoying exercises because it seems so open-ended — or it can be a lot of fun because it asks you to think for yourself. Whether it is more about fun or pain has a lot to do with your perspective.

Clearly it is important to get used to making your own predictions as to where things are likely to go if you are going to make effective career choices! We will grade you on how well you make your arguments: how your research is, how you think out the arguments, and distill them down to a few key points that you can support.

1. (25%) Do a literature search to find out what others have to say about this. Is there a popular, widely accepted view of when single chip designs will utilize a billion transistors, and how that level of density and complexity may change the way we organize chip designs? If so, cite several instances of where this is claimed. If not, cite different views. Either way, support what you find with citations. More points for more high-quality references.

2. (10%) In what year will a billion transistor single chip designs be commonplace for custom or semi-custom single chip designs (note this differs from custom processor design)?

3. (40%) Develop quantitative metrics used to provide perspective and justify an opinion. Have you even seen such a thing presented in a “perspective talk” at a conference? For example, the use of caches on processors was justified with a simple graph showing how memory speed was changing relative to processor speed, resulting in a break-point that changed the way we organized processors. Moore’s Law (which we all know isn’t really a law at all), graphed a set of observations about design sizes, over time. Through a set of metrics that illustrate trends, develop a single, high-level graph or set of equations that can be used to illustrate something... like competing trends. For example, you can find a set of conflicting graphs that others have published and point out a potential conflict between them, motivating the development of something new. An example of this is the need for low power design, and the need to have designs be programmable; this can result in conflicting requirements for next generation designs. Can this, or something like it, be quantified? One good place to start looking for information might be something called the “SIA roadmap.” The most useful chapter may be the “Overall Technology Roadmap...” Make sure you justify your metrics with references!

4. (15%) Use your results from #1 and #2 to justify what you think the single biggest challenge will be to the way we currently conceive of computer design as single chips start to have a billion transistors on them.
Turn in:

- a paper due at the start of class (worth 90%, as outlined above): no more than 5 pages of written text, answering the questions as stated above.

- a three powerpoint slide presentation (worth the remaining 10%) that summarizes your key arguments. You will present these during class. Please bring a laptop or use one from a friend, since our loading them on our computer turns out to be very problematic. Everyone gets to ask you questions about your presentation during class.