18-525 Project Overview

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Jike Chong

Outline

• Design Specifications
• Design Proposal
• Proposed Architecture
• Floor planning
• Testing
• Presentation Style
• Final words
Design Specifications

Hard Constraints:

- HP .35um technology
- < 100 input/output pins
- Die area: < 500,000 \( \mu \text{m}^2 \) (Largest bounding box for all layers)
- 4 Metal layers, 1 poly layer

Soft Constraints:

- 10K – 15K transistors
- Aspect ratio of less than 2:1

What’s 10K transistors?

- One bit register: ~ 20 trans
- One bit Carry Ripple Adder: ~ 25 trans
- One 32-bit register + buffering: ~ 1K trans
- One 32-bit adder: ~ 1K trans
- One 32-bit carry look-ahead adder: > 2K trans
- One 8-bit multiplier: 2-3K trans
Design Specifications

What’s 500,000 \( \mu m^2 \)?

- 500,000 \( \mu m^2 \): 
  ~ 700 x 700 \( \mu m^2 \)
- One bit register: 
  ~ 15 x 20 \( \mu m^2 \)

Design Proposal

From a big system:
- Implement a small portion, but do it really well!
  - e.g. QUARK register file

From a simple component:
- Use add-on’s to make it very useful!
  - e.g. NRD – Noise Reduction Device

From a simple algorithm:
- Make it run real fast!
  - e.g. MrTEA – 128-bit TEA encryption chip

From a group of simple functions:
- High level of integration of simple functions
  - i.e. internet VCR chip
Design Proposal

Suggestions:

• We can shoot for:
  – High performance
    • i.e. fast adders, multipliers
  – Size reduction
    • i.e. small registers, latches
  – Power efficiency
    • i.e. use gates with low power consumption
  – Integration of functions
    • i.e. internet VCR chip

• Application
  – What is the application?
  – How does your part fit in the big picture?
  – Why is this useful? (e.g. A demo: Before vs After)

• I/O assignments and definition
  – Exact pin functions:
    • Power, Gound, Clock, Select
  – Select signal fine definitions:
    • What is a “1”? What is a “0”?
Design Proposal

- Functional pins
  - VDD [x2]
  - GND [x2]
  - Reset
  - Input [7:0]
  - Output [7:0]
- Parameter pins
  (Sampled at reset)
  - Blitz Encryption (16 cycles)
  - Export Enable (international)
  (Sampled at ready state)
  - Prog/Ready
  - TEA/pass
  - Encry/decry
  - Key/delta
  - Data Ready
  - Output ready
- Emergency Pin

Logic Decision Hierarchy

- Schematic of major functional blocks
  - Major blocks:
    - adders, muxes, registers, latches
  - Control blocks can be behavioral
    - Identify “control path” vs “data path”

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Design Proposal

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- Estimate of transistor count
  - Complete estimates:
    - A table with counts that correspond to ALL block in your schematic
- Backup plan
  - If the design turns out to be too ambitious, how can it be cut down?

### Table: Transistor Count

<table>
<thead>
<tr>
<th>Part</th>
<th>Transistor Count</th>
<th>Size</th>
<th>Count</th>
<th>Total Transistors</th>
<th>Total Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-bit CLA</td>
<td>996</td>
<td>150 x 100 = 15,000</td>
<td>3</td>
<td>3,000</td>
<td>45,000</td>
</tr>
<tr>
<td>32-bit CLA/S</td>
<td>1,188</td>
<td>150 x 120 = 18,000</td>
<td>2</td>
<td>2,400</td>
<td>36,000</td>
</tr>
<tr>
<td>1-bit D-reg</td>
<td>14</td>
<td>20 x 15 = 300</td>
<td>160</td>
<td>2,240</td>
<td>48,000</td>
</tr>
<tr>
<td>1-bit D-reg (w/ clear)</td>
<td>18</td>
<td>20 x 12 = 240</td>
<td>104</td>
<td>1,872</td>
<td>24,960</td>
</tr>
<tr>
<td>1-bit XOR (2-input)</td>
<td>6</td>
<td>12 x 10 = 120</td>
<td>64</td>
<td>384</td>
<td>7,680</td>
</tr>
<tr>
<td>Muxes:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 input @ 32bit</td>
<td>128</td>
<td>6</td>
<td>768</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 input @ 32bit</td>
<td>256</td>
<td>1</td>
<td>256</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 input @ 128bit</td>
<td>512</td>
<td>1</td>
<td>512</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-bit counter</td>
<td>352</td>
<td>16 x 15 x 20 = 4,800</td>
<td>1</td>
<td>352</td>
<td>4,800</td>
</tr>
<tr>
<td>1-hot FSM register</td>
<td>154</td>
<td>8 x 15 x 20 = 2,400</td>
<td>1</td>
<td>154</td>
<td>2,400</td>
</tr>
<tr>
<td>Control logic</td>
<td>~1,000</td>
<td></td>
<td>~1,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Others</td>
<td>~1,000</td>
<td>1</td>
<td>~1,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td>13,938</td>
<td>168,840</td>
<td></td>
</tr>
</tbody>
</table>
Proposed Architecture

• Architecture Optimizations:
  – Mealy or Moore machine for control logic?
  – Pipelining data path?
  – Critical path identification
  – Critical path optimization

• Component Optimization
  – What aspect of each component to optimize for?
  – e.g. Decide to use RCA or CLA

• Update changes to schematics
• Estimate of transistor counts
  – A table with updated counts that correspond to each block in your schematic
• Functional Verilog Description
  – Full chip Verilog Description
  – Control logic defined in basic gates
Architectural Optimization

• We can optimize away entire levels of logic!
• e.g. 2-bit logarithmic carry look-ahead tree
  – We can optimize away two levels of logic by adding more levels of carry look-ahead units
Floor planning

Signal Flow is important!
- 32-bit bus in M3 will be at least 32 µm wide!
- Check maximum wire density and routability

Reserved metal layers for routing
- Ensured metal transparency for low level components
- Specify orientation for metal layers to guarantee routability

- Don’t switch layers too often – Vias are highly resistive
- Consider larger pitch and/or shielding for important buses
Circuit optimization –

**Transistor size optimization**

- experiments – experiments – experiments
  - Test out circuit components with similar drive and load conditions
  - Especially useful in predicting critical path and optimizing for the critical path

**Testing**

- Extensive initial testing to avoid delays later
- Keep Verilog, schematics, and hardcopy synchronized with layout modifications
- Set timing constraint for basic building blocks
Presentation Style

• Use MS PowerPoint 97 / 2000

• Must contain the required main points

• Concentrate on one or two highlights
  – Talk about what’s special about your solution.
  – We love to hear about
    • your experimental results
    • how you balance your tradeoffs
  – We want to be impressed !!

Final Thoughts

• 13 more days to a Functional Verilog Model

• We understand: this is an aggressive schedule!

• Why?
  – We want you to have time to take a shower before
    the final presentation…

  … you’ll look better on video !!