Post-Silicon Performance Modeling and Tuning of Analog/Mixed-Signal Circuits via Bayesian Model Fusion

(Invited Special Session Paper)

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ABSTRACT

Post-silicon tuning has recently emerged as an important technique to combat large-scale uncertainties (e.g., process variation, device modeling errors, etc) for today's nanoscale circuits. This talk presents a novel Bayesian Model Fusion (BMF) technique for efficient post-silicon performance modeling and tuning of analog and mixed-signal (AMS) circuits. The key idea is to borrow the simulation or measurement data from an early stage (e.g., pre-silicon) to accurately build AMS performance models at a late stage (e.g., post-silicon). The post-silicon models are then used to facilitate efficient tuning of AMS circuits. A circuit example designed in a commercial 32 nm CMOS process is used to demonstrate the efficacy of the proposed post-silicon performance modeling and tuning methodology based on BMF.

1. MOTIVATION

With the aggressive scaling of nanoscale IC technologies, AMS design becomes increasingly challenging, primarily due to the following reasons:

- *Increased process variation*: With the continuous shrinking of IC feature size, large-scale process variation significantly impacts the performance metrics of AMS circuits. It, in turn, becomes extremely difficult to design a robust AMS circuit that can work properly over all process corners.
- *Reduced voltage headroom*: The supply voltage of AMS circuits has been greatly reduced by more than 3× during the pass one decade. Given the reduced voltage headroom, many traditional AMS circuit topologies (e.g., cascode amplifier) cannot be easily implemented with today's IC technologies.
- *Highly integrated SOC design*: A large number of analog and digital components are fully integrated within a single die to build a complex SOC system. Therefore, unlike the traditional AMS circuits that are often implemented with a mature manufacturing process, today's AMS circuits must be designed with the digital blocks together by using an early-stage, advanced IC technology where even the device models have not been accurately characterized for AMS performance metrics (e.g., phase noise, nonlinear distortion, etc) yet.

The combination of these recent trends poses a large number of new design challenges for AMS circuits and, hence, suggests an immediate need to re-visit this area. Traditionally, AMS CAD tools mainly focus on pre-silicon modeling, simulation and optimization [1]. While these traditional CAD tools are extremely important, it becomes equally important to develop a comprehensive CAD methodology for AMS post-silicon modeling, validation and tuning. Here, the objective is to appropriately address the technical issues (e.g., device modeling error, process variation, etc) observed at the post-silicon stage by accurately building circuit performance models based on silicon measurement data to enable efficient post-silicon validation and tuning. As such, the pre-silicon design error can be corrected and the post-silicon circuit performance can be improved to meet the given specifications. In what follows, we will introduce our proposed BMF technique for post-silicon performance modeling and tuning of AMS circuits.

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2. BAYESIAN MODEL FUSION FOR POST-SILICON MODELING

The goal of post-silicon performance modeling is to approximate a given circuit performance (e.g., gain of an amplifier, phase noise of an oscillator, etc) as an analytical (e.g., linear, quadratic, etc) function of the parameters of interest based on post-silicon measurement data. Taking post-silicon tuning as an example, we want to approximate the circuit performance as a function of a set of tunable parameters for a given silicon die. Once such a post-silicon performance model is available, it can be used to quickly find the optimal values of the tunable parameters for the specific die, as will be discussed in detail in Section 3.

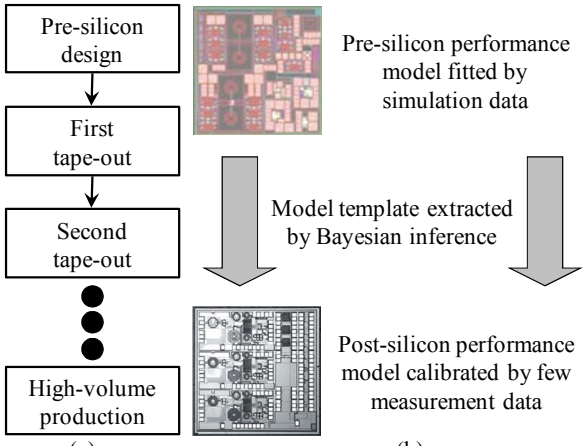

Figure 1. (a) Today's AMS design flow typically involves multiple stages. (b) A specific application example of BMF is shown to borrow pre-silicon simulation data to efficiently create post-silicon performance model.

In this talk, we will present a novel BMF technique for

efficient post-silicon modeling of AMS circuits. The key idea of BMF is to consider the AMS design flow as a multi-stage process, as shown in Figure 1(a). When such a multi-stage design flow is implemented, simulation or measurement data are generated at each stage to validate the circuit design, before moving to the next stage. Since these data collected from multiple stages come from the same circuit, they are expected to be strongly correlated. Hence, it is possible to *borrow* the data from an early stage for post-silicon performance modeling at a late stage. As such, only few post-silicon data should be measured at the late stage and, hence, the post-silicon modeling cost is substantially reduced.

Figure 1(b) shows a specific application example of BMF where the pre-silicon performance model is fitted by using simulation data. Next, a model template is statistically extracted and encoded as our *prior* knowledge based on the pre-silicon performance model. Finally, the model template is further calibrated by applying Bayesian inference [2] to very few post-silicon measurement data to accurately create the post-silicon performance model, as shown in Figure 2. In this application example, by "fusing" the pre-silicon model with the post-silicon model through Bayesian inference, the amount of required measurement data (hence, the measurement cost) for post-silicon performance modeling can be substantially reduced.

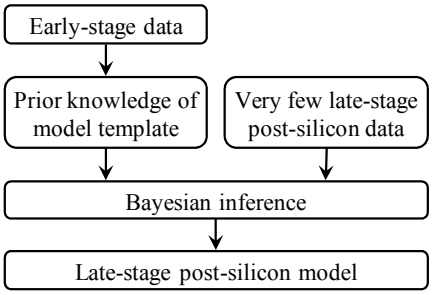

Figure 2. A simplified flow of the BMF method is summarized for late-stage post-silicon performance modeling with a small set of late-stage post-silicon measurement data.

3. POST-SILICON TUNING

Given the large-scale uncertainties (e.g., process variation, device modeling errors, etc) posed by today's advanced IC manufacturing process, it becomes extremely difficult, if not impossible, to reliably design a robust AMS circuit by following the traditional design flow to achieve first-time silicon success. Recently, adaptive post-silicon tuning has been proposed to address this design challenge [3]. The objective is not to design a fixed circuit that can guarantee to work after manufacturing. Instead, we aim to design a re-configurable AMS circuit for which a number of tunable parameters (e.g., bias current, load capacitance, etc) can be adaptively changed for a specific silicon die. By setting the optimal values for these tunable parameters based on the process corner of a specific die, the circuit functionality can be adaptively corrected and its performance metrics can be dynamically improved. From this point of view, the aforementioned post-silicon tuning offers two major benefits. First, it enables first-time silicon success and reduces the design cost. Second, it improves the parametric yield and reduces the manufacturing cost.

To make the post-silicon tuning of practical utility, one important-yet-challenging problem is how to develop an efficient post-silicon methodology to find the optimal values of tunable parameters for each individual die. Towards this goal, it is extremely important to create a post-silicon method where the circuit performance of interest is approximated as an analytical function of the tunable parameters. Note that such a function is often different from die to die. We expect that the optimal values of tunable parameters are also different for different dies. Once the post-silicon model is available, we can easily optimize the tunable parameters based on the model, instead of expensive silicon measurements. The key challenge here is how to generate the post-silicon model with a small number of silicon measurements (i.e., a small measurement cost).

In this talk, we will demonstrate that our proposed BMF technique can be used to effectively address the aforementioned modeling challenge. When applying BMF to the application of post-silicon tuning, there are two different sources of prior information that can be explored. First, when building post-silicon performance models, we can re-use the pre-silicon simulation data to extract our prior knowledge and then calibrate these models based on few post-silicon measurement data. Second, once the post-silicon performance models are fitted for a number of silicon dies, we can extract the prior knowledge from these dies and apply BMF to build the post-silicon models for other dies from the same wafer or lot. In both scenarios, we expect that by appropriately taking advantage of the prior information, the measurement cost of post-silicon performance modeling can be greatly reduced. In this talk, a circuit example designed in a commercial 32 nm CMOS process will be presented to demonstrate the efficacy of the proposed post-silicon performance moiling and tunable methodology based on BMF.

4. SUMMARY

Unlike most traditional CAD tools that focus on pre-silicon modeling, simulation and optimization, post-silicon modeling and tuning has become an important technique to address the large-scale uncertainties (e.g., process variation, device modeling errors, etc) associated with nanoscale IC technologies. In this talk, we present a novel statistical technique, referred to as Bayesian Model Fusion (BMF), to efficiently build post-silicon performance models for AMS circuits. BMF exploits the prior information extracted from an early stage (e.g., pre-silicon) to substantially reduce the modeling cost at a late stage (e.g., post-silicon). The performance models fitted by BMF are further used for efficient post-silicon tuning of AMS circuits. A circuit example designed in a commercial 32 nm CMOS process is used to demonstrate the efficacy of the proposed BMF method.

5. ACKNOWLEDGEMENTS

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