Shelley Chen

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OBJECTIVE

Full time research and development position in

- Microarchitecture development
- Performance evaluation and analysis

EDUCATION

May 2004 (Expected)
MS, Department of Electrical and Computer Engineering, Carnegie Mellon University
Thesis: MultiSMARTS: Fast and Accurate simulation of multiprocessor systems
Advisor: Babak Falsafi
GPA: 3.7/4.0

May 2002
BA, Computer Science Department, University of California, Berkeley
GPA: 3.7/4.0

AWARDS/RECOGNITION

September 2003: Semiconductor Research Corporation (SRC) Master's Scholarship Award
May 2002: Graduated with Honors, University of California, Berkeley
January 2001: Member of Upsilon Pi Epsilon (Computer Science Honor Society)
September 2000: Member of the Golden Key Honors Society

WORK/PROJECT EXPERIENCE

January 2003 – Present, Carnegie Mellon University
MultiSMARTS: Fast and Accurate Simulation of Multiprocessor Systems
Simulation time has become a bottleneck due to the great complexity of hardware systems. MultiSMARTS uses rigorous statistical sampling to produce fast and accurate measurements of multiprocessor systems. By taking measurements for a large number of small samples, we improve performance significantly without sacrificing the resulting accuracy of the measurement. This technique is applicable to a wide range of measurements, including performance analysis, power consumption, and heat dissipation. We expect the speedup of a multiprocessor system to be as good, if not better, than the 35x speedup achieved by the uniprocessor prototype.

January 2003 – May 2003, Carnegie Mellon University
Object Fusion: Co-location of keys of nodes in a tree-like structure into the same cache line.
With the traditional memory layout of tree nodes, the traversal of tree structures causes frequent cache misses. By modifying the layout of a group of nodes in the cache, only one cache access is necessary to retrieve all the keys within a group. This was implemented with the SUIF2 compiler and in the best case, resulted in a 3.6x speedup.
(class project for Compiler Optimization)

August 2002 – December 2002, Carnegie Mellon University
Dynamic Speed/Voltage scaling (DVS) for Globally Asynchronous, Locally Synchronous (GALS) processors
DVS has been a successful solution to deal with the growing power consumption associated with increased chip complexity. Unfortunately, DVS is not very effective with synchronous processors due to the significant performance degradation that results. We implemented front-end DVS in a GALS processor for balancing the front and back end stages of the pipeline. In addition, we modified the existing GALS DVS scheme in the functional units to account for inter-unit dependency issues as well as the load.
(class project for Power Aware Computing)

August 2002 – December 2002, Carnegie Mellon University
Out of Order Memory Accesses Using a Load Wait Buffer

As the disparity between processor and memory speeds increases, the Load Store Queue (LSQ) is more likely to become the bottleneck in the pipeline. We implemented a Load Wait Buffer (LWB) for holding long-latency loads to let ready-to-execute memory access instructions into the LSQ. Loads can execute out of order, but stores still execute in program order. Our simulations showed up to a 3x speedup with the implementation of the LWB.
(class project for Advanced Computer Architecture)

June 2001 – August 2001, Motorola, Elk Grove Village, IL
iMercury: Automating communication between physicians and patients through mobile devices and desktop computers
I worked with the iMercury group, which focused on designing and implementing an automated messaging application for the two-way pager (Timeport P930 and Pagewriter 2000 models), which would be geared towards efficient communication between physicians and nurses working at the hospital. During the development process, I also gained knowledge about the software production process, databases, and FLEX script, which was the development language for the two-way pager. I was in charge of the back end of the application, creating and sending XML messages to other instances of the application.
(summer internship)

June 2000 – August 2000, Sun Microsystems: Cupertino, CA
Optimizing JVM build and test tools for the Java runtime group
I worked with the runtime group, who focused on the development of the JVM. I was in charge of maintaining an in-house tool that built and tested the JVM on various platforms. In addition, I made multiple modifications to the tool, whether they be features or bug-fixes.
(summer internship)

August 1999-December 2001, University of California, Berkeley: Berkeley, CA
I was a lab assistant/grader, thus responded to various questions brought up by students in class. In addition, I assisted students in completing their assignment in C and Scheme and graded their submissions.

SELECTED COURSE LIST

Advanced Computer Architecture
Energy Aware Computing
Optimizing Compilers for Modern Architectures
Multiprocessor Architecture

PROGRAMMING LANGUAGES

C/C++, Java, VHDL, Scheme

REFERENCES

Professor Babak Falsafi
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