Electrical & Computer ENGINEERING

1st IBM Academy Conference on
Analog Design, Technology, Modeling and Tools

Design Automation for Analog: The Next Generation of Tool Challenges

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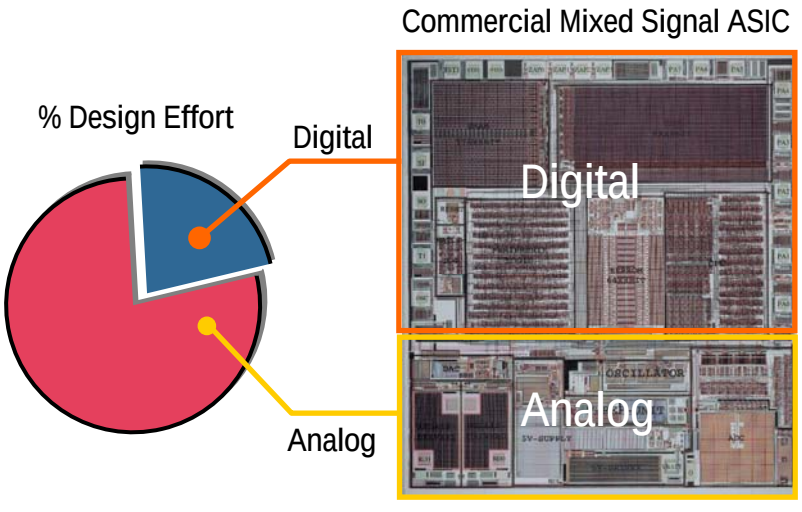
Carnegie Mellon

The Mixed-Signal Design Problem



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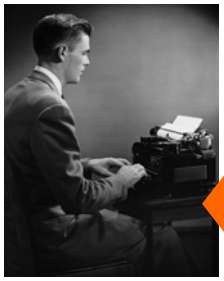
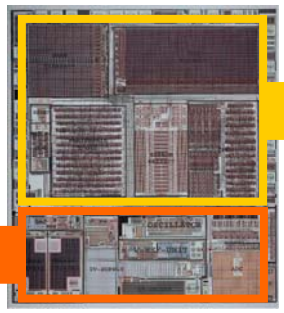
Why This Happens—Historical View





Digital Methodology
- ✓ CAD tools
- ✓ Abstraction
- ✓ Reuse & IP

Analog Methodology
- ☒ CAD tools
- ☒ Abstraction
- ☒ Reuse & IP

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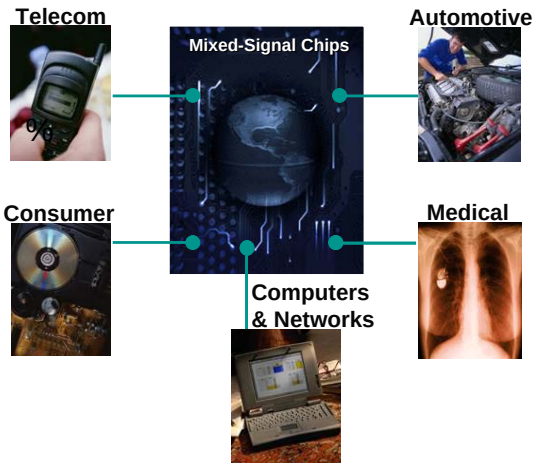
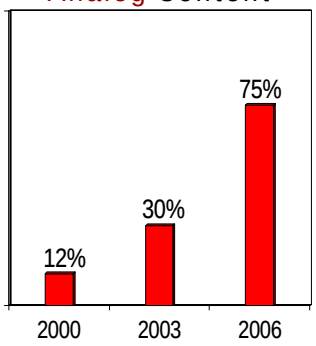
Why This Matters (I): Many "Mixed-Signal" ICs



% Digital Chips with Analog Content



[Source: IBS 2003]

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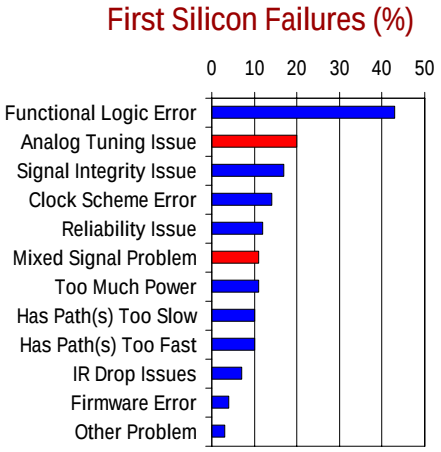
Why This Matters (II): Analog Mistakes == $$$

- How many ICs/ASICs work on first silicon? Only 39%
  - 61% of new ICs/ASICs require at least one re-spin.
  - Source: Aart de Geus, Chairman & CEO of Synopsys, 2003 Boston SNUG
- Many silicon failures are due to analog / mixed-signal design error
- This is a very expensive problem...



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The Challenges...

- *Constant* need for better tools
- Tools for productivity
- Tools for complexity
- Tools for technology (scaling)
- Tools for reuse / IP

About this Talk

- If you think this means I will talk about SPICE-like simulator stuff….
  - …you can leave now.
  - I'm not going to talk (much) about simulation *per se*
- I want to talk about *automation*: Synthesis, optimization, etc
  - Of circuits
  - Of layouts
  - Of statistics / yield
  - Of macromodels
  - Of mixed-signal systems

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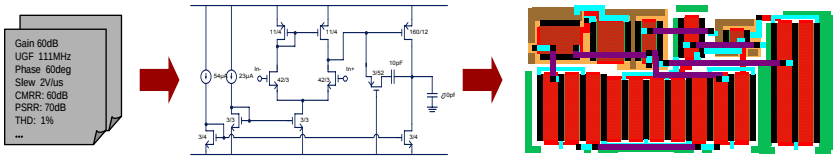
Context: Where Are We?

- Let's start with a typical analog circuit – *one cell*
  - ~5-100 devices (if bigger, usually use some hierarchy)
  - Often requires precision devices/passives for performance
  - Often requires sensitive device placement, wiring
  - Increasingly challenged by scaled digital device behaviors



Specification Circuit topology & sizing Physical layout

Need all 3 of these to finish one "complete" circuit

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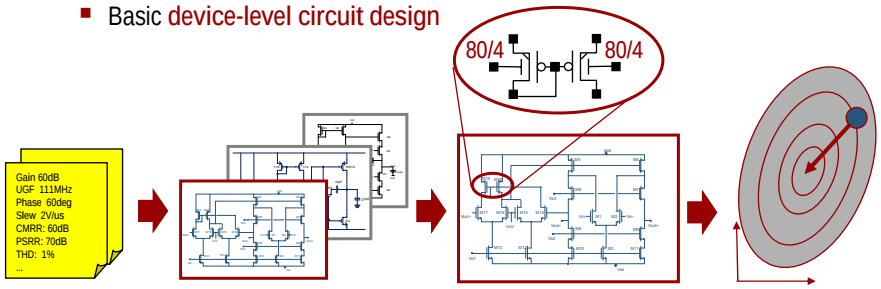
Analog Circuit Design: Sizing/Centering Tools

- No matter *how* you do it, you have to do these tasks
  - Basic device-level circuit design



Generate proper specs

Design proper circuit topology

Design proper device sizing/biasing

Optimize for centering, yield

Focus for automation / optimization

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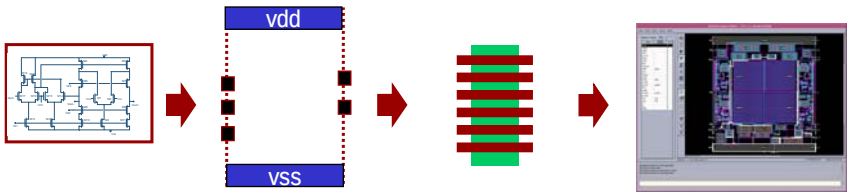
Analog Circuit Design: Layout Tools

- No matter *how* you do it, you have to do these tasks
  - Basic device-level layout design



From sized schematic

Design proper footprint power, isolation, etc

Design individual device geometries

Place/route devices, optimize area/parasitics, compact, etc.

Focus for automation / optimization

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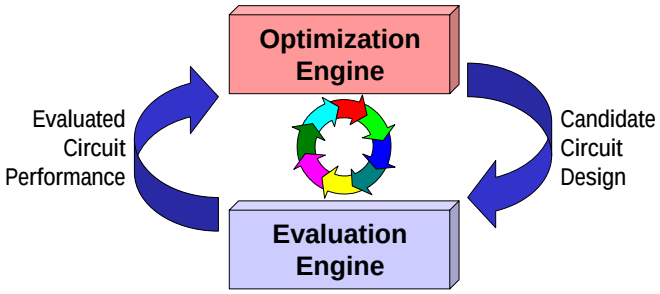
The Strategy: *Optimization-Based* Design

- All successful approaches have this overall structure



- Use some clever form of heuristic or numerical search
  - Optimization engine: proposes candidate circuit solutions
  - Evaluation engine: evaluates quality of each candidate
  - Cost-based search: cost metric represents "goodness" of design

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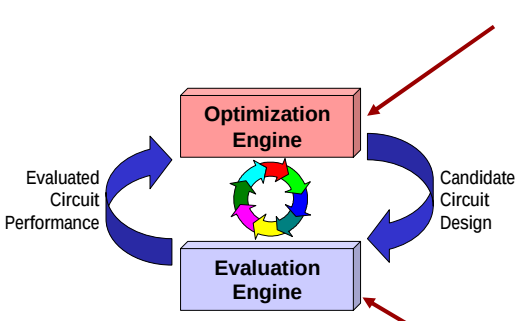
Sizing Optimization: Short Historical Tour

- Can use diagram to characterize major optimization-based ideas



What is the optimization strategy?
Who/what does optimization?
Numerical? Global? Local?
Heuristic? Serial? Parallel? ....

What is metric for evaluation?
Who/what/how is it created?
What quality? (Approx vs Sign-off)
What speed? How general? ...

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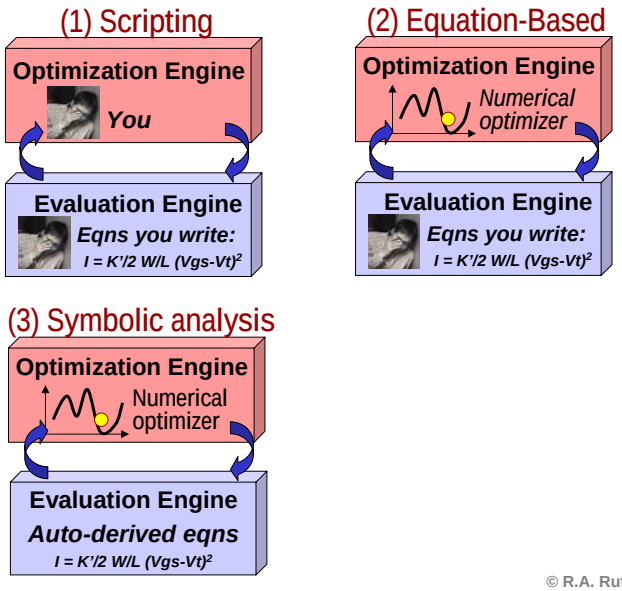
The History: Four Major Approaches



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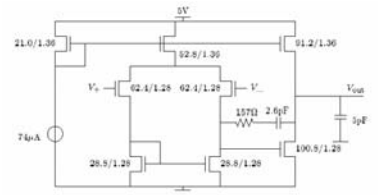
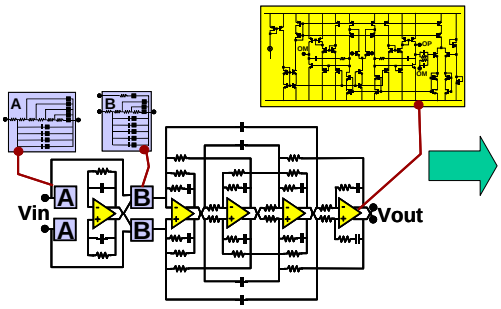
Problems with Scripting/Equations/Symbolic



Tell me gain/bandwidth
for this opamp, ~10 devices
== *easy*



Tell me noise, THD,
across all 6 operating settings
of the configuration switches
for this equalizer/filter frontend
for a commercial ADSL receiver
~400 devices == *hard*

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Aside: Commercial Scripting/ Eqn / Symbolic Efforts

- Marketplace has *not* been kind to these synthesis approaches

(Pre-packaged Equations + Scripting)

(Designer Equations + Symbolic)

(Designer Equations + Optimization)

(Pre-packaged Convex Equations + Optimization)

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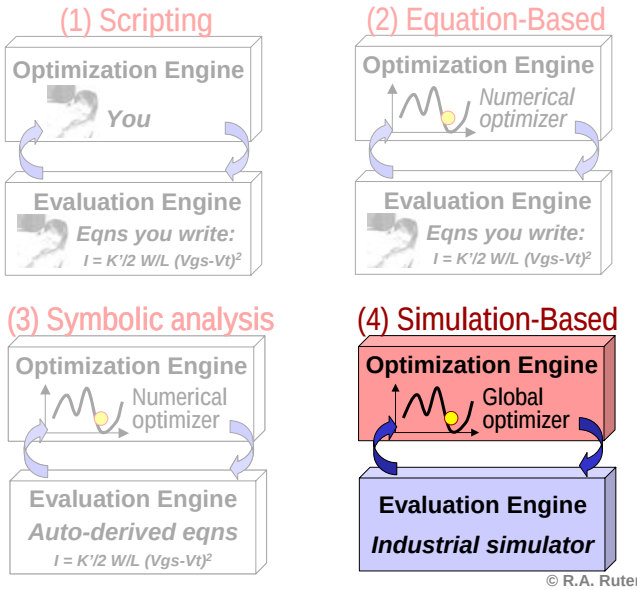
Back to our Historical Tour: What's Left?



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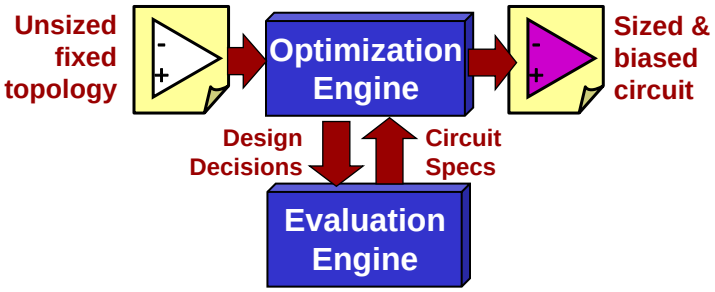
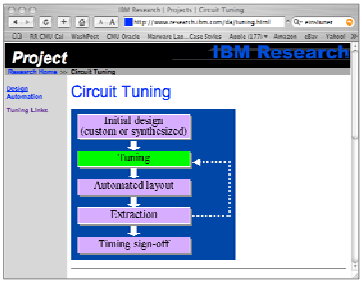
Analog Sizing Synthesis: Basic Architecture



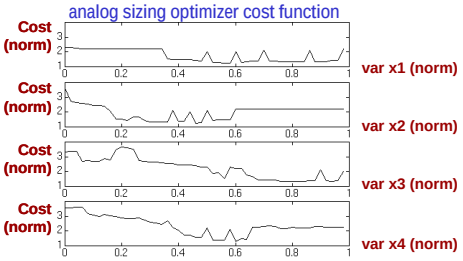
- Why it works
  - Eval engine is the same one designer uses, trusts for manual verification
  - Fast, cheap computers make it easy to use network parallelism for speed
  - Smart optimizers can deal with even very difficult circuit problems

Idea Should Not Be Unfamiliar to IBM

- IBM tuner tools, eg, *EinsTuner*
  - Large-scale optimizer
  - Adjusts device sizing
  - Simulation (circuit, timing) in loop
  - Very successfully applied
- What's different for analog case?
  - *Smaller* problems (10s – 100s devices)
  - Simulator *independent;* runs on *network*
  - *Not* smooth, *not* differentiable
  - *Cannot* use friendly gradient optimiz
  - Starting circuit may *not* be functional



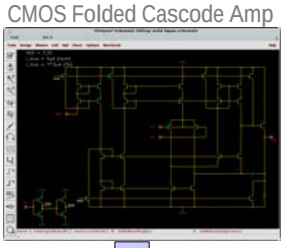
Example of 4 orthogonal "slices" thru analog sizing optimizer cost function



Industrial Applications

- Infineon result
  [Hennig, Sommer, Charlack, DATE02]

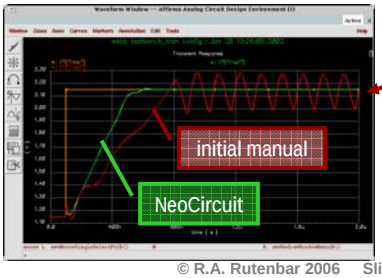
CMOS Folded Cascode Amp



Cadence NeoCircuit (Sizing)

Sizing optimization

Performance	Specification	Result
Supply voltage	3.3 V	
Load	10 MΩ || 10 pF	
DC Gain	> 90 dB	90.47 dB
Gain margin	> 3	3.152
Phase margin	> 60°	60.49°
Unity-gain frequency	> 2 MHz	2.972 MHz
PSRR	> 100 dB	120.9 dB
CMRR	> 110 dB	117.7 dB
Offset	< 1 mV	752.5 µV
Slew rate	> 1 V/µs, maximize!	2.331 V/µs
Settling time	< 500 ns	490.9 ns
Overshoot	< 50 mV	5.673 mV
Power	< 300 µW, minimize!	297.4 µW



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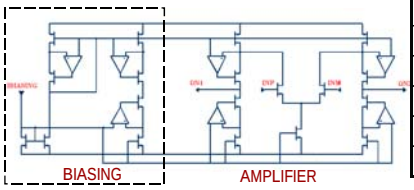
Industrial Applications

- STMicroelectronics result
  [Shah, Dugalleix, Lemery DATE02]

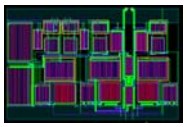


	GOALS at 0.18µm	RESULTS 0.18µm Corners	RESULTS 0.12µm Corners
DC Gain	> 70 dB	70 dB	70.3 dB
UGF	> 600 MHz	1.1 GHz	2.17 GHz
Phase Margin	> 45°	48°	49.2°
Settling Time	< 8 ns	7.4 ns	5.77 ns
Slew	> 400 V/µs	1900 V/µs	1620 V/µs
Power	< 10 mW	9.15 mW	1.1 mW

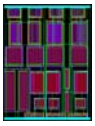
0.18µm → NeoCircuit (sizing) → NeoCell (layout)

0.12µm → NeoCircuit (sizing) → NeoCell (layout)

Both sizing and layout



Area: 0.009 mm^2
Power: 9.15 mW



Area: 0.004 mm^2
Power: 1.1 mW

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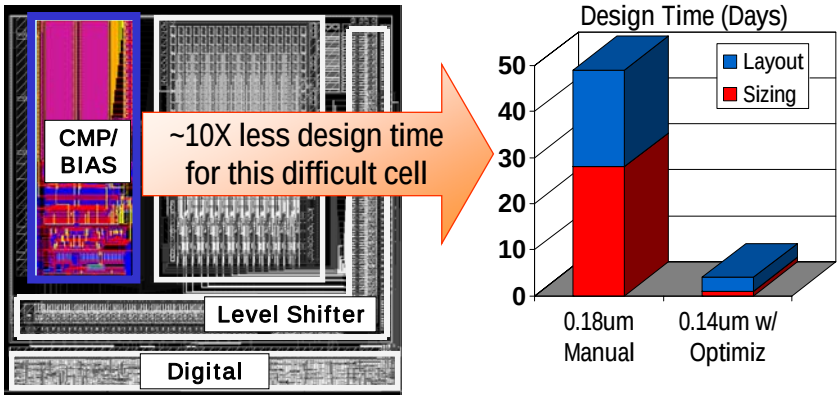
Industrial Applications

- Toshiba result
  - Porting a data converter from 0.18μm to 0.14μm



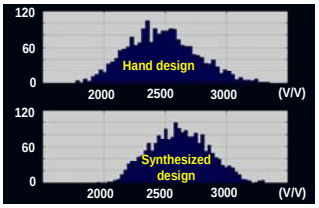
Mid-Point Summary

- Analog synthesis / optimization tools
  - Lots of progress over last decade
  - Moving (finally) from research into production
  - Moving (s l o w l y) from research into production
- What's next…?
  - *Lots..*

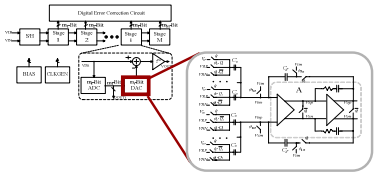
What's Next?

- (1) Usability

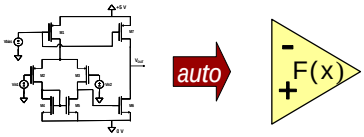
- (2) Statistical variability



- (3) Scalability: Circuits → Systems

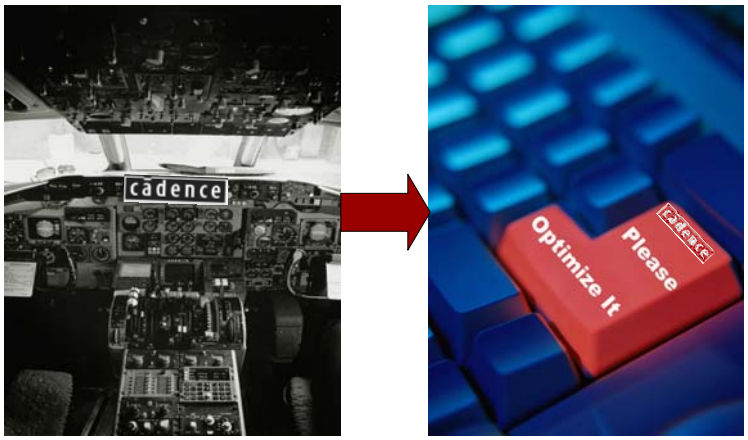


- (4) Systematic macromodeling



(1) Usability: Near-Term Challenge

- Yes Virginia – the tools can be *challenging* to use…



Usability Issues

- Some *myths* about analog optimization tools
  - They're *impossible* to set up and use
  - They're *brainless* – hitting a mosquito with a bazooka
  - They're *slow*
- Some *truths*
  - They're *hard* to set set up and use (we're working on it…)
  - They can be used very *intelligently* (if you're willing to invest in setup)
  - They're not so slow when you set them up *correctly*

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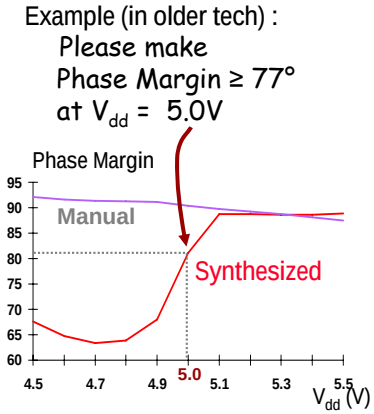
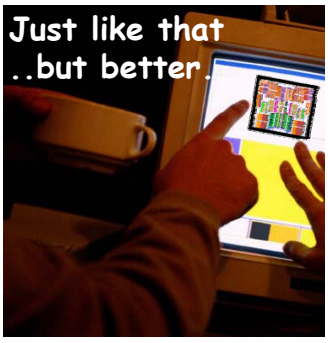
Why So Hard To Use? Constraint Mgt

- Optimizers give you *exactly* what you ask for – not one thing more
- Analog designs exceptionally rich in critical – *inexplicit* –constraints





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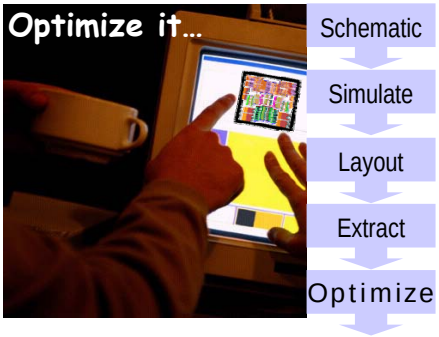
Robust Constraint Acquisition: *Big Problem*

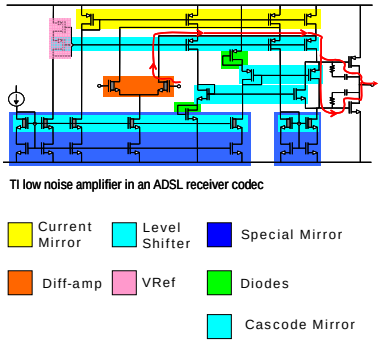
High-performing design teams often evolve highly individualized 'channels' for communicating critical design constraints.

Sadly, it's *not* universal across teams, technologies, companies…

Robust Constraint Acquisition & Management

- Much of this is just good integration, GUI, database work
- Interesting research on scriptable electrical/geometric constraint recognition and enforcement





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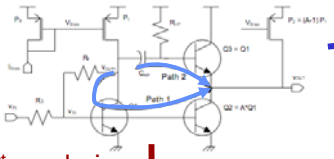
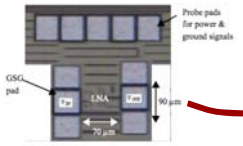
Final Point: Using Optimizers *Smart*

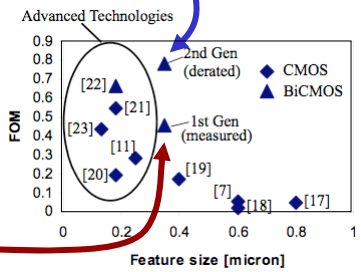
- Actually desirable to augment optimization setup with "smart" constraints – if you know them, put them in
  - Example: noise canceling wideband amp, after [Nauta JSSC04], from [Mukherjee et al, GLVLSI06], in 0.35um SiGe, done with Cadence optimizer



2nd gen design:
More *subtle* constraints on paths,
Add explicit FOM goals for
FOM = (s_{21} * BW) / (NF * P_{DC})

1st gen design:
constraints to
match *path gains*
for noise cancel





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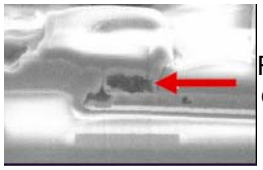
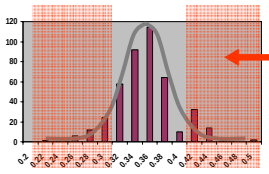
(2) Statistics: Long-Term Challenge for Yield Loss

- Process defects



Failure due to void

- Environmental / process variations



Out of spec

Functional Yield:
Chip does not work at all

Parametric Yield:
Chip works but not within specification

[Courtesy Andrzej J. Strojwas, CMU]

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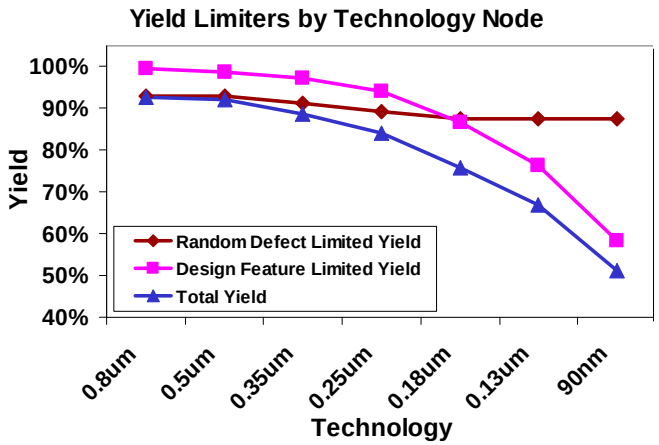
What Effects Limit Yield, As Technology Scales?



[Courtesy Andrzej J. Strojwas, CMU]

- Random defects are no longer the dominant yield loss mechanism
  - Yields are now limited by *design features, systematic* and *parametric* effects

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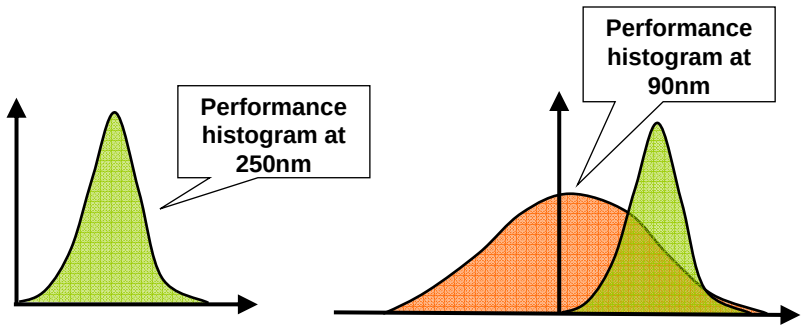
Analog Circuit Performance Variation *Increases*

- Analog always more sensitive to physics of fab process
  - Analog exploits rather than abstracts away basic nonlinearities of devices
  - Devices optimized for digital switching are increasingly lousy for analog



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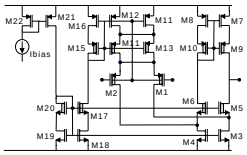
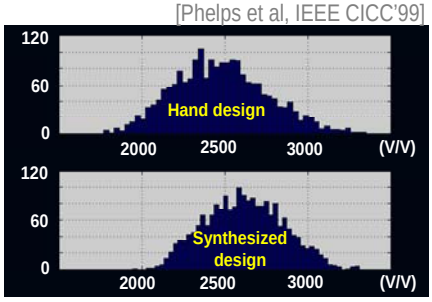
New Challenge: Statistically-Aware Optimization

- Good news: sim-based methods handle mfg corners easily
  - Sample result for TI circuit's low frequency gain; set up w/ *ad hoc* mfg constraints
  - 3σ process, +/-10% supply and temperature variations

[Phelps et al, IEEE CICC'99]





- Bad news: corners are no longer sufficient to ensure success
  - Too many corners, too much complexity, correlated behavior among statistics

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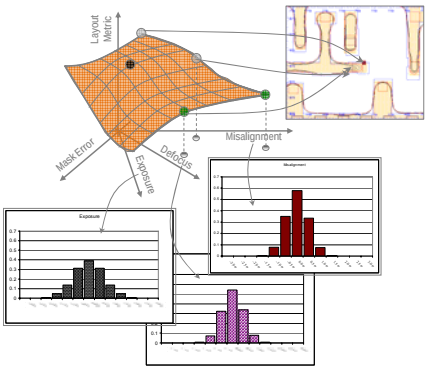
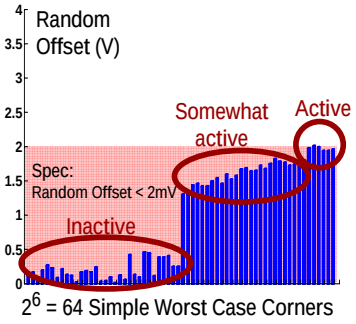
Broadly, Two Different Approaches

- Response surface methods (RSM)
  - Build a low-order model of how process disturbances affect design
  - Optimize on this surface



[Litho/Layout RSM from Andrzej Strojwas CMU]

- Dynamic (active) corners
  - Specify a vast number of process corners (Monte Carlo spread) but figure out which ones really *matter*, either up front, or on the fly



2^6 = 64 Simple Worst Case Corners

[Mukherjee et al, IEEE TCAD'00]

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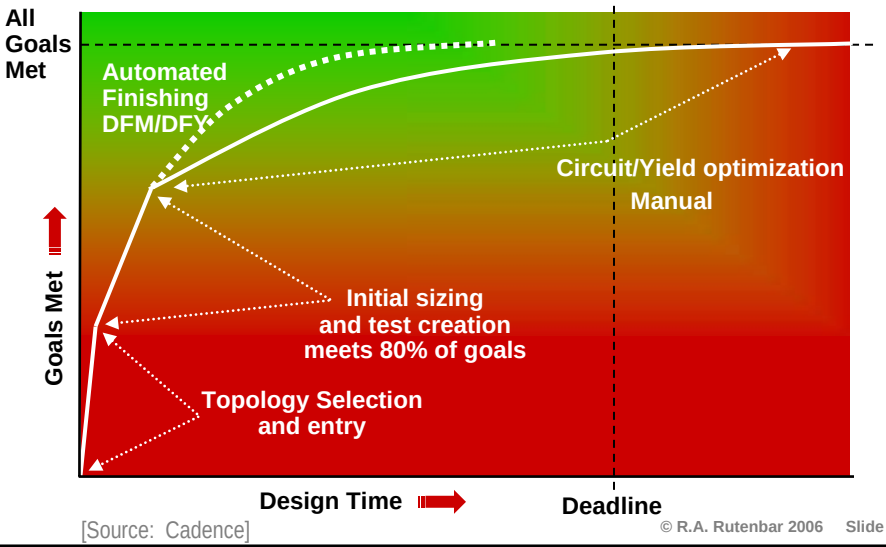
One Usage Model: *Circuit Finishing*

- DFM/DFY by hand is painful: last 20% of design takes 80% of time



[Source: Cadence]

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Statistics: Challenges

- Dimensionality
  - I don't want to handle just 10 statistical variations, want to handle 10,000
  - Leads to work on statistical dimensionality reduction (principal components)
- Correlation / complexity
  - Life would be great if all disturbances were Gaussian & independent.
  - They're not.
- Optimization
  - Once got statistics / dimensionality handled, how do formulate optimization?
  - And, optimizing what cost function form? Linear, quadratic, convex, arbitrary?
- Lots of different ideas bubbling around now; *active* area

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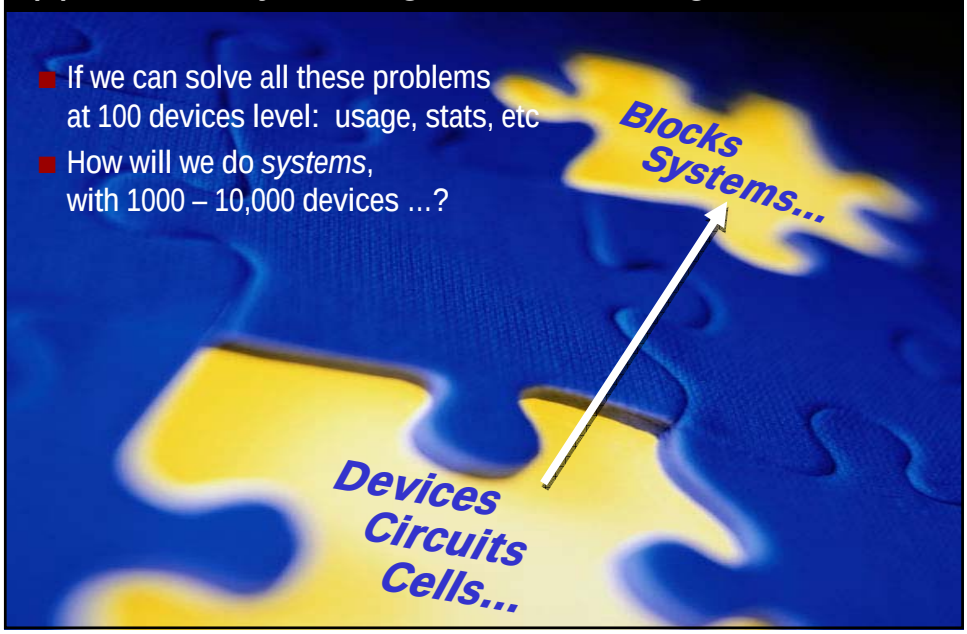
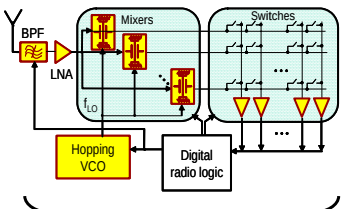
(3) Scalability: Long-Term Challenge

- If we can solve all these problems at 100 devices level: usage, stats, etc
- How will we do *systems*, with 1000 – 10,000 devices …?

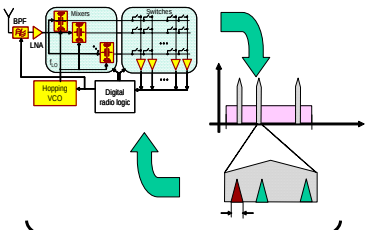


Why Not Synthesize *Flat*, like a Basic Circuit?

- Too complex
  - Too many design decisions for effective optimization
- Too slow to evaluate
  - Simulation-based synthesis needs to simulate *each* candidate solution many times during search



~ 10K design decisions



~ hours → days

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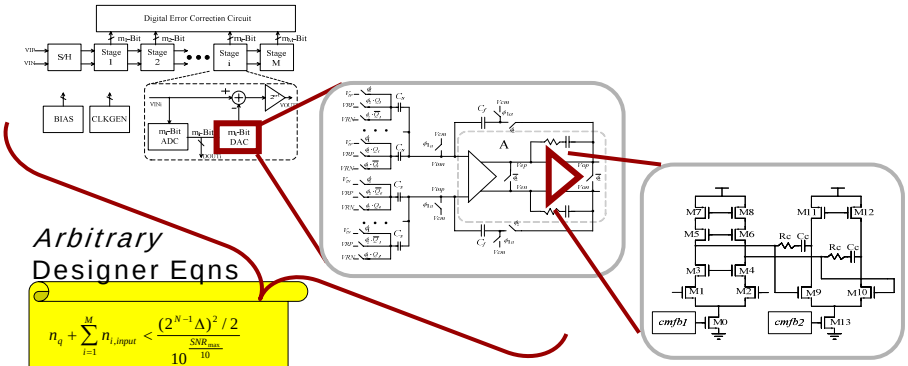
Strategy: Hybrid Optimization

- Idea: Use same infrastruct, *replace* simulators
  - Simulation-based optimization is natural for individual circuits
  - Equations, parameterized by circuit sims, natural for bigger systems



Arbitrary Designer Eqns

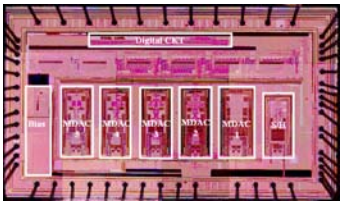
$$n_q + \sum_{i=1}^{M} n_{i,input} < \frac{(2^{N-1}\Delta)^2/2}{10^{\frac{SNR_{max}}{10}}}$$

$$\left|V_{out}(t = T1) - V_{slew\_ideal}\right| \le V_{tol}$$

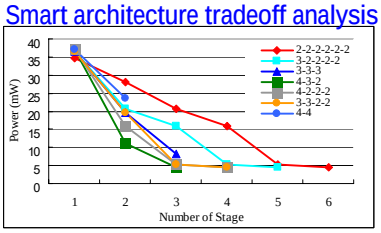
●●●

+ Ckt Simulations

Example: *Hybrid* Synthesis Solution

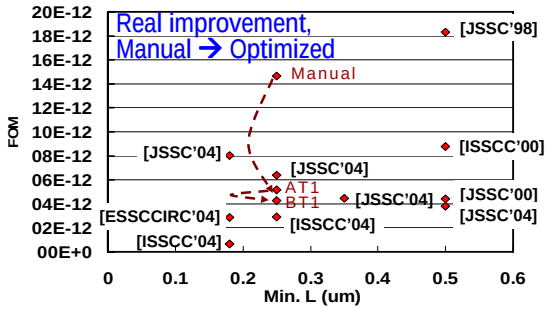


Smart architecture tradeoff analysis



- CMU (US) + ITRI (Taiwan) collaborative design
- 40MS/s 13b pipelined ADC 69.2dB SNR @ 250nm
- Equations + sims + optimization

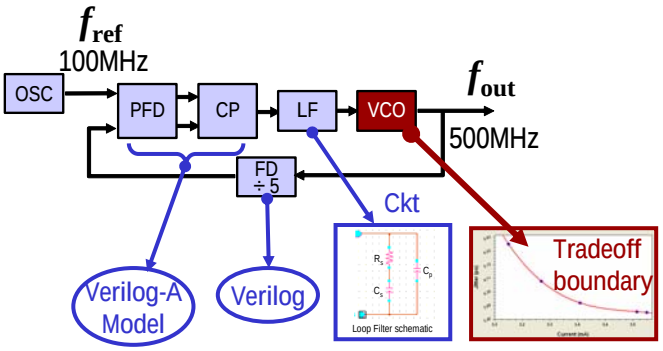
[Chien, Mukherjee et al, ASSCC'05]



AT1: First two MDAC stages synthesized
BT1: All MDACs synthesized

Another Idea: Replace Circuits with Tradeoff Curves

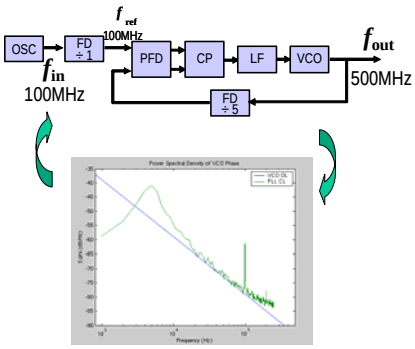
- Replace device blocks with either simple macromodels or *optimal tradeoff curves* obtained via circuit-level auto-sizing
  - Abstract away device details into essential tradeoffs that matter for system
  - Example: for the VCO in a PLL, Power vs Jitter for a VCO
  - System level "sizing" chooses right points on curve for each block



[Tiwary, et al, *Proc. Nanotech 2004 Conf.*]

Reminder: Why is Sizing the PLL So Hard?

- Why is this hard?
  - 2 hours in SpectreRF to simulate enough cycles to estim PLL jitter



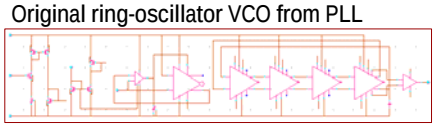
VCO openloop phase noise compared with that in C-L

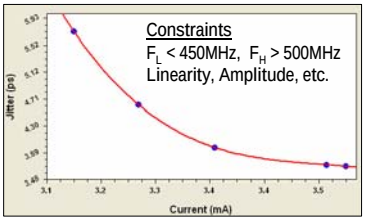
- Consequences
  - Cannot visit enough candidate solutions to find a good final ckt
  - Cannot synthesize this flat
  - Better simulators will help, but they cannot erase this problem
- Solution
  - Need to replace individual ckts with appropriate macromodels
  - Need to reduce number of variables
  - Need to reduce overall eval time

Tradeoff Models: Can Derive with Existing Tools

- Several sizing runs, *carefully* set up, can trace these tradeoff curves

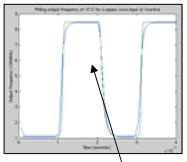
Original ring-oscillator VCO from PLL



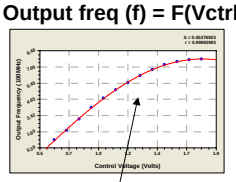


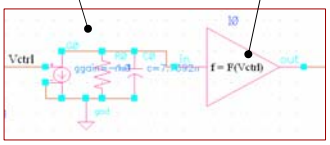
Bias current vs Jitter tradeoffs

One pole for delay



Output freq (f) = F(Vctrl)

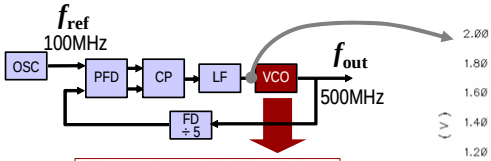




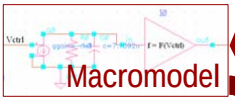
Manually derived model template lets us simulate a VCO for *any* pt on this curve

[Tiwary, et al, *Proc. Nanotech 2004 Conf.*]

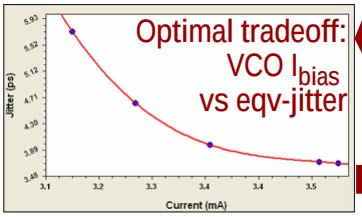
Complete PLL Synthesis Results

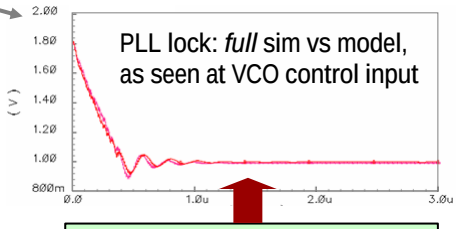


Detailed Ckt



Macromodel





Target PLL simulated 4000 cycles for each synthesis pt, ~4hrs on 1 CPU to optimize, for example:

PLL settling time: 0.822 us
VCO bias current: 3.37 mA
PLL jitter: 0.46% (9.1ps)

Cadence NeoCircuit

[Tiwary, et al, *Proc. Nanotech 2004 Conf.*]

(4) Macromodeling: Long-Term Challenge

"*The Allegory of St. Darlington,*" from Pane 37, North window, Central vault, Notre Linear

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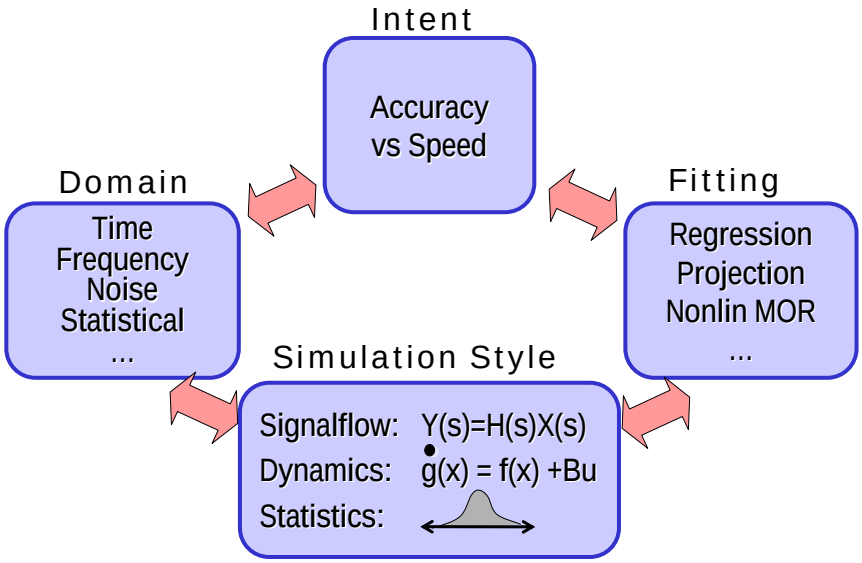
Why So Hard? End-Use Diversity Complicates Problem



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...As Do User Expectations

- Like simulator controls, everybody hates having to "twiddle" model details
- This is what every designer *ultimately* wants

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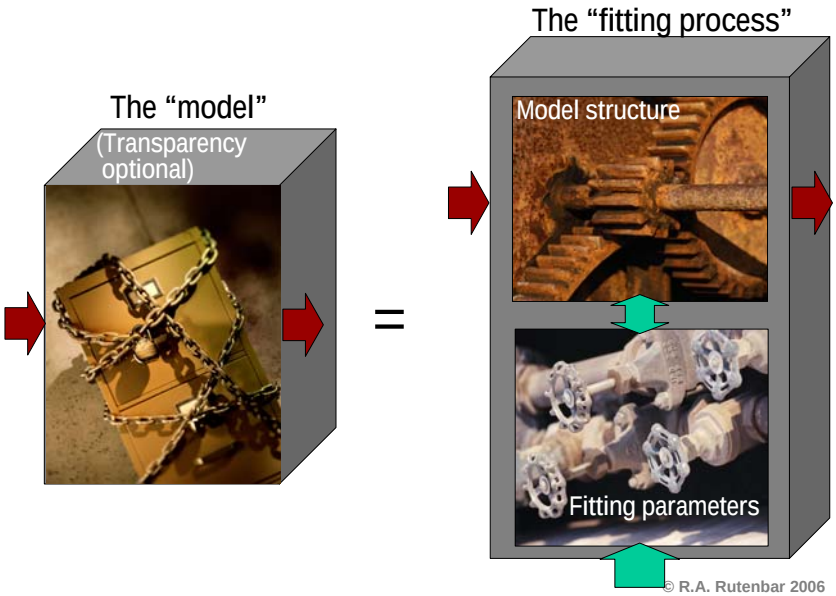
Today's Models Don't Always Inspire Confidence



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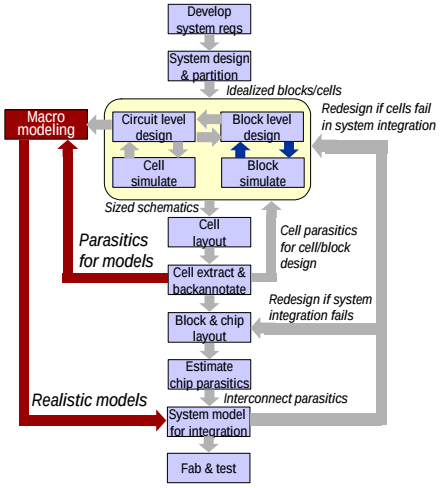
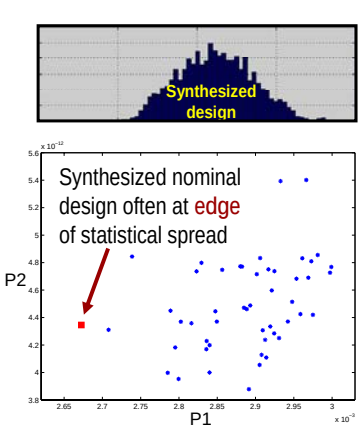
Why Macromodeling Matters

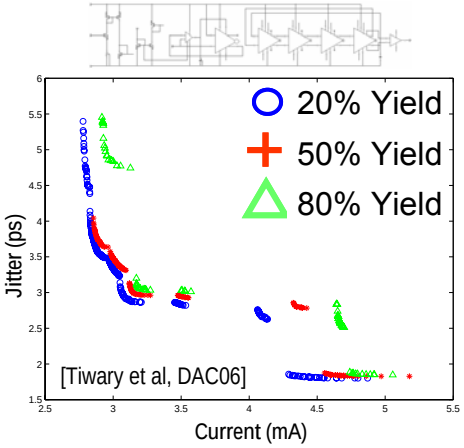
- Rutenbar's Rule:
  - *"Everybody who starts out working on optimization, ends up working on macromodeling"*
- Why
  - As we get optimization methods that are increasingly *practical*…
  - …we want more tools to automatically *abstract* circuits
  - …we expose *weaknesses* in simulation-based verification methodology, for full systems



Lots of Cross-Links Across 4 Challenges

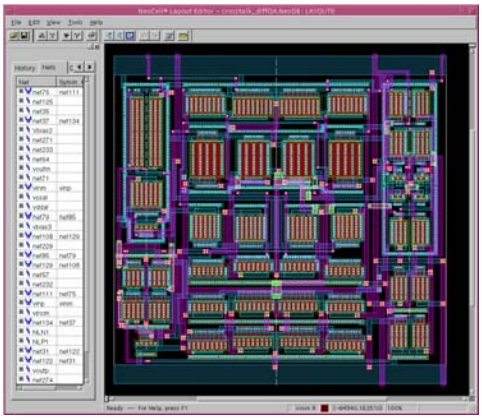
- Statistical… tradeoff macromodels … for system optimization
- Statistical tradeoff surfaces – tradeoff curves with *yield nums*





Summary

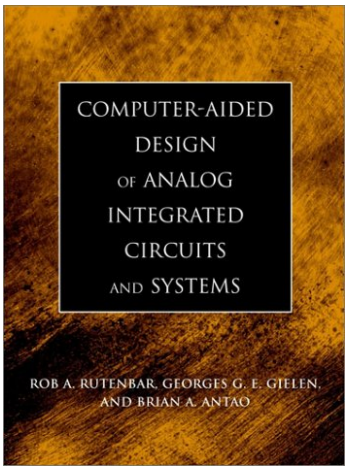
- Analog CAD
  - Not an oxymoron
  - We're making progress
  - Lots of optimization ideas in first gen commercial form
- New challenges
  - Usability
  - Statistics
  - Scalability
  - Macromodeling
- High hopes of analog CAD job security in coming years…



Courtesy Cadence

To Learn More: Mixed-Signal CAD

- Computer-Aided Design of Analog Integrated Circuits and Systems
  - Rob A. Rutenbar, Georges G. E. Gielen, Brian A. Antao, Editors
  - Hardcover: 768 pages
  - Publisher: IEEE
  - Published: April 2002
  - ISBN: 047122782X
- Book is a collection of essential papers on all aspect sof analog and mixed signal synthesis, modeling, layout, etc. Most of the results shown here appear in these papers.



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- From TI, Dallas
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