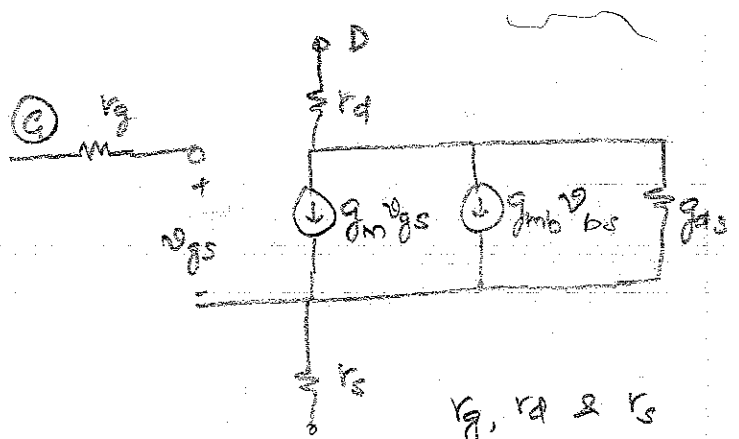
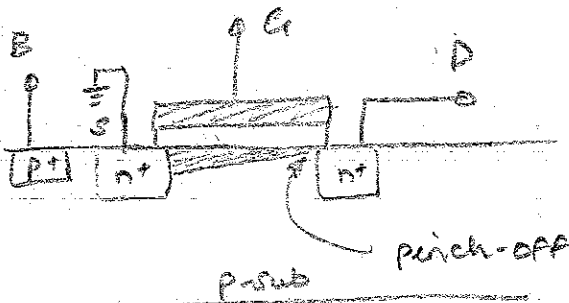


- A few applications -
- PCB chip-to-chip signaling links
  - optic fibre communications  
(transimpedance amplifiers)
  - Wideband wireline communication  
(TV: 48MHz - 1100MHz)
  - Measurement instrument front-ends  
e.g. oscilloscopes
  - Wireless: Ultra-wideband radio & multi-standard receivers.

Review of MOS small-signal models:

(a) DC model in saturation



(i) Long-channel

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$V_T = V_{T0} + \gamma \left[ \sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right]$$

$$g_m = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right) I_D} = \frac{2I_D}{V_{GS} - V_T} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)$$

$$g_{mb} = \frac{\gamma g_m}{\sqrt{|2\phi_F| + V_{SB}}} \quad \text{where } \gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$

$$g_{ds} = \lambda I_D \quad \text{where } \lambda \propto \frac{1}{L}$$

$r_g, r_d$  &  $r_s$   
→ extrinsic resistances in device

(b) Short-channel model:

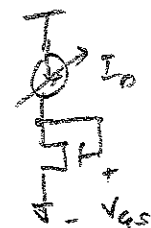
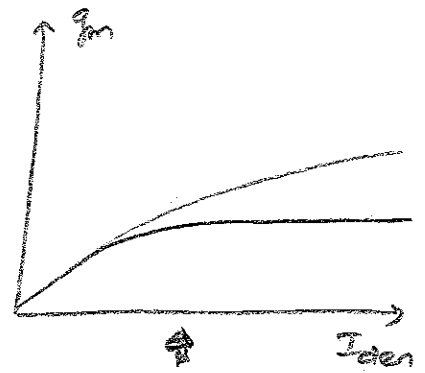
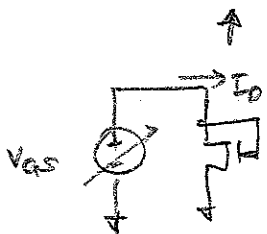
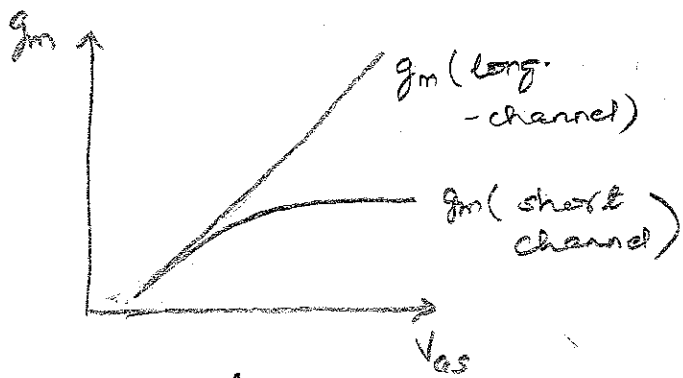
Recall that the horizontal electric field in the MOS channel is  $E_H = \frac{V_{as}}{L}$ . In an NMOS device,  $E_H$  accelerates electrons from the source to the drain. The velocity of an electron increases as it approaches the drain. If  $E_H$  is larger than some critical value  $E_c$  the velocity saturates. This can happen at large  $V_{ds}$  values or in short-channel length devices.

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{as} - V_T) \left[ (V_{as} - V_T) \parallel L E_c \right]$$

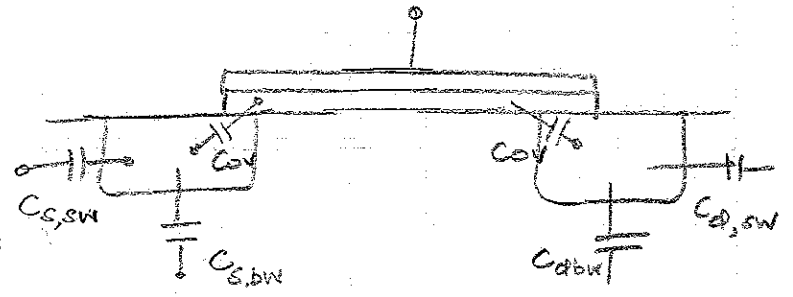
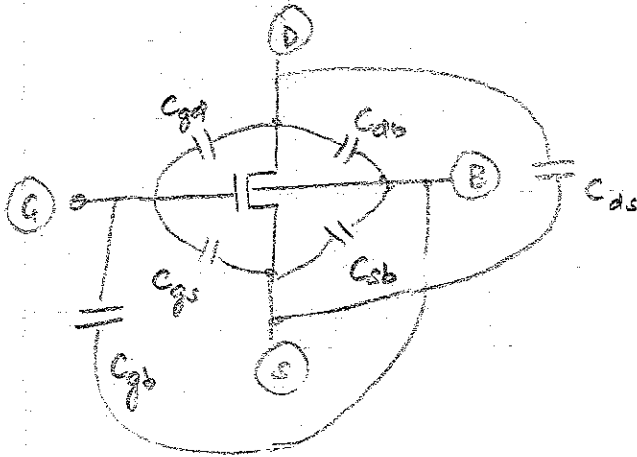
$$\propto \begin{cases} V_{as} - V_T & \text{if } \frac{V_{as} - V_T}{L} \ll E_c \text{ (no vel. sat.)} \\ L E_c & \text{if } \frac{V_{as} - V_T}{L} \gg E_c \text{ (with vel. sat.)} \end{cases}$$

$$g_m = \begin{cases} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{as} - V_T) & \text{w/o velocity sat} \\ \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (L E_c) & \text{with velocity sat.} \end{cases}$$

$\Rightarrow g_m$  does not increase with  $V_{as}$ !



(c) Parasitic capacitances:



(Refer to Gray & Meyer for expressions in other regions of operation)

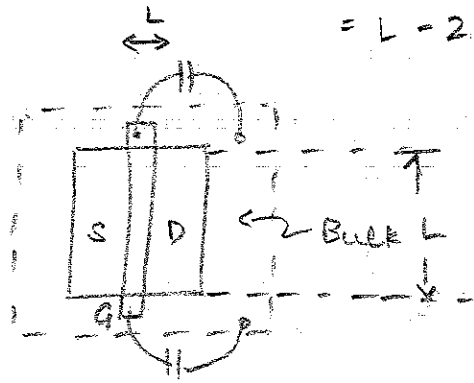
In saturation:

•  $C_{gs} = \frac{2}{3} C_{ox} W l_{eff} + C_{ov} W$  (Left = effective channel length =  $L - 2l_{ov}$ )

•  $C_{gd} = C_{ov} W$

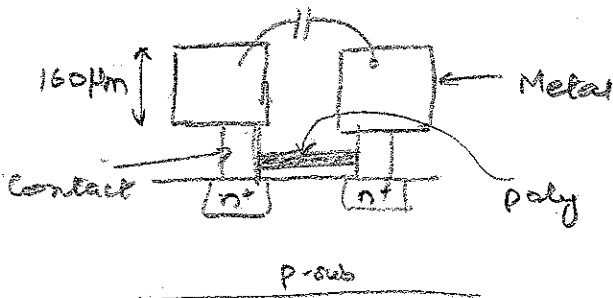
•  $C_{gb} = C_{gbov} L$

•  $C_{db}$  &  $C_{sb}$  are depletion capacitances of reverse biased diodes:



$$C_{db} = \frac{C_{j0} W}{\left(1 + \frac{V_{db}}{V_0}\right)^{m_{j0}}} + \frac{C_{jsw} \cdot W}{\left(1 + \frac{V_{db}}{V_0}\right)^{m_{jsw}}}$$

•  $C_{ds}$  is usually not included in a MOS model. However, it can be significant in very short-channel MOS.



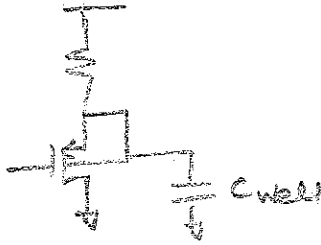
Note that in very short channel MOS technology, the height of the metal is greater than the minimum channel length.

(eg.  $H_{M1} = 160nm$ ,  $L_{min} = 90nm$ )

- Other parasitics:
- interconnect capacitance (parasitic extraction)
  - wiring inductance (EM field solvers)
  - extrinsic resistances
    - poly gate resistance (reduced by silicide)
    - S-D implant resistances
    - interconnect resistances

Rule of thumb  
 $L = 0.5 - 1 \text{ nH/mm}$  of wire

Also for PMOS devices → well-to-ground capacitance  
 Example: PMOS source follower:



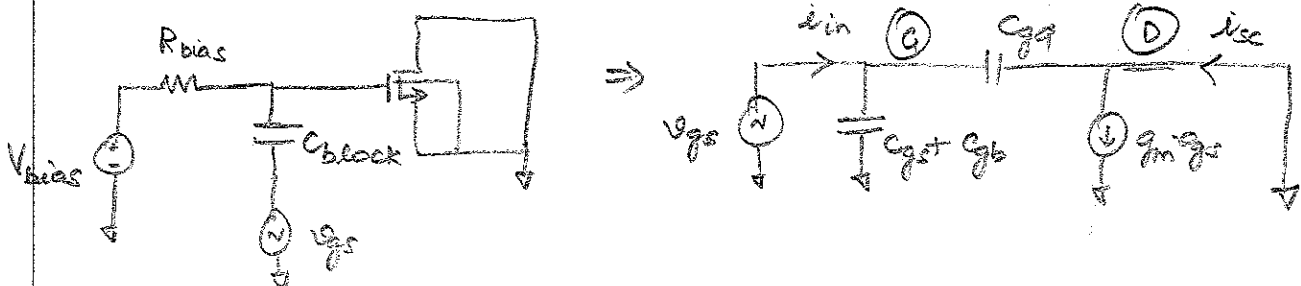
High-frequency figures of merit:

- $f_t$  = transition frequency = frequency at which current gain is unity.
- $f_{max}$  = max. frequency of oscillation = frequency at which power gain is unity.

Calculation of  $f_t$ :

Although MOS gate current is 0 at DC, it draws current at high frequency.

$f_t$  = frequency at which short-circuit current gain of a common-source amplifier falls to unity:





(3) The picture is not as rosy in velocity-saturated devices:

$$g_m \approx \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) L E_c, \quad C_{gs} \approx \frac{2}{3} C_{ox} W L$$

$$\Rightarrow \boxed{f_T \approx \frac{1}{2\pi} \frac{3}{2} \frac{\mu_n E_c}{L}} \Rightarrow f_T \text{ scales as } L^{-1} \text{ (not } L^{-2}) \text{ in the short-channel regime}$$

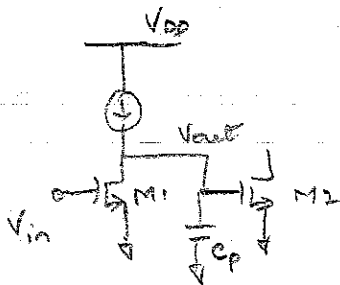
(4) NMOS devices have 2 to 3 times greater  $f_T$  than PMOS.

$$\mu_n \approx 2.5 \mu_p$$

$$I_{dn} \approx 2.5 I_{dp}$$

$$g_{mn} \approx 2.5 g_{mp}$$

Gain - Bandwidth trade-off:



→ C-S amp drives an identical stage.

Voltage transfer function is:

$$\frac{V_{out}(s)}{V_{in}} = A_V(s) = \frac{g_m r_{ds}}{1 + s C_L r_{ds}}$$

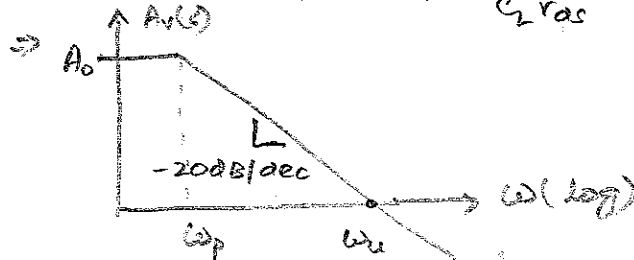
$$C_L = C_p + C_{gs2}$$

$$\Rightarrow \text{DC gain } A_0 = g_m r_{ds}$$

$$\text{3dB frequency } \omega_p = \frac{1}{C_L r_{ds}}$$

Unity gain frequency

$$\text{is } \omega_u = A_0 \omega_p = \frac{g_m}{C_L}$$

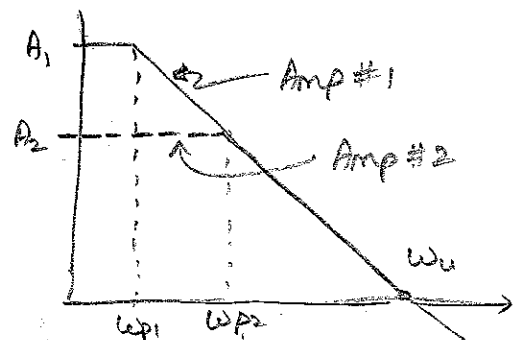


→  $\omega_u$  is fixed by device size, bias point and load cap

Wideband amplifier specs include DC gain  $A_0$ , 3dB BW  $\omega_{-3dB}$  and a max. power dissipation.

Key point: We often can't satisfy

both the gain & BW specs with one stage without increased power dissipation.

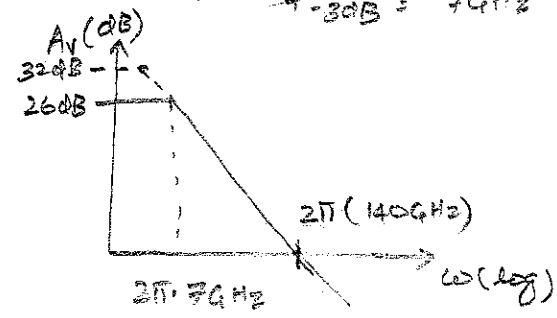


Consider some numbers:  
 (typical for our 0.13µm process)

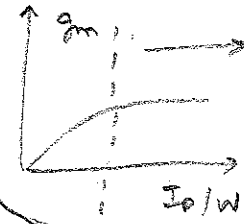
$$g_m r_{ds} = 20 \text{ (26 dB)}$$

$$f_T = \frac{g_m}{C_{gs}} = \frac{g_m r_{ds}}{r_{ds} C_{gs}} = 2\pi (140 \text{ GHz})$$

$$\Rightarrow f_{-3dB} = 7 \text{ GHz}$$



- Note that this is a very optimistic calculation.
- Also note that increasing power cannot take us much further:



Velocity saturation  
 $\Rightarrow$  we can increase  $g_m$  by increasing  $W$ , but  $C$  also increases proportionately  
 $\Rightarrow \frac{g_m}{C} \rightarrow \text{constant}$

But suppose we want higher gain (say 32dB) with the same  $\omega_{-3dB}$  (say 7GHz). Does the above analysis mean that we cannot design such an amplifier?

- Gain-BW product for a single stage cannot be increased further.

- $\Rightarrow$  Not with one stage, even with increased power consumption
- $\Rightarrow$  BUT: we can, if we cascade a number of amps each having a single pole roll-off.
- $\rightarrow$  but we have greater delay.

$\Rightarrow$  Gain-Bandwidth-Delay trade-off is most fundamental.

General problem statement: For a given total gain specification

- $A_{TOT}$  bandwidth
- How do we maximize  $3dB_{\wedge}$  for the cascaded system?
  - How do we minimize delay?

## A few loose ends on noise

Recall for a source degenerated C-S LNA, the noise contribution of the device is:

$$F = 1 + \left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma g_{do}}{g_m} \frac{1}{2Q} \left[ 1 + (4Q^2 + 1) \left(\frac{g_m}{g_{do}}\right)^2 \frac{\delta}{5\gamma} - 2|c| \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}} \right]$$

If we ignore gate-noise (ie  $\delta \rightarrow 0$ ),

$$F \approx 1 + \left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma g_{do}}{g_m} \frac{1}{2Q}$$

- For a velocity saturated device,  $g_{do} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{as} - V_T)$ ,

$$g_m \approx \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) L E_c \quad \text{and} \quad \omega_T = \frac{3}{2} \frac{\mu_n E_c}{L}$$

$$\text{Also, } C_{gs} = \frac{2}{3} C_{ox} W L \quad \text{and} \quad Q = \frac{1}{2\omega_0 R_0 C_{gs}}$$

$$\Rightarrow F_{vsat} = 1 + \frac{3}{2} \frac{\omega_0}{C_{ox} W R_0} \cdot \frac{1}{\mu_n^2 E_c^3} (V_{as} - V_T)$$

- For a given device size,  $F_{vsat} \uparrow$  as  $(V_{as} - V_T) \uparrow$  (or  $F_{vsat} \uparrow$  as current density  $\uparrow$ )

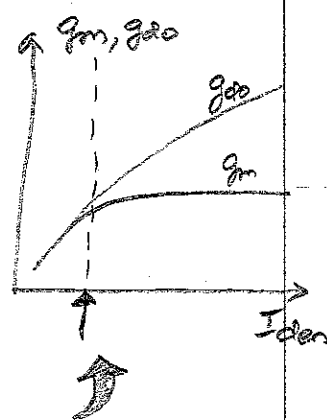
- For a long-channel device w/o velocity saturation:

$$g_m = g_{do} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_T)$$

$$\omega_T = \frac{3}{2} \frac{\mu_n (V_{as} - V_T)}{L^2}$$

$$\Rightarrow F_{long} \approx 1 + \frac{\gamma}{2Q} \cdot \frac{4}{9} \frac{\omega_0^2 L^4}{\mu_n^2 (V_{as} - V_T)^2}$$

- $F_{long} \downarrow$  as  $(V_{as} - V_T) \uparrow$  (or as  $I_{den} \uparrow$ )



- Optimally want to operate close to the velocity saturation limit for low-noise