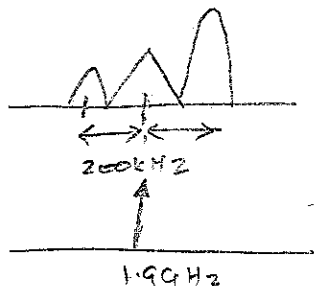


I PLL's in wireless systems:

1) Need to accurately tune frequency to receive a desired channel \leftarrow Frequency synthesizers.

e.g. GSM/PCS in 1.9GHz band, channel spacing = 200kHz



- Need an accuracy of 100's of Hz in LO frequency

- Free-running VCO frequency drifts with temperatures, loading etc

2) Coherent detection: need to lock overall phase at Rx. to the carrier phase of transmitter \rightarrow usually done in the digital domain as a digital or software PLL.

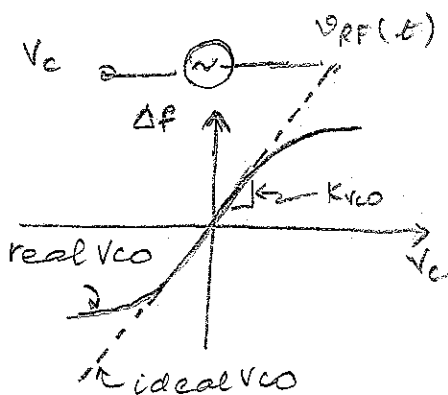
3) Polar modulation in FM-type transmitters (e.g. GSM)

- VCO acts as a frequency modulator.

\Rightarrow data modulation + RF upconversion in one-step.

- PLL locks VCO to an external reference and also allows tuning of RF frequency.

II Linear model of VCO



Tuning characteristics of VCO

$$\Delta f = f_{VCO} - f_0$$

f_{VCO} = total instantaneous VCO output freq.

f_0 = free running frequency of VCO.

$$\Delta f = K'_{VCO} V_c(t)$$

VCO gain
in Hz/V

control voltage, possibly
time varying (noise or
modulation)

$$\Rightarrow f_{VCO}(t) = f_0 + K'_{VCO} V_c(t)$$

\rightarrow control voltage modulates instantaneous O/P frequency \Rightarrow frequency modulator.

Recall relationship between instantaneous phase and frequency:

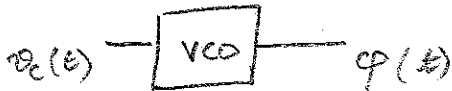
$$f_i(t) = \frac{1}{2\pi} \frac{d\theta(t)}{dt} \Rightarrow \theta(t) = 2\pi \int_{-\infty}^t f_i(t) dt = 2\pi \int_0^t f_i(t) dt + \theta_0$$

$$\theta(t) = \underbrace{2\pi f_0 t}_{\text{carrier phase}} + 2\pi K'_{VCO} \int_0^t \underbrace{v_c(t)}_{\text{excess phase } \phi(t)} dt + \underbrace{\theta_0}_{\text{initial phase}}$$

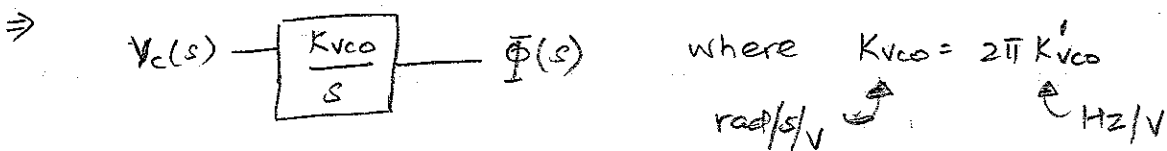
• Ideal VCO output voltage:

$$v_{RF}(t) = A \cos \left[2\pi f_0 t + 2\pi K'_{VCO} \int_0^t v_c(t) dt + \theta_0 \right] \rightarrow \text{frequency modulated RF output}$$

• Phase-domain model: If we think of the control voltage as the input and the excess phase $\phi(t)$ as the output, then an ideal VCO is an LTI system:



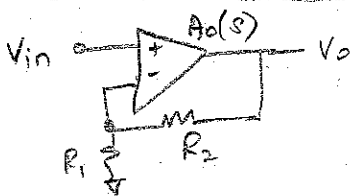
$$\phi(t) = 2\pi K'_{VCO} \int_0^t v_c(t) dt \iff \Phi(s) = \frac{2\pi K'_{VCO}}{s} V_c(s)$$



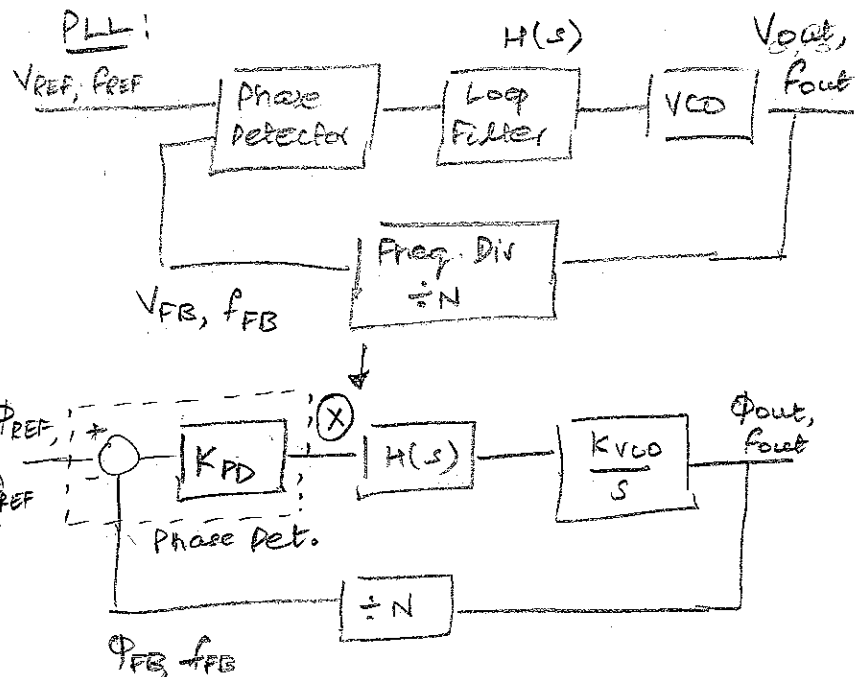
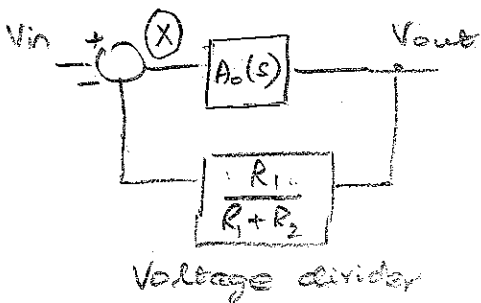
III

Basic PLL analogy:

Feedback amplifier:



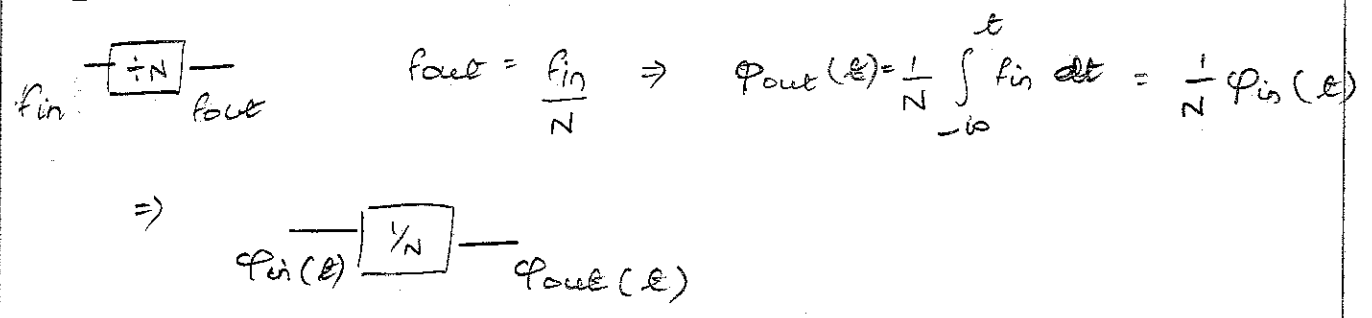
linear model



For a slowly varying voltage input, the large loop gain drives voltage error @ (X) to zero

- For a slowly varying phase input, the large loop gain drives the phase error to a constant, well defined value (which is not always zero)
- This is called phase-lock.
- Phase-lock \Rightarrow frequency lock
 i.e. $\theta_{REF}(t) - \theta_{FB}(t) = \theta_e = \text{constant}$
 $\Rightarrow \frac{1}{2\pi} \frac{d\theta_{REF}}{dt} - \frac{1}{2\pi} \frac{d\theta_{FB}}{dt} = 0$
 $\Rightarrow f_{REF} = f_{FB}$
- However, frequency lock does not imply phase-lock.

IV Phase-domain model of frequency divider:



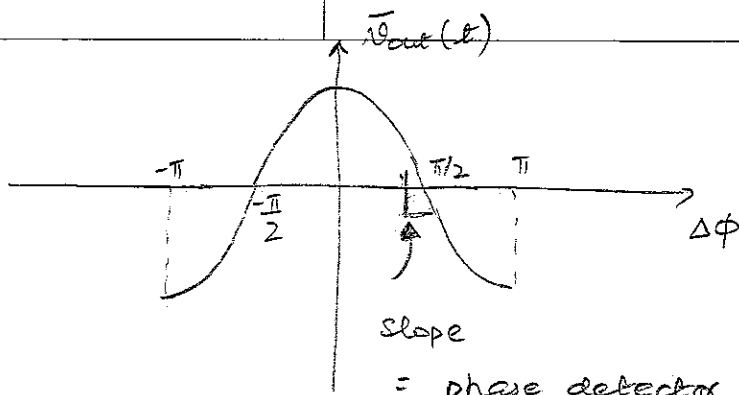
V Multiplier-based phase detectors:

(a) Multiplier: (4-quadrant, Gilbert cell)

$V_{REF}(t) = A_1 \cos \omega_1 t$
 $V_{FB}(t) = A_2 \cos(\omega_2 t + \Delta\phi)$
 Multiplier gain = α

$\Rightarrow V_{out}(t) = \alpha \cdot A_1 \cos \omega_1 t \cdot A_2 \cos(\omega_2 t + \Delta\phi)$
 $= \frac{\alpha A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t + \Delta\phi] + \frac{\alpha A_1 A_2}{2} \cos[(\omega_1 + \omega_2)t + \Delta\phi]$

For $\omega_1 = \omega_2$, average output $\overline{V_{out}(t)} = \frac{\alpha A_1 A_2}{2} \cos(\Delta\phi)$

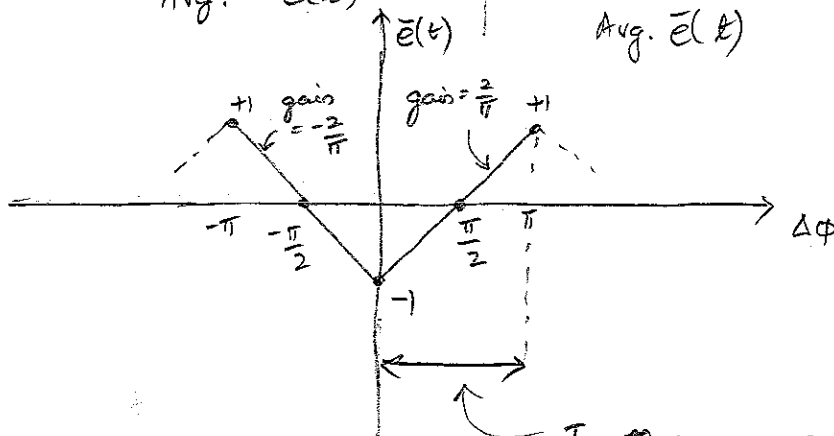
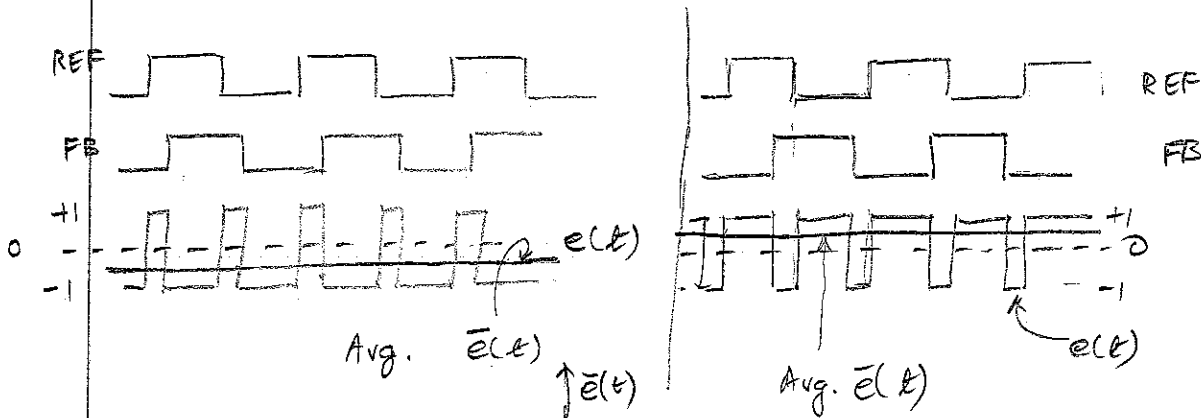


Around $\Delta\phi \approx \frac{\pi}{2}$, $\bar{V}_{out}(t) = \frac{\alpha A_1 A_2}{2} \sin\left(\frac{\pi}{2} - \Delta\phi\right) \approx \frac{\alpha A_1 A_2}{2} \left(\frac{\pi}{2} - \Delta\phi\right)$

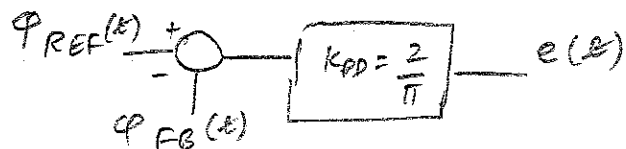
$\Rightarrow K_{PD} = \frac{-\alpha A_1 A_2}{2}$

(b) XOR gate (= over-driven four-quadrant multiplier)

REF \Rightarrow $e(t)$ or a digital gate

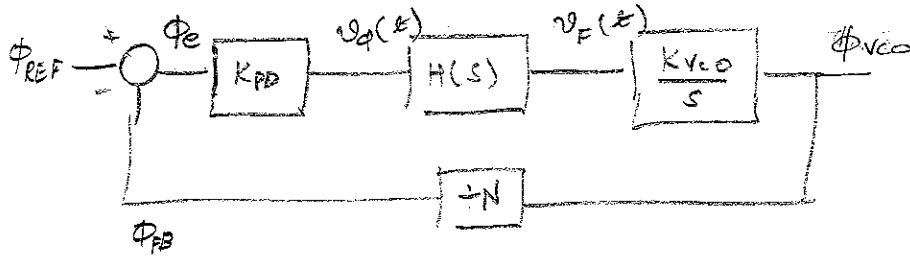


In this range $\Delta\phi \in (0, \pi)$
phase-domain model is

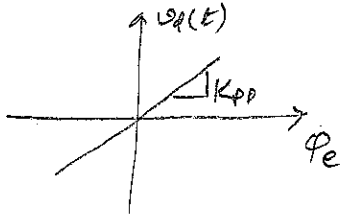


Note that in these cases, the PLL achieves lock in quadrature i.e. REF & FB differ in phase by 90° in steady-state

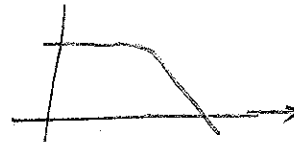
Linear PLL model:



- Assume that PLL is locked i.e. ϕ_e is constant in time
- Assume that the PD has an incremental transfer function:



- Assume $H(s)$ is low pass:



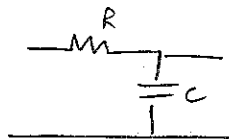
- Linear model works for small perturbations about this operating point.

• Loop gain $T_O(s) = K_{PD} \frac{K_{VCO}}{s} \cdot \frac{1}{N} \cdot H(s)$

this is a Type - I loop because the number of lossless integrations in the loop = 1

• C.L Transfer function $A_{CL}(s) = \frac{K_{PD} \cdot H(s) \cdot K_{VCO}/s}{1 + K_{PD} \cdot H(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N}} = \frac{\phi_{VCO}(s)}{\phi_{REF}}$

$$\Rightarrow A_{CL}(s) = \frac{K_{PD} \cdot K_{VCO} H(s)}{s + \frac{K_{PD} K_{VCO}}{N} H(s)}$$

• For a simple LPF:  , $H(s) = \frac{1}{1+s/\omega_p}$

$$\Rightarrow A_{CL}(s) = N \frac{K_{PD} K_{VCO}/N}{\frac{s^2}{\omega_p} + s + \frac{K_{PD} K_{VCO}}{N}} \quad \left(\equiv N \cdot \frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \right)$$

Define $K = \frac{K_{PD} K_{VCO}}{N} \Rightarrow \omega_n = \sqrt{\omega_p K}$ and $\zeta = \frac{1}{2} \sqrt{\frac{\omega_p}{K}}$

- Note that $A_{CL}(s)$ relates the output phase to input phase & also output excess freq. to input excess frequency:

$$\text{i.e. } A_{CL}(s) = \frac{\Delta \omega_{VCO}(s)}{\Delta \omega_{REF}} = \frac{\phi_{VCO}(s)}{\phi_{REF}}$$

Also calculate the phase error T.F:

$$A_e(s) = \frac{\phi_e}{\phi_{REF}}(s) = \frac{\phi_{REF} - \phi_{VCO}/N}{\phi_{REF}} = 1 - \frac{1}{N} A_{CL}(s)$$

$$\Rightarrow A_e(s) = \frac{s^2/\omega_n^2 + 2\zeta s/\omega_n}{s^2/\omega_n^2 + 2\zeta s/\omega_n + 1}$$

(i) If input is a phase step: $\phi_{REF}(s) = \frac{\Delta\phi}{s}$ what is the steady state output?

Recall initial value theorem of Laplace transform theory:

$$y(t)|_{t \rightarrow \infty} = \lim_{s \rightarrow 0} s Y(s)$$

$$\Rightarrow \phi_{VCO}(t \rightarrow \infty) = N \Delta\phi \quad \text{ie} \quad \phi_{FB}(t \rightarrow \infty) = \Delta\phi$$

$$\& \quad \phi_e(t \rightarrow \infty) = 0$$

\therefore Type-I PLL tracks input phase step with zero steady state phase error

(ii) Input = phase ramp, or frequency step:

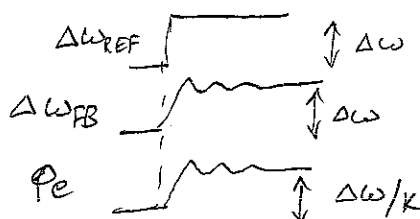
$$\Rightarrow \Delta\omega_{REF}(s) = \frac{\Delta\omega}{s} \quad \Rightarrow \quad \Delta\omega_{out}|_{t \rightarrow \infty} = \lim_{s \rightarrow 0} s A_{CL}(s) \frac{\Delta\omega}{s} = 0$$

$$\& \quad \phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} s A_e(s) \phi_{REF}(s)$$

$$= \lim_{s \rightarrow 0} s A_e(s) \frac{\Delta\omega}{s^2} = \frac{2\zeta}{\omega_n} \Delta\omega = \frac{\Delta\omega}{K}$$

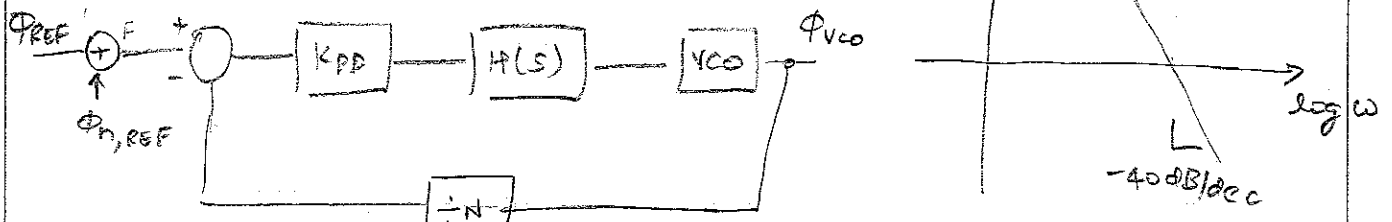
\Rightarrow Type-I PLL tracks an input frequency step with a finite phase error

For small perturbations, loop settles with second-order dynamics:



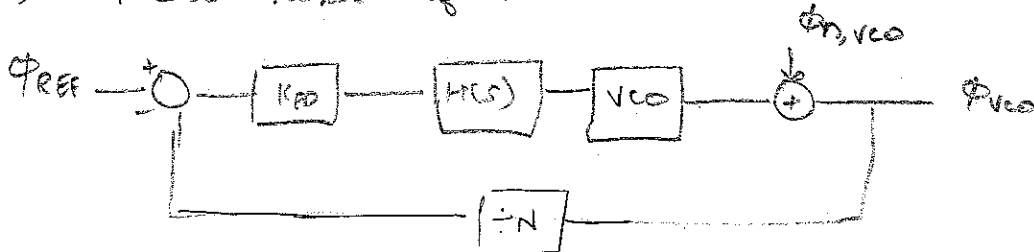
Noise in PLL's:

(a) Phase noise @ input:



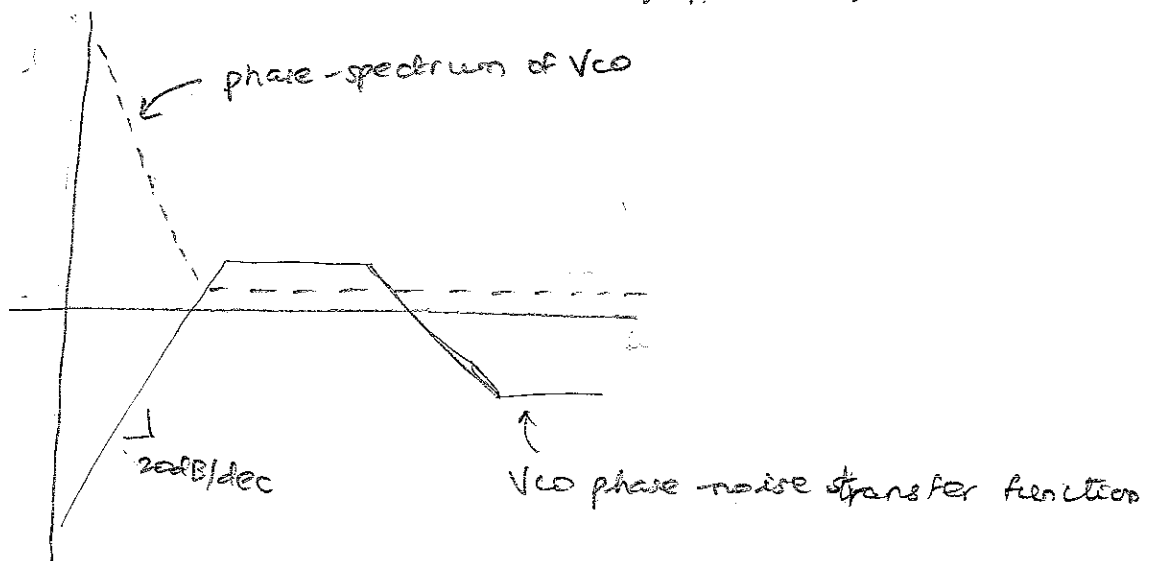
⇒ phase noise @ input is filtered by closed-loop transfer function of PLL.
 ⇒ For high input noise, want low-BW loop filter

(b) Phase noise of VCO



Phase-noise of VCO is shaped by the loop according to the transfer function

$$\frac{\Phi_{VCO}}{\Phi_{n,VCO}}(s) = \frac{1}{1+T(s)} = \frac{s(s+2\zeta\omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$



⇒ VCO phase-noise at small frequency offsets is suppressed by the loop (e.g. $1/s^2$ portion)
 ⇒ If VCO phase noise is large, want wideband loop filter