Program Interference in MLC NAND Flash Memory: Characterization, Modeling, and Mitigation

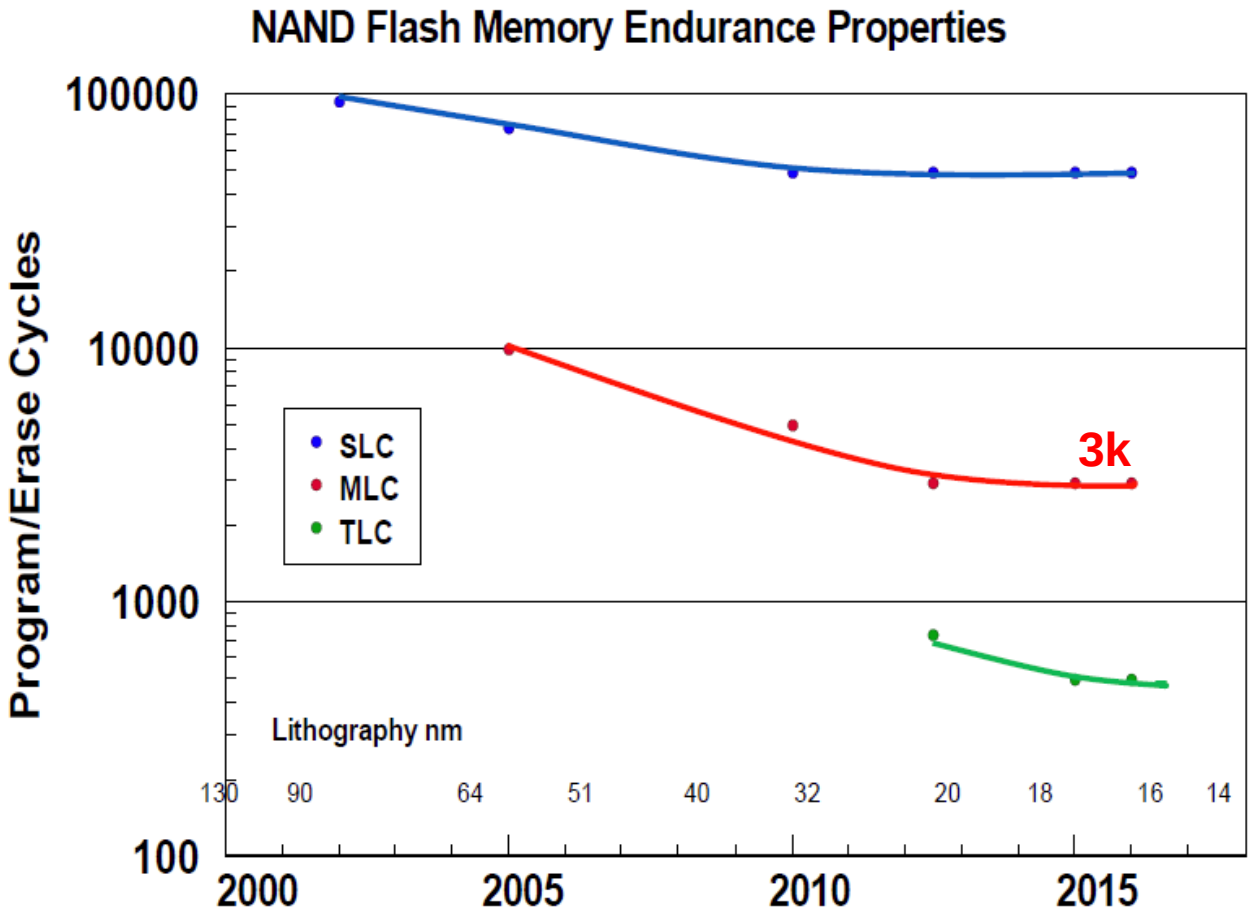
Yu Cai[1] Onur Mutlu[1] Erich F. Haratsch[2] Ken Mai[1]

[1] Carnegie Mellon University
[2] LSI Corporation

SAFARI

Carnegie Mellon

Flash Challenges: Reliability and Endurance



- **P/E cycles (provided)**

  A few thousand

E. Grochowski et al., "Future technology challenges for NAND flash and HDD products", Flash Memory Summit 2012

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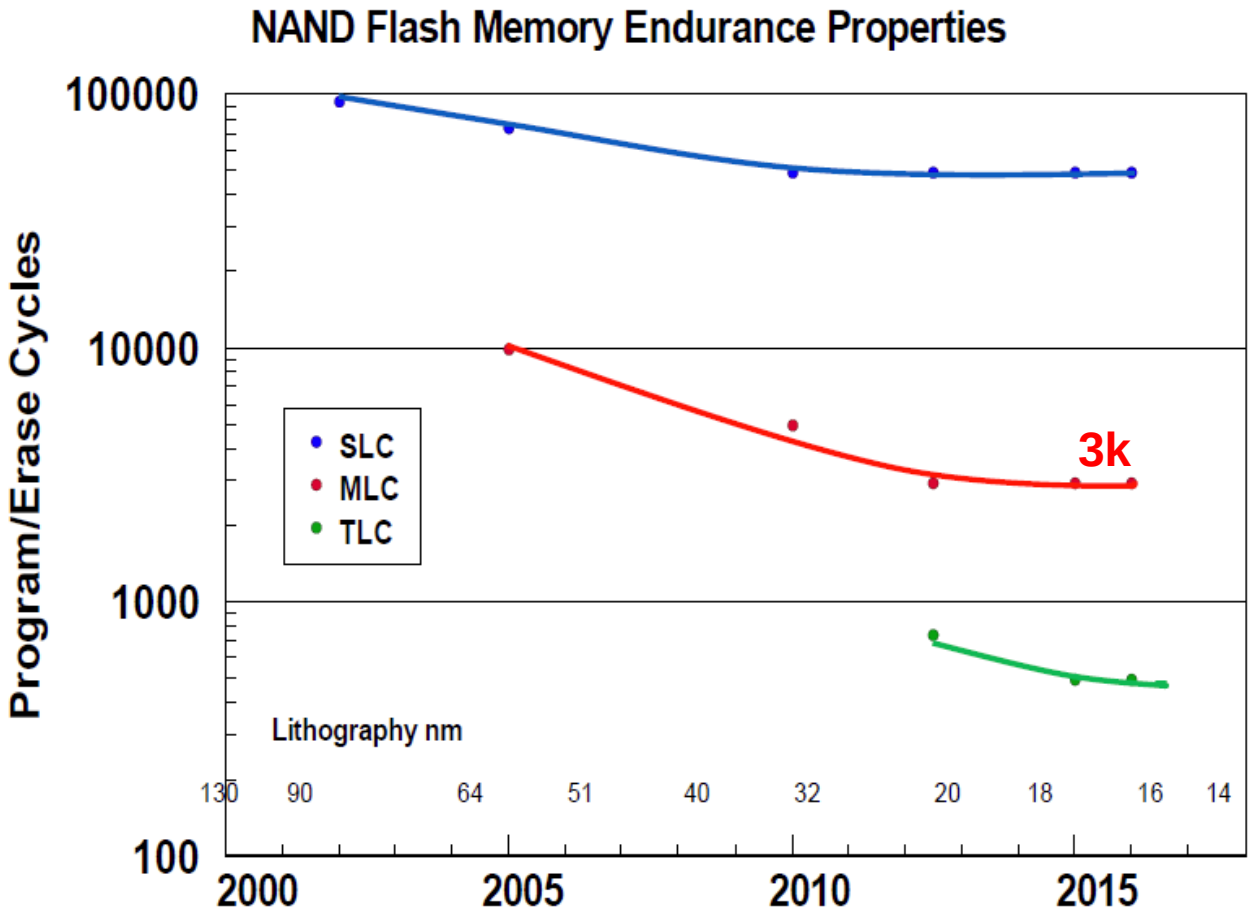

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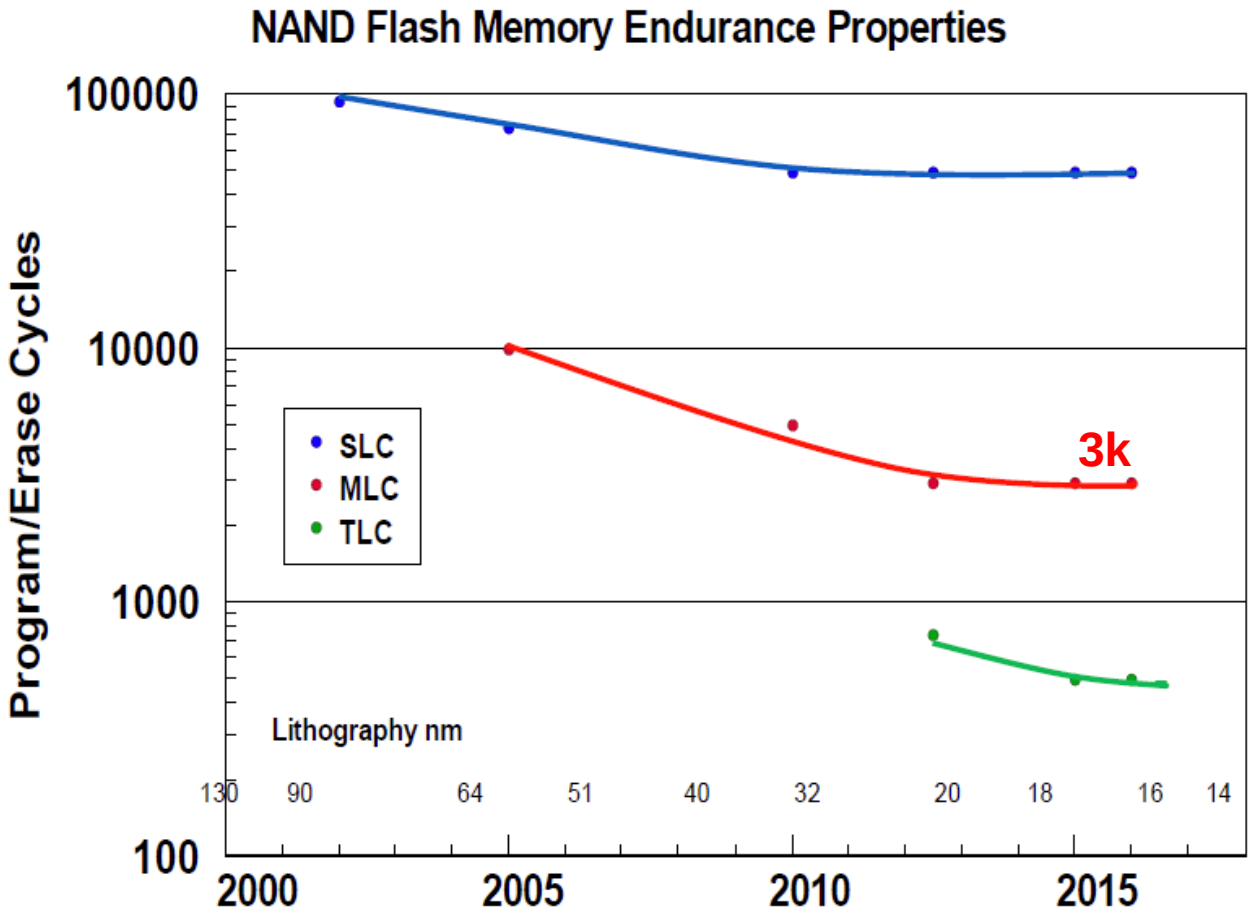

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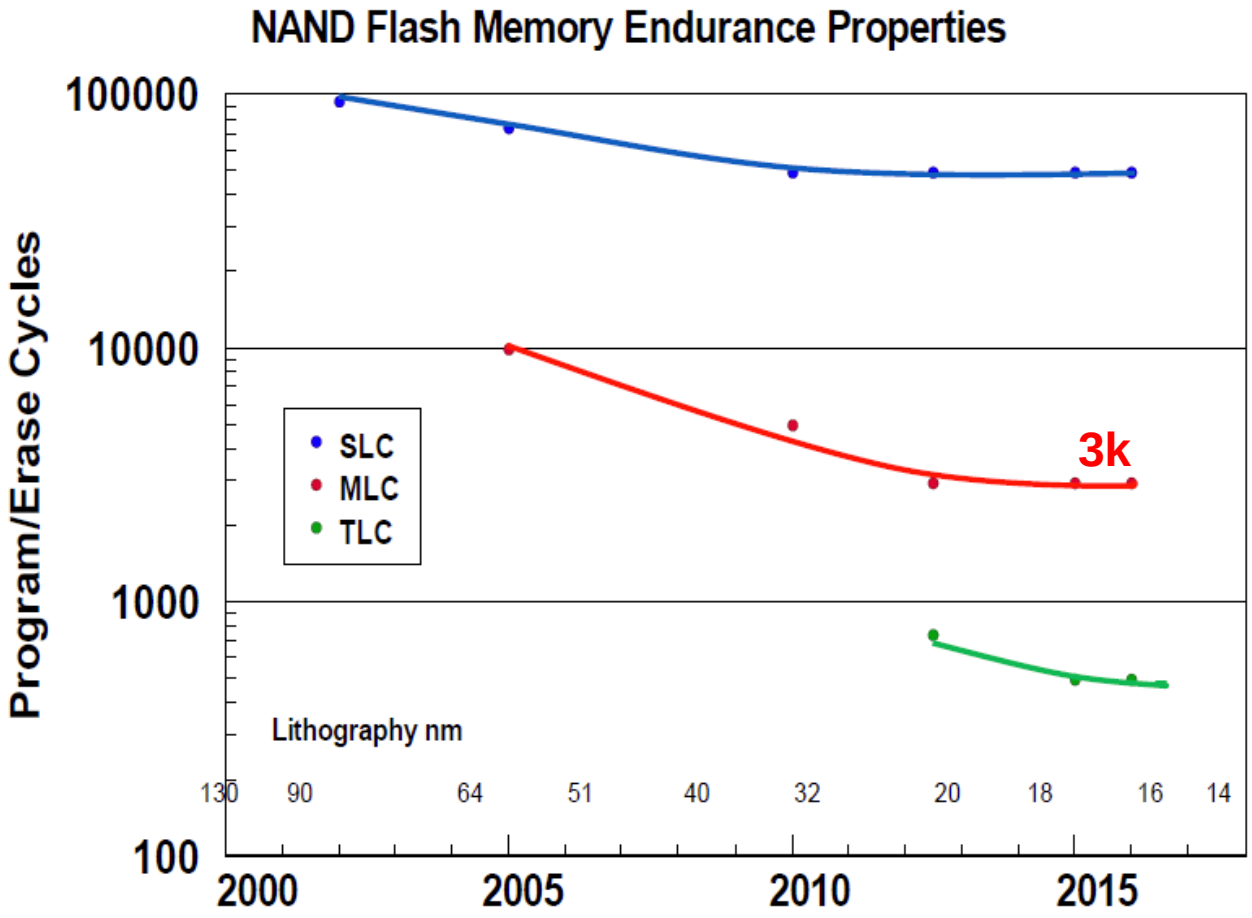

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Our Goals:

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Model NAND Flash as a digital communication channel

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Model NAND Flash as a digital communication channel

Design efficient reliability mechanisms based on the model

NAND Flash Channel Model

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Simplified NAND Flash channel model based on dominant errors

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- **Erase operation**
- **Program page operation**

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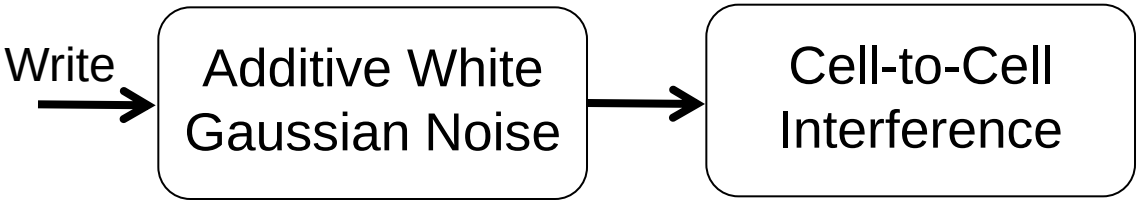

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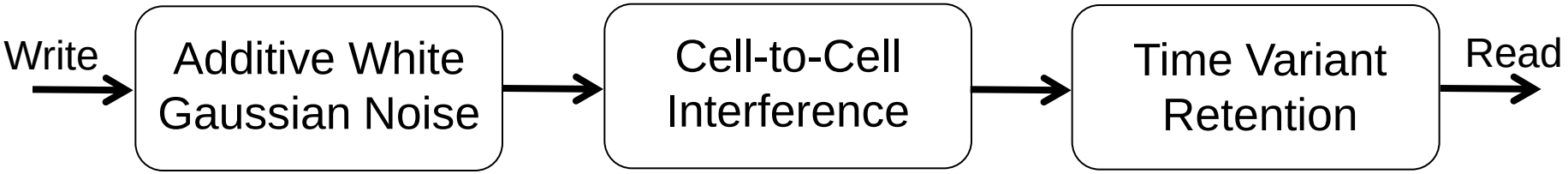

- **Erase operation**
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- **Retention**

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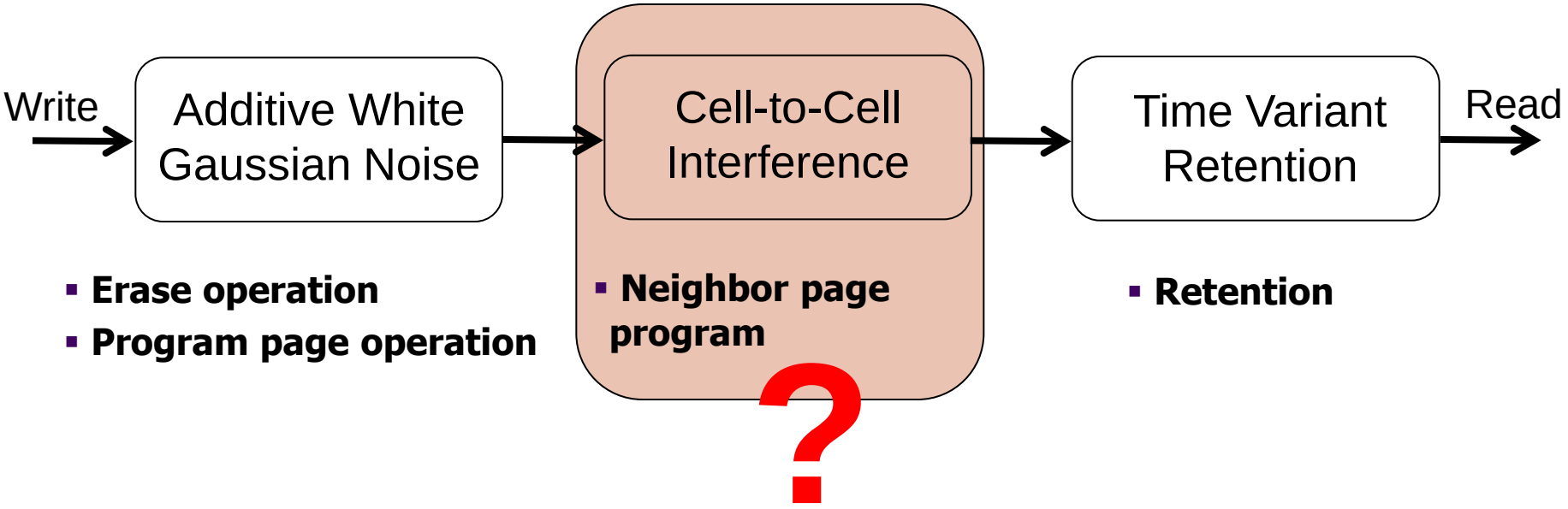
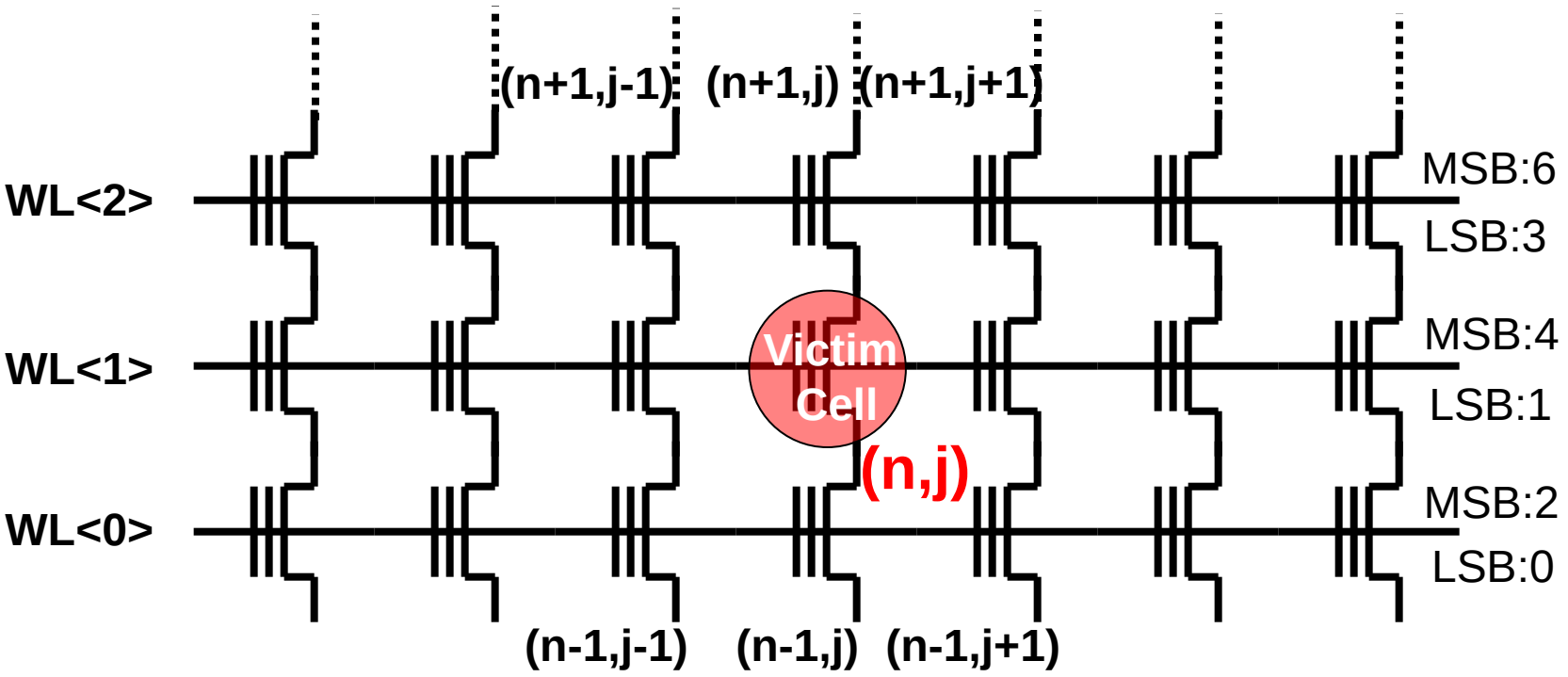


Basics of Program Interference



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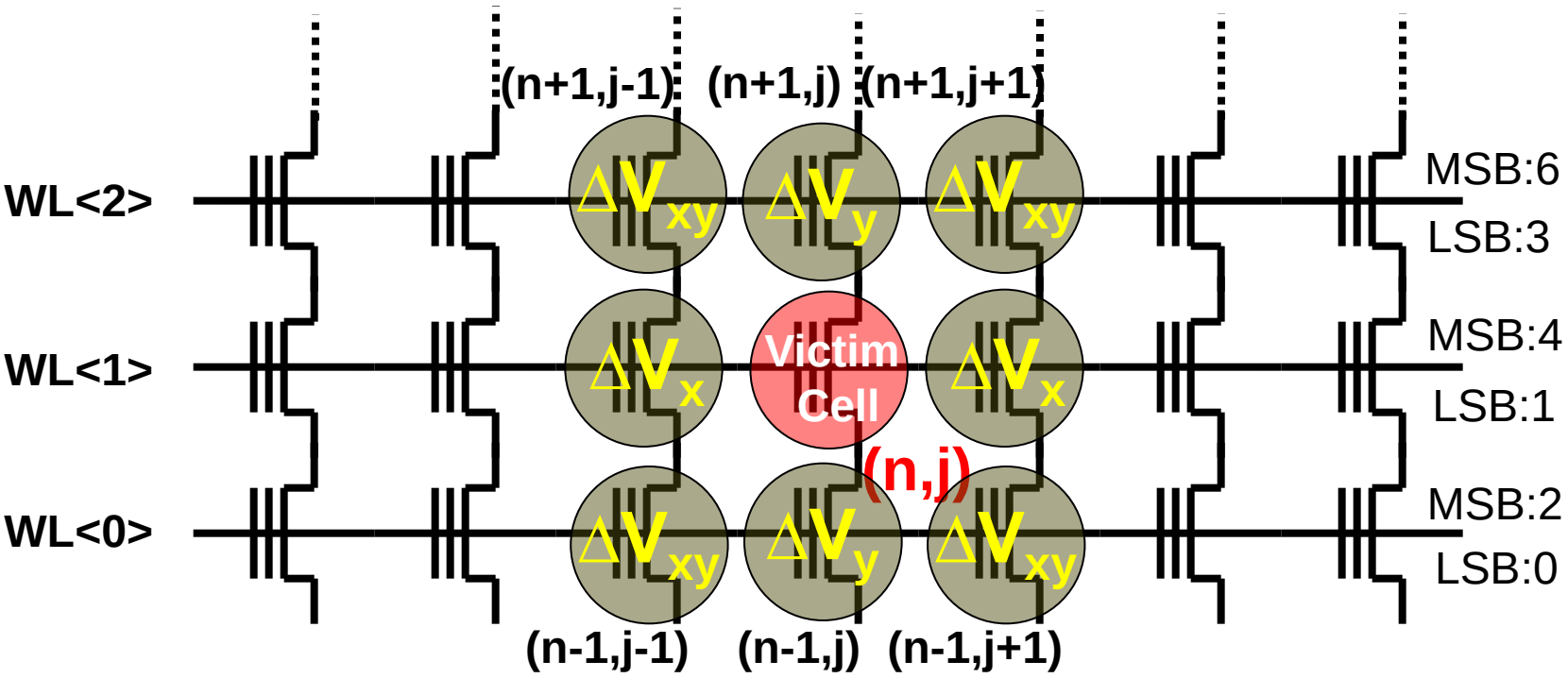

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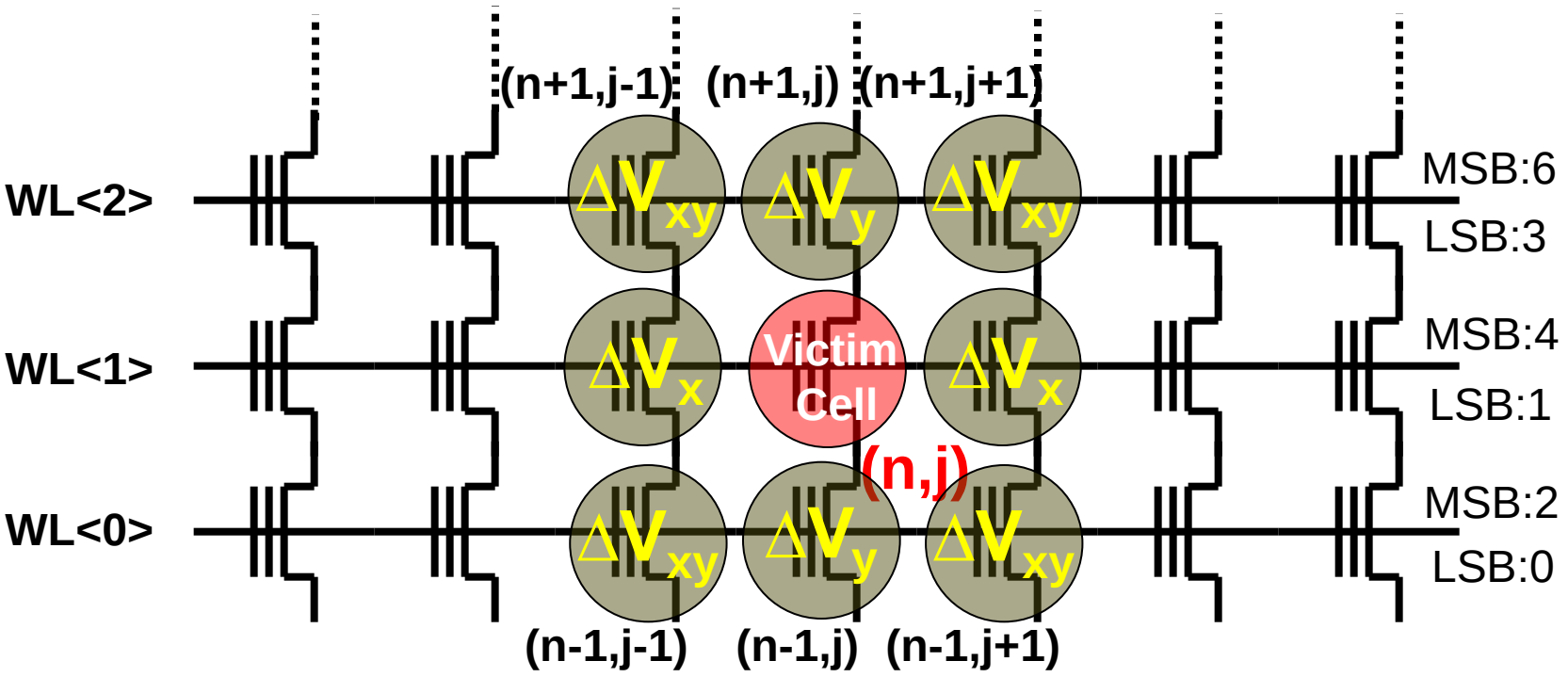

What affects cell-to-cell program interference in Flash chips?

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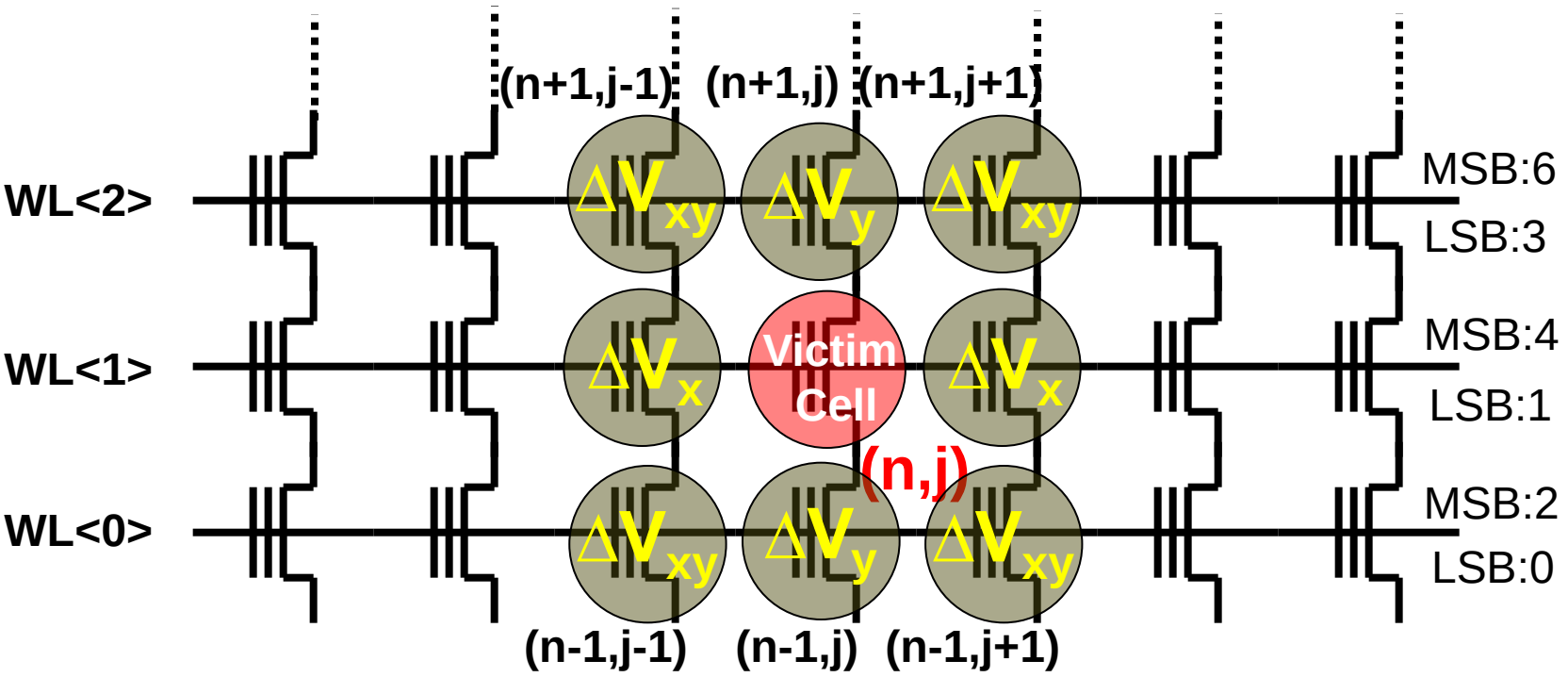

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How to accurately model cell-to-cell program interference?

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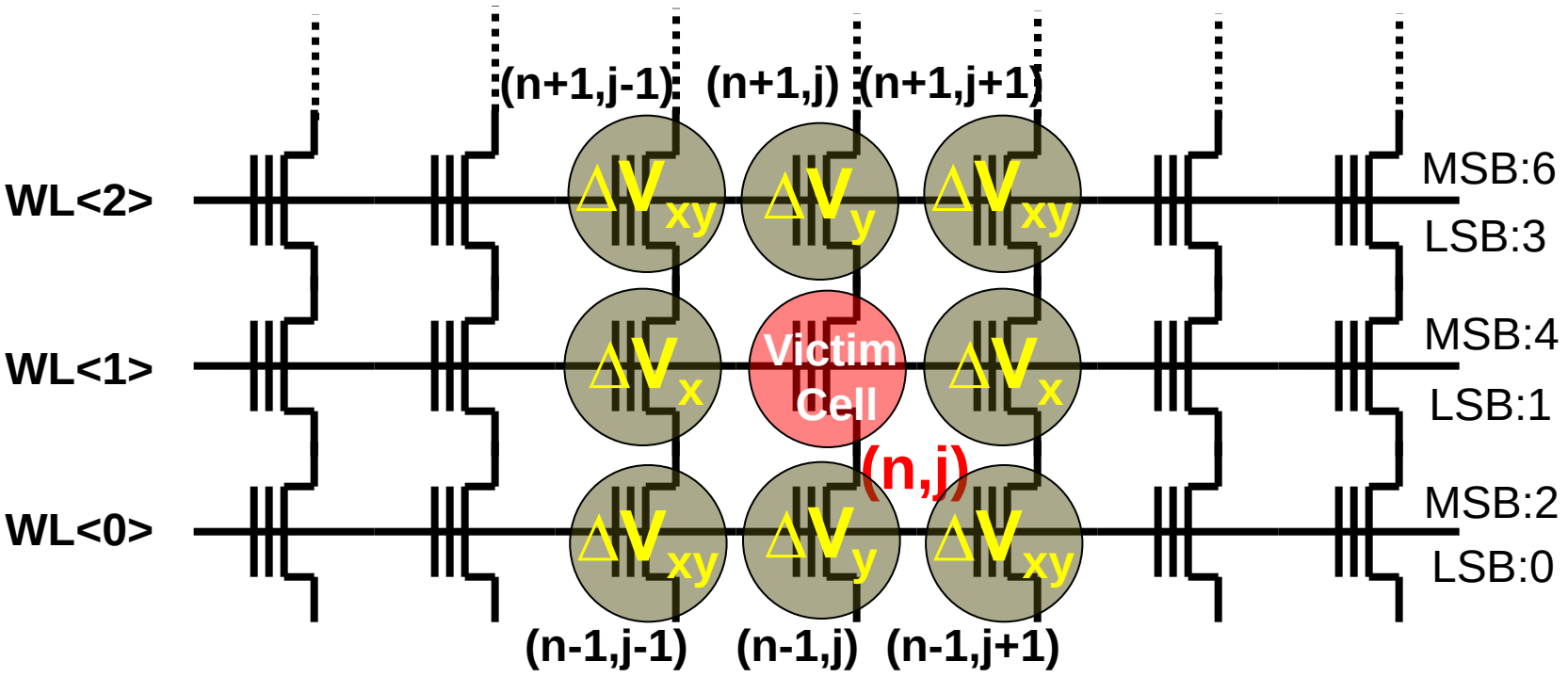

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How to accurately model cell-to-cell program interference?

How to improve flash reliability using the model?

Key Findings and Contributions

- Methodology: Extensive experimentation with real 2Y-nm MLC NAND Flash chips

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- Our new model can predict the amount of program interference with 96.8% prediction accuracy
- Our new read reference voltage prediction technique can improve flash lifetime by 30%

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Today 1:40pm
CSA-2: Memory Systems Session

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