

Onur Mutlu

5000 Forbes Ave., Hamerschlag Hall A305, Pittsburgh, PA 15213
<http://www.ece.cmu.edu/~omutlu>

Work Phone: 412-268-1186
Email: onur@cmu.edu

Research and Teaching Interests

- Computer architecture and systems. Memory systems. Multi/many-core systems. Scalable, QoS-aware, latency-tolerant systems.
- Computer architectures for secure and robust operating systems (OS). OS/architecture interaction.
- Architectural support for safe/managed/parallel programming languages (PL) and programmer productivity. PL/architecture interaction.
- Fault tolerant and bug-tolerant architectures. Dependable systems.
- System-wide resource management and QoS, especially in multi-core/many-core/multithreaded systems.
- Novel computer architectures for health, biology, medical, and bioinformatics applications.

Education

University of Texas at Austin
September 2000 - August 2006

Ph.D., Computer Engineering, August 2006
Dissertation Title: *Efficient Runahead Execution Processors*
Nominated for the ACM Doctoral Dissertation Award by UT-Austin
M.S.E., Computer Engineering, May 2002

University of Michigan, Ann Arbor
September 1997 - August 2000

B.S.E., *summa cum laude*, Computer Engineering, August 2000, GPA: 4.0/4.0
B.S., *with highest distinction*, Psychology, August 2000, GPA: 4.0/4.0

Professional Work Experience

Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Assistant Professor, *January 2009 - Present*
Carnegie Mellon University, Dept. of Computer Science, Courtesy Assistant Professor, *January 2009 - Present*
Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Adjunct Assistant Professor, *July 2008 - January 2009*
Microsoft Research, Computer Architecture Group (Redmond, WA), Researcher, *August 2006 - January 2009*
University of Texas at Austin, Dept. of Electrical and Computer Engineering, Research and Teaching Assistant, *August 2000 - August 2006*
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, *May - August 2005*
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, *May - August 2004*
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, *May - August 2003*
Intel Corporation, Microprocessor Research Labs (Hillsboro, OR), Graduate Technical Intern, *May - August 2002*
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, *May - August 2001*

Awards and Achievements

- Best paper award at ASPLOS 2010
Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems
- Three papers (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2010
Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior
Aergia: Exploiting Packet Latency Slack in On-Chip Networks
Data Marshaling for Multi-core Architectures
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2009
Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures
Architecting Phase Change Memory as a Scalable DRAM Alternative
- One paper (of 12 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2008
Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers
- One paper (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2006
Diverge-Merge Processor (DMP): Generalized and Energy-Efficient Dynamic Predication
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2005
Efficient Runahead Execution: Power-efficient Memory Latency Tolerance
Wish Branches: Enabling Adaptive and Aggressive Predicated Execution
- One paper (of 15 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2003
Runahead Execution: An Effective Alternative to Large Instruction Windows
- One paper selected for CACM's "Research Highlights," 2009
Architecting Phase Change Memory as a Scalable DRAM Alternative
- Best Paper Session at HPCA 2010: *ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers*
- Best Paper Session at HPCA 2009: *Techniques for Bandwidth-Efficient Prefetching of Linked Data Structures in Hybrid Prefetching Systems*
- Best paper award nominations at HPCA 2010, HPCA 2009, HPCA 2007, MICRO 2006, and MICRO 2005 conferences
- Selected to the ISCA and MICRO Halls of Fame, 2009
- NSF CAREER Award, 2010 (*QoS-Aware, High-Performance, and Scalable Many-Core Memory Systems*)
- Microsoft Gold Star Award, 2008

- PhD Dissertation nominated by UT-Austin for the ACM Doctoral Dissertation Award, 2006
- University Co-op/George H. Mitchell Award for Excellence in Graduate Research (Awarded to 6 out of 271 nominees at UT-Austin), 2005
- Intel Foundation Ph.D. Fellowship, 2004
- University of Texas Graduate School Continuing Fellowship, 2003
- University of Michigan EECS Dept. Summer Research Fellowship, 1999, 2000
- University of Michigan EECS Dept. William Harvey Seeley Award (money award given to the top undergraduate junior), 1999
- University of Michigan Branstrom Freshman Prize, 1998
- University of Michigan Angell Scholar (every semester), 1998-2000
- Turkish Government Scholarship for Undergraduate Education in the USA (full tuition + stipend), 1997-2000
- Bilkent University (Ankara, Turkey) Scholarship (full tuition + stipend), 1996-1997
- Ranked 36th (social sciences) and 70th (experimental sciences) out of 1.5 million students in Turkish University Entrance Examinations, 1996

Publications

(Please visit <http://www.ece.cmu.edu/~omutlu/projects.htm> for electronic copies.)

Refereed Conference (and Major Workshop) Publications

1. Chris Fallin, Chris Craik, Onur Mutlu, “CHIPPER: A Low-complexity Bufferless Deflection Router,” *Proceedings of the 17th IEEE International Symposium on High Performance Computer Architecture (HPCA)*, San Antonio, TX, February 2011.
2. Yoongu Kim, Michael Papamichael, Onur Mutlu, and Mor Harchol-Balter, “Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior,” *Proceedings of the 43rd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Atlanta, GA, December 2010. **One of the 11 papers of 2010 selected as “Top Picks” by IEEE Micro**
3. George Nychis, Chris Fallin, Thomas Moscibroda, Onur Mutlu, “Next Generation On-Chip Networks: What Kind of Congestion Control Do We Need?,” *Proceedings of the 9th ACM Workshop on Hot Topics in Networks (HotNETS)*, Monterey, CA, October 2010.
4. Tanausu Ramirez, Alex Pajuelo, Oliverio Santana, Onur Mutlu, and Mateo Valero, “Efficient Runahead Threads,” *Proceedings of the 19th ACM International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Vienna, Austria, September 2010.
5. Reetuparna Das, Onur Mutlu, Thomas Moscibroda, and Chita R. Das, “Aergia: Exploiting Packet Latency Slack in On-Chip Networks,” *Proceedings of the 37th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, St. Malo, France, June 2010. **One of the 11 papers of 2010 selected as “Top Picks” by IEEE Micro**
6. M. Aater Suleman, Onur Mutlu, Jose A. Joao, Khubaib, and Yale N. Patt, “Data Marshaling for Multi-core Architectures,” *Proceedings of the 37th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, St. Malo, France, June 2010. **One of the 11 papers of 2010 selected as “Top Picks” by IEEE Micro**
7. Boris Grot, Steve Keckler, and Onur Mutlu, “Topology-aware Quality-of-Service Support in Highly Integrated Chip Multiprocessors,” *Proceedings of the 6th Annual Workshop on the Interaction between Operating Systems and Computer Architecture (WIOSCA)*, in conjunction with the 37th International Symposium on Computer Architecture, St. Malo, France, June 2010.
8. Paul Bogdan, Miray Kas, Radu Marculescu, and Onur Mutlu, “QuaLe: A Quantum-Leap Inspired Model for Non-Stationary Analysis of NoC Traffic in Multi-Processor Platforms,” *Proceedings of the 4th International Networks-On-Chip Symposium (NOCS)*, May 2010.
9. Yanjing Li, Onur Mutlu, Donald S. Gardner, and Subhasish Mitra, “Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips” *Proceedings of the 28th IEEE VLSI Test Symposium (VTS)*, Santa Cruz, CA, April 2010.
10. Eiman Ebrahimi, Chang Joo Lee, Onur Mutlu, and Yale N. Patt, “Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems,” *Proceedings of the 15th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Pittsburgh, PA, March 2010. **Best Paper Award.**
11. Yoongu Kim, Dongsu Han, Onur Mutlu, and Mor Harchol-Balter, “ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers,” *Proceedings of the 16th IEEE International Conference on High Performance Computer Architecture (HPCA)*, Bangalore, India, January 2010. **Best Paper Session. One of the 4 papers nominated for the Best Paper Award by the Program Committee.**
12. Reetuparna Das, Onur Mutlu, Thomas Moscibroda, and Chita R. Das, “Application-Aware Prioritization Mechanisms for On-Chip Networks,” *Proceedings of the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York, NY, pp. 280-291, December 2009.
13. Eiman Ebrahimi, Onur Mutlu, Chang Joo Lee, and Yale N. Patt, “Coordinated Control of Multiple Prefetchers in Multi-Core Systems,” *Proceedings of the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York, NY, pp. 316-326, December 2009.
14. Boris Grot, Steve Keckler, and Onur Mutlu, “Preemptive Virtual Clock: A Flexible, Efficient, and Cost-effective QOS Scheme for Networks-on-Chip,” *Proceedings of the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York, NY, pp. 268-279, December 2009.
15. Chang Joo Lee, Veynu Narasiman, Onur Mutlu, and Yale N. Patt, “Improving Memory Bank-Level Parallelism in the Presence of Prefetching,” *Proceedings of the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York, NY, pp. 327-336, December 2009.

16. Yanjing Li, Onur Mutlu, and Subhasish Mitra, "Operating System Scheduling for Efficient Online Self-Test in Robust Systems," *Proceedings of the 2009 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 201-208, November 2009.
17. Thomas Moscibroda and Onur Mutlu, "A Case for Bufferless Routing in On-Chip Networks," *Proceedings of the 36th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 196-207, Austin, TX, June 2009.
18. José A. Joao, Onur Mutlu, and Yale N. Patt, "Flexible Reference Counting Based Hardware Acceleration for Garbage Collection," *Proceedings of the 36th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 418-428, Austin, TX, June 2009.
19. Benjamin Lee, Engin Ipek, Onur Mutlu, and Doug Burger, "Architecting Phase Change Memory as a Scalable DRAM Alternative," *Proceedings of the 36th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 2-13, Austin, TX, June 2009. **One of the 13 papers of 2009 selected as "Top Picks" by IEEE Micro. Opening Paper of the Conference. Selected for publication in CACM Research Highlights.**
20. M. Aater Suleman, Onur Mutlu, Moinuddin Qureshi, Yale N. Patt, "Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures," *Proceedings of the 14th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 253-264, Washington, DC, March 2009. **One of the 13 papers of 2009 selected as "Top Picks" by IEEE Micro**
21. Eiman Ebrahimi, Onur Mutlu, Yale N. Patt, "Techniques for Bandwidth-Efficient Prefetching of Linked Data Structures in Hybrid Prefetching Systems," *Proceedings of the 15th IEEE International Conference on High Performance Computer Architecture (HPCA)*, pp. 7-17, Raleigh, NC, February 2009. **Best Paper Session. One of the 3 papers nominated for the Best Paper Award by the Program Committee**
22. Boris Grot, Joel Hestness, Steve Keckler, Onur Mutlu, "Express Cube Topologies for On-Chip Interconnects," *Proceedings of the 15th IEEE International Conference on High Performance Computer Architecture (HPCA)*, pp. 163-174, Raleigh, NC, February 2009.
23. Kypros Constantinides, Onur Mutlu, Todd Austin, "Online Design Bug Detection: RTL Analysis, Flexible Mechanisms, and Evaluation," *Proceedings of the 41st IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 282-293, Lake Como, Italy, November 2008.
24. Chang Joo Lee, Onur Mutlu, Veynu Narasiman, Yale N. Patt, "Prefetch Aware DRAM Controllers," *Proceedings of the 41st IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 200-209, Lake Como, Italy, November 2008.
25. Thomas Moscibroda and Onur Mutlu, "Distributed Order Scheduling and its Application to Multi-Core DRAM Controllers," *Proceedings of the 27th Annual ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC)*, pp. 365-374, Toronto, Canada, August 2008.
26. Onur Mutlu and Thomas Moscibroda, "Parallelism-Aware Batch Scheduling: Enhancing both Performance and Fairness of Shared DRAM Systems," *Proceedings of the 35th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 63-74, Beijing, China, June 2008. **One of the 12 papers of 2008 selected as "Top Picks" by IEEE Micro**
27. Engin Ipek, Onur Mutlu, José F. Martínez, Rich Caruana, "Self-Optimizing Memory Controllers: A Reinforcement Learning Approach," *Proceedings of the 35th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 39-50, Beijing, China, June 2008.
28. José A. Joao, Onur Mutlu, Hyesoon Kim, Rishi Agarwal, Yale N. Patt, "Improving the Performance of Object-Oriented Languages with Dynamic Predication of Indirect Jumps," *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 80-90, Seattle, WA, March 2008.
29. Chang Joo Lee, Hyesoon Kim, Onur Mutlu, Yale N. Patt, "Performance-aware Speculation Control using Wrong Path Usefulness Prediction," *Proceedings of the 14th IEEE International Conference on High Performance Computer Architecture (HPCA)*, pp. 39-49, Salt Lake City, UT, February 2008.
30. Onur Mutlu and Thomas Moscibroda, "Stall-Time Fair Memory Access Scheduling for Chip Multiprocessors," *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 146-158, Chicago, IL, December 2007.
31. Kypros Constantinides, Onur Mutlu, Todd Austin, and Valeria Bertacco, "Software-Based Online Detection of Hardware Defects: Mechanisms, Architectural Support, and Evaluation," *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 97-108, Chicago, IL, December 2007.
32. Thomas Moscibroda and Onur Mutlu, "Memory Performance Attacks: Denial of Memory Service in Multi-Core Systems," *Proceedings of the 16th USENIX Security Symposium (USENIX SECURITY)*, pp. 257-274, Boston, MA, August 2007.
33. Hyesoon Kim, José A. Joao, Onur Mutlu, Chang Joo Lee, Yale N. Patt, Robert S. Cohn, "VPC Prediction: Reducing the Cost of Indirect Branches via Hardware-based Dynamic Devirtualization," *Proceedings of the 34th IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 424-435, San Diego, CA, June 2007.
34. Hyesoon Kim, José A. Joao, Onur Mutlu, Yale N. Patt, "Profile-assisted Compiler Support for Dynamic Predication in Diverge-Merge Processors," *Proceedings of the 5th Annual International Symposium on Code Generation and Optimization (CGO)*, pp. 367-378, San Jose, CA, March 2007.
35. Santhosh Srinath, Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Feedback Directed Prefetching: Improving the Performance and Bandwidth-Efficiency of Hardware Prefetchers," *Proceedings of the 13th IEEE International Conference on High Performance Computer Architecture (HPCA)*, pp. 63-74, Phoenix, AZ, February 2007. **One of the 5 papers nominated for the Best Paper Award by the Program Committee**

36. Hyesoon Kim, José Joao, Onur Mutlu, Yale N. Patt, “Diverge-Merge Processor (DMP): Dynamic Predicated Execution of Complex Control-Flow Graphs Based on Frequently Executed Paths,” *Proceedings of the 38th IEEE/ACM Annual International Symposium on Microarchitecture (MICRO)*, pp. 53-64, Orlando, FL, December 2006. **One of the 11 papers of 2006 selected as “Top Picks” by IEEE Micro**
37. Moinuddin K. Qureshi, Daniel N. Lynch, Onur Mutlu, Yale N. Patt, “A Case for MLP-Aware Cache Replacement,” *Proceedings of the 33rd IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 167-177, Boston, MA, USA, June 2006.
38. Hyesoon Kim, M. Aater Suleman, Onur Mutlu, Yale N. Patt, “2D-Profiling: Detecting Input-Dependent Branches with a Single Input Data Set,” *Proceedings of the 4th Annual International Symposium on Code Generation and Optimization (CGO)*, pp. 159-169, New York, NY, USA, March 2006.
39. Onur Mutlu, Hyesoon Kim, Yale N. Patt, “Address-Value Delta (AVD) Prediction: Increasing the Effectiveness of Runahead Execution by Exploiting Regular Memory Allocation Patterns,” *Proceedings of the 38th IEEE/ACM Annual International Symposium on Microarchitecture (MICRO)*, pp. 233-244, Barcelona, Spain, November 2005. **One of the 5 papers nominated for the Best Paper Award by the Program Committee**
40. Hyesoon Kim, Onur Mutlu, Jared Stark, Yale N. Patt, “Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution,” *Proceedings of the 38th IEEE/ACM Annual International Symposium on Microarchitecture (MICRO)*, pp. 43-54, Barcelona, Spain, November 2005. **One of the 13 papers of 2005 selected as “Top Picks” by IEEE Micro**
41. Onur Mutlu, Hyesoon Kim, Yale N. Patt, “Techniques for Efficient Processing in Runahead Execution Engines,” *Proceedings of the 32nd IEEE/ACM International Symposium on Computer Architecture (ISCA)*, pp. 370-381, Madison, WI, USA, June 2005. **One of the 13 papers of 2005 selected as “Top Picks” by IEEE Micro**
42. Moinuddin K. Qureshi, Onur Mutlu, and Yale N. Patt, “Microarchitecture-Based Introspection: A Technique for Transient-Fault Tolerance in Microprocessors,” *Proceedings of the 2005 IEEE International Conference on Dependable Systems and Networks (DSN)*, pp. 434-443, Yokohama, Japan, June 2005.
43. David N. Armstrong, Hyesoon Kim, Onur Mutlu, Yale N. Patt, “Wrong Path Events: Exploiting Unusual and Illegal Program Behavior for Early Misprediction Detection and Recovery,” *Proceedings of the 37th IEEE/ACM Annual International Symposium on Microarchitecture (MICRO)*, pp. 119-128, Portland, OR, USA, December 2004.
44. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, “Cache Filtering Techniques to Reduce the Negative Impact of Useless Speculative Memory References on Processor Performance,” *Proceedings of the 16th IEEE International Symposium on Computer Architecture and High Performance Computing*, pp. 2-9, Foz do Iguacu, Brazil, October 2004. **Opening Paper of the Conference.**
45. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, “Understanding The Effects of Wrong-Path Memory References on Processor Performance,” *Proceedings of the 3rd ACM Workshop on Memory Performance Issues (WMPI), in conjunction with the 31st International Symposium on Computer Architecture*, pp. 56-64, Munchen, Germany, June 2004.
46. Onur Mutlu, Jared Stark, Chris Wilkerson, Yale N. Patt, “Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors,” *Proceedings of the 9th IEEE International Conference on High Performance Computer Architecture (HPCA)*, pp. 129-140, Anaheim, CA, USA, February 2003. **One of the 15 papers of 2003 selected as “Top Picks” by IEEE Micro**

Refereed Journal Publications

47. Yoongu Kim, Michael Papamichael, Onur Mutlu, and Mor Harchol-Balter, “Thread Cluster Memory Scheduling,” *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 31 (1), January/February 2011.
48. Reetuparna Das, Onur Mutlu, Thomas Moscibroda, and Chita R. Das, “Aergia: A Network-On-Chip Exploiting Packet Latency Slack,” *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 31 (1), January/February 2011.
49. M. Aater Suleman, Onur Mutlu, Jose A. Joao, Khubaib, and Yale N. Patt, “Data Marshaling for Multi-core Systems,” *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 31 (1), January/February 2011.
50. Benjamin Lee, Engin Ipek, Onur Mutlu, Doug Burger, “Phase Change Memory Architecture and the Quest for Scalability,” *Communications of the ACM (CACM)*, Research Highlight, vol. 53 (7), pp. 99-106, July 2010.
51. Chang Joo Lee, Onur Mutlu, Veynu Narasiman, and Yale N. Patt, “Prefetch-Aware Memory Controllers,” accepted to *IEEE Transactions on Computers*, publication pending, June 2010.
52. M. Aater Suleman, Onur Mutlu, Moinuddin Qureshi, Yale N. Patt, “Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures,” *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 30 (1), pp. 131-141, January/February 2010.
53. Benjamin Lee, Ping Zhou, Jun Yang, Youtao Zhang, Bo Zhao, Engin Ipek, Onur Mutlu, Doug Burger, “Phase Change Technology and the Future of Main Memory,” *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 30 (1), pp. 60-70, January/February 2010.
54. Can Alkan, Jeffrey M. Kidd, Tomas Marques-Bonet, Gozde Aksay, Francesca Antonacci, Fereydoun Hormozdiari, Jacob O. Kitzman, Carl Baker, Maika Malig, Onur Mutlu, S. Cenk Sahinalp, Richard A. Gibbs, Evan E. Eichler, “Personalized Copy-Number and Segmental Duplication Maps using Next-Generation Sequencing,” *Nature Genetics*, [Epub: August 30], vol. 41 (10), pp. 1061-1067, October 2009.
55. Hyesoon Kim, José A. Joao, Onur Mutlu, Chang Joo Lee, Yale N. Patt, Robert S. Cohn, “Virtual Program Counter (VPC) Prediction: Very Low-Cost Indirect Branch Prediction using Conditional Branch Prediction Hardware,” *IEEE Transactions on Computers (TC)*, vol. 58 (9), pp. 1153-1170, September 2009. **Online featured article.**

56. Kypros Constantinides, Onur Mutlu, Todd Austin, and Valeria Bertacco, "A Flexible Software-Based Framework for Online Detection of Hardware Defects," *IEEE Transactions on Computers (TC)*, vol. 58 (8), pp. 1063-1079, August 2009.
57. Onur Mutlu and Thomas Moscibroda, "Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers," *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 28(1), January/February 2009.
58. José A. Joao, Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Dynamic Predication of Indirect Jumps," *IEEE Computer Architecture Letters (CAL)*, vol. 6, May 2007.
59. Hyesoon Kim, José A. Joao, Onur Mutlu, Yale N. Patt, "Diverge-Merge Processor: Generalized and Energy-Efficient Dynamic Predication," *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 27(1), pp. 94-104, January/February 2007.
60. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Address-Value Delta (AVD) Prediction: A Hardware Technique for Efficiently Parallelizing Dependent Cache Misses," *IEEE Transactions on Computers (TC)*, vol. 55 (12), pp. 1491-1508, December 2006. **Featured article.**
61. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Efficient Runahead Execution: Power-Efficient Memory Latency Tolerance," *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 26(1), pp. 10-20, January/February 2006.
62. Hyesoon Kim, Onur Mutlu, Jared Stark, Yale N. Patt, "Wish Branches: Enabling Adaptive and Aggressive Predicated Execution," *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 26(1), pp. 48-58, January/February 2006.
63. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "An Analysis of the Performance Impact of Wrong-Path Memory References on Out-of-Order and Runahead Execution Processors," *IEEE Transactions on Computers (TC)*, vol. 54 (12), pp. 1556-1571, December 2005.
64. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "Using the First-Level Caches as Filters to Reduce the Pollution Caused by Speculative Memory References," *International Journal of Parallel Programming (IJPP)*, vol. 33 (5), pp. 529-559, October 2005.
65. Onur Mutlu, Hyesoon Kim, Jared Stark, Yale N. Patt, "On Reusing the Results of Pre-Executed Instructions in a Runahead Execution Processor," *IEEE Computer Architecture Letters (CAL)*, vol. 4, January 2005.
66. Onur Mutlu, Jared Stark, Chris Wilkerson, Yale N. Patt, "Runahead Execution: An Effective Alternative to Large Instruction Windows," *IEEE Micro, Special Issue: Top Picks from Computer Architecture Conferences (TOP PICKS)*, vol. 23(6), pp. 20-25, November/December 2003.

Editorial Articles

67. Yale N. Patt, Onur Mutlu, "Guest Editor's Introduction: Top Picks," *IEEE Micro, Special Issue (IEEE MICRO)*, vol. 31(1), January/February 2011.
68. Sangyeun Cho, Tao Li, Onur Mutlu, "Interaction of Many-core Computer Architecture and Operating Systems: Guest Editors' Introduction," *IEEE Micro, Special Issue (IEEE MICRO)*, vol. 28(3), pp. 2-5, May/June 2008.

Significant Technical Reports (otherwise unpublished)

69. Veynu Narasiman, Chang Joo Lee, Michael Shebanow, Rustam Miftakhutdinov, Onur Mutlu, Yale N. Patt, "Improving GPU Performance via Large Warps and Two-Level Warp Scheduling," HPS Technical Report, TR-HPS-2010-006, December 2010.
70. Eiman Ebrahimi, Chang Joo Lee, Onur Mutlu, Yale N. Patt, "Prefetch-Aware Shared-Resource Management for Multi-Core Systems," HPS Technical Report, TR-HPS-2010-005, December 2010.
71. Chang Joo Lee, Eiman Ebrahimi, Veynu Narasiman, Onur Mutlu, Yale N. Patt, "DRAM-Aware Last-Level Cache Replacement," HPS Technical Report, TR-HPS-2010-007, December 2010.
72. Chang Joo Lee, Veynu Narasiman, Eiman Ebrahimi, Onur Mutlu, Yale N. Patt, "DRAM-Aware Last-Level Cache Writeback: Reducing Write-Caused Interference in Memory Systems," HPS Technical Report, TR-HPS-2010-002, April 2010.
73. Onur Mutlu, "Efficient Runahead Execution Processors," Ph.D. Dissertation, HPS Technical Report, TR-HPS-2006-007, July 2006. **Nominated for the ACM Doctoral Dissertation Award by the University of Texas at Austin**

Patents and Invention Disclosures (filed while in Industry)

1. Thomas Moscibroda, Onur Mutlu, "Bufferless Routing in On-Chip Interconnection Networks," US Patent application filed January 2009.
2. Thomas Moscibroda, Onur Mutlu, "Prioritization of Multiple Concurrent Threads for Scheduling Requests to Shared Memory," US Patent application filed October 2008.
3. Thomas Moscibroda, Onur Mutlu, "Coordination Mechanisms among Multiple Memory Controllers for Reducing Energy Consumption," US Patent application filed March 2008.
4. Thomas Moscibroda, Onur Mutlu, "Controlling Interference in Shared DRAM Systems using Batch Scheduling," US Patent Application filed February 2008.
5. Onur Mutlu, José A. Joao, "Feedback Mechanism for Dynamic Predication of Indirect Jumps," US Patent Application filed December 2007.
6. José A. Joao, Onur Mutlu, "Target-Frequency based Indirect Jump Prediction for High-Performance Processors," US Patent Application filed December 2007.

7. Onur Mutlu, Thomas Moscibroda, “A Software-Configurable and Stall-Time Fair Memory Access Scheduling Mechanism for Shared Memory Systems,” US Patent Application filed November 2007.
8. Thomas Moscibroda, Onur Mutlu, “Multi-level DRAM Controller to Manage Access to DRAM,” US Patent Application filed August 2007.
9. Onur Mutlu, Thomas Moscibroda, “Parallelism-Aware Memory Request Scheduling in Shared Memory Controllers,” US Patent Application filed August 2007.
10. Thomas Moscibroda, Onur Mutlu, “Fairness in Memory Systems,” US Patent Application filed July 2007.
11. Jared Stark, Chris Wilkerson, Onur Mutlu, “Apparatus for Memory Communication During Runahead Execution,” US Patent Application filed December 2002.
12. Eric Sprangle, Onur Mutlu, “Method and Apparatus to Control Memory Accesses,” US Patent number 6,799,257 (September 28, 2004). Assignee: Intel Corporation.

Invited Talks and Lectures

1. “PCM (NVM) as Main Memory: Opportunities and Challenges”
 - Carnegie Mellon University, Parallel Data Lab Retreat, Pittsburgh, PA, October 25, 2010.
2. “Research Challenges in Future Computing Platforms”
 - Carnegie Mellon University, ECE Department Faculty Retreat, Wheeling, WV, August 12, 2010.
3. “Multi-core Architectures and Shared Resource Management: Fundamentals and Recent Research”
 - Seoul National University, Lecture Series (12 hours), Seoul, Korea, July 6-9, 2010.
 - Korea Advanced Institute of Science and Technology, Global Lecture Series (15 hours), Daejeon, Korea, July 26-29, 2010.
4. “End-to-end QoS-aware, High-Performance and Customizable Many-Core Memory Systems”
 - Intel Memory Hierarchy Meeting, Hillsboro, OR, 8 October 2010.
5. “Rethinking Core Design in the Power-Constrained Many-Core Era”
 - Intel Core Workshop, Hillsboro, OR, 27 September 2010.
6. “Some Ideas for ILP Research”
 - CRA Workshop on Advancing Computer Architecture Research, Seattle, WA, 20 September 2010.
7. “Designing High-Performance and Fair Shared Multi-core Memory Systems: Two Approaches” or “QoS-Aware Multi-Core Memory System Management”
 - Gigascale Systems Research Center E-Seminar, 23 March 2010.
 - Pennsylvania State University, CSE Colloquium, 26 March 2010.
 - ARM, Inc., Austin, TX, 8 April 2010.
 - Advanced Micro Devices, Austin, TX, 9 April 2010.
 - Microsoft Research, Redmond, WA, 27 April 2010.
 - HP Laboratories, Palo Alto, CA, 25 May 2010.
 - VMware, Palo Alto, CA, 26 May 2010.
 - Intel Corporation, Hillsboro, OR, 27 May 2010.
 - Gigascale Systems Research Center Annual Review, San Jose, CA, 29 September 2010.
 - Intel Corporation ArchFest, Hillsboro, OR, 8 October 2010.
 - ASPLOS 2011 Program Committee Symposium, Pittsburgh, PA, 22 October 2010.
8. “Rethinking Memory System Design in the Nanoscale Many-Core Era”
 - Intel Memory Hierarchy Workshop, Hillsboro, OR, 22 January 2010.
 - ASPLOS Workshop on Architecting Memory Technologies, Pittsburgh, PA, 14 March 2010.
9. “Asymmetry Everywhere (with Automatic Resource Management)”
 - CRA Workshop on Advancing Computer Architecture Research, San Diego, CA, 22 February 2010.
10. “Preventing Memory Performance Attacks in Multi-Core Systems”
 - ECE Seminar, Carnegie Mellon University, 5 February 2009.
 - Massachusetts Institute of Technology, 23 April 2008.
 - Carnegie Mellon University, 15 April 2008.
11. “Parallelism-aware Batch Scheduling: Enhancing both Performance and Fairness of Shared DRAM Systems”
 - IBM Austin Research Laboratory, Austin, TX, 19 June 2009.
 - Advanced Micro Devices Research Lab, Redmond, WA, 6 March 2009.
 - Beihang University, Beijing, China, 21 June 2008.
12. “ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers”
 - Advanced Micro Devices Research Lab, Redmond, WA, October 2009.
 - Freescale Semiconductor, Austin, TX, 8 April 2010.
13. “Memory Performance Attacks and Fair Memory Scheduling”
 - University of British Columbia and IEEE Computer Society, Vancouver, BC, Canada, 6 March 2008.
 - ASPLOS PC Meeting Research Seminar, Microsoft Research, 18 October 2007.
 - Multi-Core Virtual Team Meeting, Microsoft, 5 October 2007.
14. “MSR Computer Architecture Group: Vision and Projects”

- Presentation to Rico Malvar, MSR-Redmond Director, Microsoft Research, 12 December 2007.
15. “Hardware-Based Devirtualization of Virtual Function Calls”
 - MSR Systems and Networking Seminar, Microsoft Research, 7 December 2006.
 16. “Runahead Execution and AVD Prediction: A Power-efficient Processing Paradigm for Tolerating Long Main Memory Latencies”
 - University of Illinois Urbana-Champaign, Computer Engineering Seminar, Urbana, IL, USA, 23 January 2007.
 - Xilinx Labs, San Jose, CA, USA, 16 June 2006.
 - Microsoft Research, Redmond, WA, USA, 12 June 2006.
 - Stanford University, Department of EE, Computer Architecture Seminar, Stanford, CA, USA, 7 June 2006.
 - MIPS Technologies, Mountain View, CA, USA, 6 June 2006.
 - IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, 1 June 2006.
 - Carnegie Mellon University, Department of ECE, CALCM Seminar, Pittsburgh, PA, USA, 30 May 2006.
 - Hewlett-Packard Laboratories, Palo Alto, CA, USA, 4 May 2006.
 - University of California, San Diego, Department of Computer Science and Engineering, CA, USA, 21 April 2006.
 - University of Texas at Austin, Department of ECE, Guest Lecture for EE382N (Microarchitecture), 11-12 April 2006.
 17. “Efficient Runahead Execution”
 - Advanced Micro Devices, Sunnyvale, CA, USA, May 2005.
 - Intel Barcelona Research Center, Barcelona, Spain, November 2005.
 18. “Runahead Execution”
 - Advanced Micro Devices, Sunnyvale, CA, USA, May 2004.
 - Instituto de Informatica, Universidade Federal Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, October 2004.
 19. “Runahead Execution: A Mechanism to Approximate the Performance of Large Instruction Windows”
 - Enterprise Platforms Group, Intel Corporation, Santa Clara, CA, USA, August 2002.
 - Desktop Platforms Group, Intel Corporation, Hillsboro, OR, USA, August 2002.

Conference Talks

20. “Data Marshaling for Multi-core Architectures,” *37th International Symposium on Computer Architecture*, St. Malo, France, June 2010.
21. “Parallelism-aware Batch Scheduling: Enhancing both Performance and Fairness of Shared DRAM Systems,” *35th International Symposium on Computer Architecture*, Beijing, China, June 2008.
22. “Stall-Time Fair Memory Access Scheduling,” *40th International Symposium on Microarchitecture*, Chicago, IL, USA, December 2007.
23. “Memory Performance Attacks: Denial of Memory Service in Multi-Core Systems,” *16th USENIX Security Symposium*, Boston, MA, USA, August 2007.
24. “Address-Value Delta Prediction,” *38th International Symposium on Microarchitecture*, Barcelona, Spain, November 2005.
25. “Techniques for Efficient Processing in Runahead Execution Engines,” *32nd International Symposium on Computer Architecture*, Madison, WI, USA, June 2005.
26. “Wrong Path Events and Their Application to Early Misprediction Detection and Recovery,” *37th International Symposium on Microarchitecture*, Portland, OR, USA, December 2004.
27. “Cache Filtering Techniques to Reduce the Negative Impact of Useless Speculative Memory References on Processor Performance,” *16th Symposium on Computer Architecture and High Performance Computing*, Foz do Iguacu, Brazil, October 2004.
28. “Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors,” *9th International Conference on High Performance Computer Architecture*, Anaheim, CA, USA, February 2003.

Teaching Experience

Carnegie Mellon University, ECE Department, Instructor for Graduate Computer Architecture Course CS/ECE-740, *Fall 2010*

- Instructor rating based on student evaluations: 4.5/5.0 (43/53 students responded)

Carnegie Mellon University, ECE Department, Instructor for Parallel Computer Architecture Course ECE-742, *Spring 2010*

- Instructor rating based on student evaluations: 4.44/5.0 (18/20 students responded)

Carnegie Mellon University, ECE Department, Instructor for Advanced Computer Architecture Course ECE-741, *Spring 2009*

- Instructor rating based on student evaluations: 4.6/5.0 (25/35 students responded)

University of Texas at Austin, ECE Department, Teaching Assistant for Senior-level Computer Architecture Course EE360N, *Spring 2003*

- Instructor rating based on student evaluations: 4.7/5.0 (59/70 students responded)

University of Texas at Austin, ECE Department, Teaching Assistant for Senior-level Computer Architecture Course EE360N, *Spring 2001*

- Instructor rating based on student evaluations: 4.8/5.0 (30/50 students responded)

University of Texas at Austin, ECE Department, Teaching Assistant for Freshman-level Intro. to Computing Course EE306, *Fall 2000*

- Instructor rating based on student evaluations: 4.7/5.0 (35/55 students responded)

Supervised Students

Current PhD Students at CMU: Rachata Ausavarungnirun, Chris Craik, Chris Fallin, Yoongu Kim, Justin Meza, Gennady Pekhimenko, Vivek Seshadri, Lavanya Subramanian, Evangelos Vlachos, Han Bin Yoon

Current Undergraduate Students at CMU: Rachael Harding

Current Masters Students at CMU: Huimin Yang

Current Mentees at UT-Austin: Eiman Ebrahimi, Jose Joao, Khubaib, Chang Joo Lee, Rustam Miftakhutdinov, Veynu Narasiman, Aater Suleman
Internship Manager of: Rishi Agarwal (IIT-Kanpur), Kypros Constantinides (Michigan), Alejandro Cornejo (MIT), Reetuparna Das (Penn State),
Eiman Ebrahimi (UT-Austin), Engin Ipek (Cornell), Jose Joao (UT-Austin), Yanjing Li (Stanford), Xuehai Qian (Illinois)

Ph.D. Thesis Committee Member of: Chen-Ling Chou (CMU), Reetuparna Das (Penn State), Eiman Ebrahimi (UT-Austin), Engin Ipek (Cornell),
Lei Jin (Pitt), Karthik Lakshmanan (CMU), Chang Joo Lee (UT-Austin), Olatunji Ruwase (CMU), Marek Telgarsky (CMU)

Professional Service

Technical Journal Editorships

Associate Editor, ACM Transactions on Architecture and Code Optimization, Feb. 2010 - Present.

Co-Guest Editor, IEEE Micro special issue (May/June 2008) on "The Interaction of Computer Architecture and Operating Systems in the Many-core Era," May/June 2008.

Co-Guest Editor, IEEE Micro special issue (Jan/Feb 2011) on "Micro's Top Picks from Computer Architecture Conferences," Jan/Feb 2011.

Technical Conference Program and Steering Committee Chairmanships/Memberships

IEEE Micro Top Picks Selection Committee Co-Chair, IEEE Micro Special Issue on Top Picks from Computer Architecture Conferences, 2011.

IEEE Micro Top Picks Selection Committee Member, IEEE Micro Special Issue on Top Picks from Computer Architecture Conferences, 2010, 2009.

ISCA Program Committee Member, International Symposium on Computer Architecture, 2010, 2008.

MICRO Program Committee Member, International Symposium on Microarchitecture, 2008, 2007.

ASPLOS Program Committee Member, Intl. Conf. on Architectural Support for Programming Lang. and Operating Systems, 2011, 2009.

HPCA Program Committee Member, International Symposium on High Performance Computer Architecture, 2010, 2009.

ICCD Program Committee Member, IEEE International Conference on Computer Design, 2010, 2009.

IISWC Program Co-Chair, 4th IEEE International Symposium on Workload Characterization (IISWC), Sep. 2008.

IISWC Program Committee Member, IEEE International Symposium on Workload Characterization, 2009.

IISWC Steering Committee Member, IEEE International Symposium on Workload Characterization, 2008-Present.

MSPC Program Committee Member, ACM SIGPLAN Workshop on Memory Systems Performance and Correctness, with ASPLOS, 2008.

Technical Workshop Committee Memberships

WIOSCA Co-organizer, Workshop on the Interaction between Operating Systems and Computer Architecture, 2007-2010. (Held with ISCA).

WEED Program Committee Member, Workshop on Energy-Efficient Design, 2010. (held with ISCA)

PESPMA Program Committee Member, Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures, 2010, 2009. (held with ISCA)

CATARS Program Committee Member, Workshop on Compiler/Architectural Techniques for Application Reliability/Security, 2009, 2008. (held with DSN)

WDA Program Committee Member, Workshop on Dependable Architectures, 2008, 2006. (held with MICRO)

RAAW Program Committee Member, Reconfigurable and Adaptive Architecture Workshop, 2007. (held with MICRO)

Technical Reviewer for Journals

ACM Transactions on Architecture and Code Optimization, ACM Transactions on Design Automation of Electronic Systems, Communications of the ACM, IEEE Computer, IEEE Micro, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Reliability, IEEE Computer Architecture Letters, HiPEAC Journal. Journal of Parallel and Distributed Computing, ACM/IEEE Transactions on Networking.

Technical Reviewer for Conferences

ISCA, MICRO, HPCA, ASPLOS, Usenix Security Symposium, HotOS, DAC, ICS, PACT, IPDPS, ISPASS, HiPEAC, Euro-Par, SBAC-PAD, WASP, SBCCI.

Expert Reviewer for Research Proposals

NSF Review Panel Participant, 2007, 2008, 2009, 2010.

DOE Review Panel Participant, 2010.

Microsoft Research Breakthrough Research Grant Proposal Reviewer, 2007.

Microsoft Research New Faculty Fellowship Candidate Reviewer, 2006, 2007.

Microsoft Research Reviewer for Miscellaneous Requests for Proposals, 2007, 2008.

Microsoft Research Fellowship Candidate Reviewer, 2006, 2007, 2008.

Departmental Committee Memberships

CMU CSD Faculty Hiring Committee, 2010.

CMU ECE Seminar Committee, 2011, 2010.

Other Committee Memberships

Local Arrangements Chair, ASPLOS 2010.

Publicity Chair, HPCA 2010, IISWC 2009, ASPLOS 2008.

Publications Chair, ICS 2007.

Professional Memberships

Member of IEEE, since 2000, IEEE-CS, ACM, and ACM-SIGARCH, since 2005, and ACM-SIGMICRO, since 2007

Member of Eta Kappa Nu Electrical Engineering Honor Society and Tau Beta Pi Engineering Honor Society, since 1998