CAD for Integrated MEMS Design

Tamal Mukherjee

Department of Electrical and Computer Engineering
Carnegie Mellon University, Pittsburgh, PA 15213-3890 USA, tamal@ece.cmu.edu

ABSTRACT

The long term impact of MEMS technology will be in its ability to integrate novel sensing and actuation functionality on traditional computing and communication devices enabling the ubiquitous digital computer to *interact* with the world around it. The design of such integrated systems will occur at the system level, driven primarily by the application. Methodologies that ease the integration of the digital domain to the real world using mixed domain technologies are therefore crucial. A hierarchical structured design approach that is compatible with standard IC design is outlined. It starts with schematic capture of a design topology, followed by behavioral simulation, layout generation, parasitic extraction, and final verification. This flow is based on a process-independent design representation of commonly used MEMS building blocks, and process-dependent materials properties, design rules, and parasitic parameters.

Keywords: MEMS CAD, MEMS design methodology, modular design, composable design, integrated MEMS design.

1. INTRODUCTION

The trend towards monolithically integrating MEMS with standard CMOS processes is being driven by the ever-present need to lower cost and increase device sensitivity and reliability. The ability to integrate digital control and to provide digital interfaces increases actuator or sensor value, while the exploitation of the process integration and automation common in CMOS fabrication increases device yield. The combined effect is underscored by the fact that recent high-volume product introductions have tended to be integrated such as: airbag accelerometers [1], digital light processors [2] and pressure sensors [3]. In addition to increasing device integration, process integration of CMOS to a variety of MEMS processes including deep reactive-ion-etching of silicon (Si DRIE) [4], dissolved-wafer [3], polysilicon [5] and thick epi-polysilicon [6] technologies is under way.

Current low-cost MEMS designs are targeted for high-volume applications such as the automotive accelerometers, gyroscopes and pressure sensors, or consumer ink-jet print heads. Smaller markets for MEMS that cannot be addressed by existing commercial systems tend to be ignored due to design time and cost involved in custom MEMS design. Custom design currently involves designers that need to be experts in MEMS processing, MEMS device design, system integration, as well as the final application domain. As in-depth expertise in each of these regions and breath across these domains is extremely difficult to acquire, few custom designs are attempted. Therefore MEMS continues to be dominated by high-volume markets.

Translating the excitement of the researchers developing the initial integrated microsystems into an ubiquitous embedding of MEMS in the information appliances of tomorrow requires an integrated MEMS design methodology that formalizes the communication between the process, device, system and application domains, and exploits the expertise in each domain. Such a methodology is required both because of the complexity of integrating MEMS design with CMOS design, as well as to enable the information appliance design experts to include MEMS sensors if so desired. It is this very capability to enable the successful design of Application Specific Integrated Microsystems (ASIMs) that will enable an enormous advance in commercialization of MEMS in the various application areas where MEMS is ideally suited.

Characteristics of an integrated MEMS design methodology that can enable rapid design of low-volume custom MEMS include: supporting a wide class of MEMS designs; being extensible to handle new MEMS concepts; supporting a wide variety of MEMS fabrication techniques; fitting into the existing VLSI design flows; and, having the capability to evaluate integrated system designs. A modular approach to MEMS design which addresses these requirements is being developed at Carnegie Mellon [7][8][9][10][11]. The approach is underpinned by a library of elements that enables modular design compo-

sition. The library of elements has been created from the observation that today's full-custom MEMS designs tend to be decomposable to a set of common elements, parameterized by the design (layout) geometry.

The modular design methodology focuses on suspended micromechanical systems. The class of suspended MEMS devices covers many important application domains (including accelerometers, gyroscopes, and pressure sensors for automotive markets; micropositioners for data storage; resonators, RF filters, variable capacitors for communication systems; micromirrors for optical data processing systems; and acoustic and ultrasonic transducers). This application variety and complexity, all decomposable into a very small set of fundamental elements, led to our focus in this class of designs. The decomposition of electrostatically-actuated suspended MEMS designs into perforated plates, beam springs of various topologies (*e.g.*, folded-flexure, crab-leg flexure), electrostatic air-gaps and anchors, is exemplified in Figure 1. This list of elements can be expanded to include additional classes of MEMS devices (such as thermomechanical systems). Process variety (such as Si DRIE, dissolved-wafer, CMOS-MEMS and polysilicon) is managed using process-specific materials constants and geometric dimensions such as thickness. The composition of complex devices from simple elements and use of parameterized behavioral models for simulation are analogous and compatible with VLSI design. By developing this methodology in design environments already in common use in VLSI design, and enabling simulation of cross-domain effects arising from integration, seamless insertion of MEMS into an application-specific design flow is possible.

Our approach falls into a class of design methodologies known as *top-down* or *structured* design methodologies [12][13][14][15]. Top-down design methodologies begin with a conceptual representation of a microsystem, gradually, hierarchically specifying components of the microsystem, and verifying that the sub-components can achieve the component design goals. Such methodologies require an abstraction of process dependent parameters for a characterized process, as will be discussed in Section 2, as well as process independent interoperable composable design representations as will be discussed in Section 3. Once a design is composed, it needs to be evaluated: Section 4 shows how behavioral simulation can be used for design evaluation and iterative design improvement. Section 5 details the layout generation and Section 6 covers the layout verification approaches at the back end of the design flow. Finally, we consider the future of integrated MEMS design in the conclusions in Section 7.

2. PROCESS ABSTRACTIONS

One of the required foundations for application specific integrated MEMS is foundries. The number of MEMS start-ups offering unique processing capabilities has exploded in the last few years. Furthermore, standardized MEMS processes such as the polysilicon iMEMS^{TM} [16] or MUMPS [17] processes have become increasingly available as foundry processes. As an alternative to polysilicon, microstructures fabricated using CMOS interconnect layers that decouples the micromachining steps from the CMOS process flow has been demonstrated [18]. Plans for offering this post-CMOS micromachining process as a foundry process are being developed. This process has the advantage of low-cost fabrication of integrated MEMS and the capability to place multiple isolated conductors within suspended structures. A 3D visualization of the single-structural layer beams possible from the polysilicon and CMOS MEMS processes is shown in Figure 2. The top-most metal layer is used as a mask to define the structure in CMOS micromachining. Fourteen different composite structures can be made by using different combinations of the embedded metal layers and polysilicon. A scanning electron micrograph of a released composite beam with three metal conductors is shown in Figure 2(d).

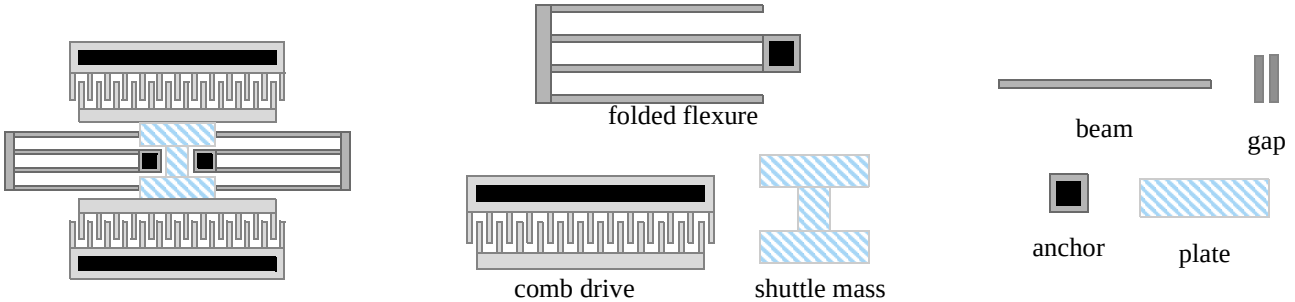


Figure 1 Decomposition of a folded-flexure resonator: (a) component-level folded-flexure resonator; (b) functional elements include comb drive and folded flexure; and (c) atomic elements include plates, beams, gaps and anchors.

Unlike VLSI, where a few processes dominate, MEMS is characterized by a wide variety of process technologies and novel processes still being developed. Any effort to create a design methodology for MEMS must therefore concern itself with developing an abstraction of the MEMS processes to interface between process engineers and design engineers. The idea of process abstraction is not new. Some of the very first approaches to MEMS design involved microscopy-based characterization of the fabricated device, development of a solid model, subsequent meshing and numerical simulation. These simulation studies, though cumbersome could be used to suggest design improvements only if the process-specific material propreties were known. Process abstraction grew out of the need to make these simulation codes process independent.

The process abstractions for an integrated MEMS design flow based on composable behavioral models, however, have to be different from those of a design flow based on solid modeling, meshing and continuum simulation. Observing that all processes are based on the same deposition, patterning and etch fundamentals allows us to develop a layered abstraction. Each process can be defined by its layer definitions required for manufacturing as well as associated characterized material properties and geometric dimensions. In the VLSI design methodology, this information is captured in a layout technology file, a layout design rule file, a layout parasitic extraction file and a device model file. Our modular design methodology uses the same four files to map process information into the design flow. As in VLSI, the layout technology file identifies the layers available for layout (no MEMS specific changes are required).

The layout design rule file captures the process engineer's view of what can be robustly manufactured by the process. Due to the similarity of the processing steps, many of the design rules have the same flavor as in VLSI. Process steps unique to MEMS include sacrificial etching for microstructure definition and device release. The undercut etch process for release in a foundry fabrication line can be characterized by the hole or gap size (related to quantity of etchant available for sacrificial etching) and the structure size (related to amount of sacrificial etching needed). High volume processes can alter etch time for optimal release of a given product. Low volume or foundry processes can only offer a constant-time release etch. For such processes the relationship between the hole/gap size and structure size required for release can be encapsulated in maximum structure width and minimum hole or gap size (i.e., a single number for each parameter), or by a non-linear function. Commercial DRC representations can only handle a single minimum or maximum constraint for each parameter. As the single value is overly restrictive (comb-drives tend to have small gaps between thin beams for improved sensing while plates tend to be wide and require larger gaps around them to ensure release), a discretized approach is followed. The span of structure widths commonly used by designers are studied and binned. For each bin, the minimum gap and hole size required to ensure release is determined, and encoded into the design rules.

The process-dependent layout parasitic extraction file encodes the parametrized values of the undesired but inevitable resistances and capacitances in VLSI. As a different set of parasitic resistances and capacitances occur within the MEMS portion as compared to the electronics portion of integrated MEMS designs, parasitic parameters for both regions have to be separately characterized and encoded into the layout parasitic extraction file. Additionally, mechanical parasitics exist, such as the joint between beams. The modeling of these parasitics is related to the lumped parameter modeling of the beams, and will be detailed in Section 6.

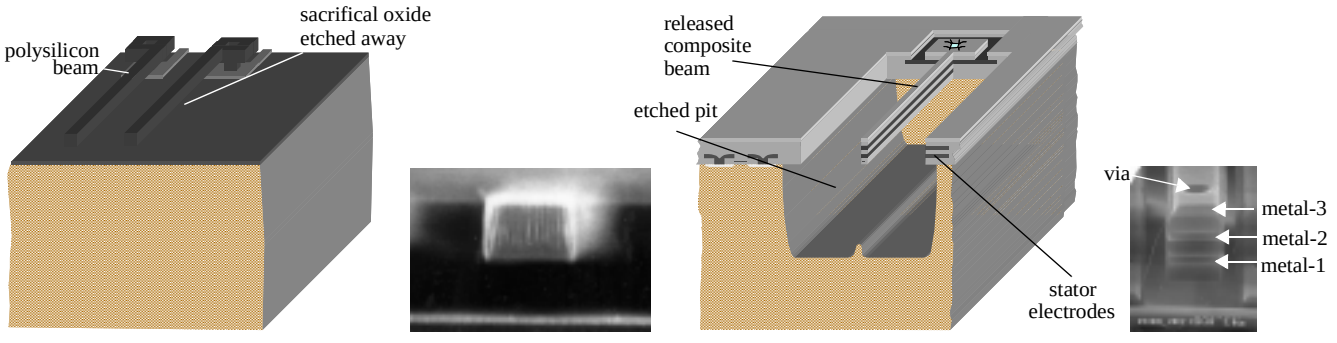


Figure 2 Comparison of polysilicon and CMOS micromachining: (a) visualization of polysilicon beams; (b) cross section of polysilicon beam; (c) visualization of CMOS micromachined beam; (d) cross section of a composite CMOS microstructural beam with three CMOS metallization layers embedded

The success of application-specific integrated MEMS design requires both low design and fabrication cost as well as a fast time to market. Preventing fabrication iterations is therefore highly desired, and can only be attained if the device model parameters are well characterized. Technology-dependent modeling parameters required for electromechanical design include nominal, minimum and maximum values for layer thicknesses, structural sidewall overetch and angles, structural release undercut, layer sheet resistance, effective material density, effective Young's modulus, residual stress, and residual stress gradient. For post-CMOS micromachining with three-metal interconnect layers, a different set of parameters are needed for each of the different composite beam types. Just as process characterization is used to determine the values of the technology dependent design rule file, and parasitic characterization is used to determine the values in the technology dependent parasitic extraction rule file, the device model parameters can be characterized using appropriate test structures. Although characterization approaches based on automated all-electrical testing have been proposed [19][20], many parameters such as residual stress gradients can still only be obtained by time-consuming manual methods.

Our modular design methodology has initially been targeted to two MEMS fabrication technologies, polysilicon technologies such as Analog Devices (ADI) iMEMS^{TM} or Cronos MUMPS process and the Carnegie Mellon CMOS-MEMS process. The process abstractions described above enable subsequent targeting to a variety of MEMS processes which have been integrated with CMOS including deep reactive-ion-etching of silicon (Si DRIE), dissolved-wafer, and thick epi-polysilicon.

3. DESIGN ABSTRACTIONS

In addition to the process-dependent parameters needed for design, our integrated MEMS design methodology depends on an interoperable composable design representation. Each element in the modular representation can have multiple views: symbol, behavioral model, schematic, layout, and 3D, all stored in the element library at the center of Figure 3. The symbol representation is used to construct schematics at a design hierarchy level immediately higher than the symbol's level. The behavioral model associated with the symbol capture the same electrostatic forces, mechanics, coupled electromechanics, and damping physics as in commercial finite-element and boundary-element tools. The schematic representation is used for evaluation of the design performance, and captures the interconnection of symbols (design topology), and the geometry parameters of each symbol (component sizing). The schematic representation enables iterative simulation-based design by allowing the designer to alter design topology and sizing and subsequently simulate the effect of these alterations using the behavioral models. The layout view is required for defining the design to the manufacturing foundry. Schematic-driven layout generation eliminates the tediousness of design entry directly at the layout representation although manual design entry of layout is still allowed for historical compatibility. Translating the layout back to a schematic representation involves extraction. Finally, automatic mesh generation algorithms directly from schematic, or from layout can be used for generating the 3D solid model

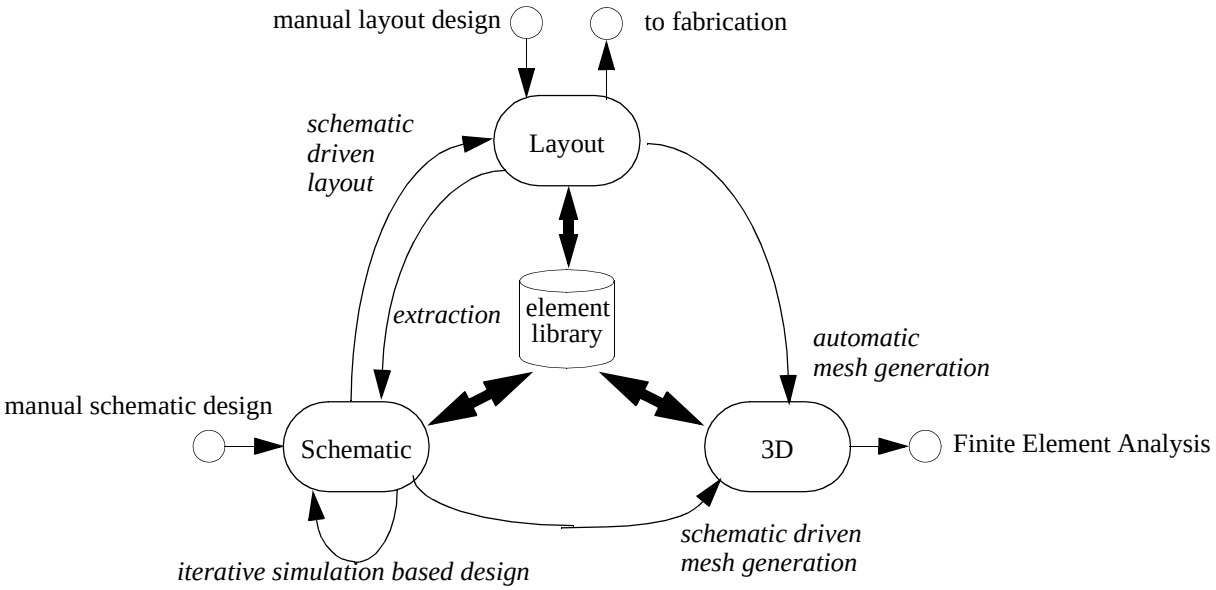


Figure 3 Integrated MEMS Design Methodology.

or mesh representations common in MEMS. In our methodology, the 3D view is solely for detailed design verification; therefore translators from that representation to the alternative representations are unnecessary.

Current design methodologies tend to begin with a layout view that is transformed to a solid model or mesh view, or start directly from a solid model view of the MEMS device. Finite- and boundary-element modeling of the electrostatic forces, mechanics, coupled electromechanics and damping are then used to construct reduced-order behavioral models [21][22] for system-level simulation. These derived models are fixed for the given geometry and material properties. In contrast, our methodology is centered around schematic-based simulation and relies on models parameterized by the design geometry and material properties. These physical parameterized models for each of the low-level elements such as beams that have adequate accuracy (~ 1%) as compared to numerical simulation form the foundation of our design methodology [23][24][25][26].

The design library can contain elements at several levels of the hierarchy. At the lowest level are the *atomic elements* such as beams, plates, gaps and anchors of Figure 1(c). These elements are chosen by three characteristics: they are often re-used (albeit sized by appropriate geometric parameters); they are modular (in the sense that they are decoupled from neighboring elements); and simple lumped parameter models describe their behavior to first order. Additional higher-level elements can also satisfy these characteristics. In particular, the parameterized *functional elements* of Figure 1(b) are easily re-used because they capture a single function (generate electrostatic force, provide mechanical stiffness, *etc.*) and hence can be accurately represented by behavioral models. While parameterized models at the *component-level* are still possible, the fixed topology of entire components such as in Figure 1(a) limits their re-usability, thereby reducing the motivation for parametrized modeling. Furthermore, the larger number of design variables at the component level requires substantially more simulation for generating a parametrized reduced-order model.

We now consider the details of iterative simulation, schematic driven layout, extraction, and mesh generation in more detail.

4. MEMS CIRCUIT SIMULATION

Once an integrated MEMS circuit representation is composed, the first issue is evaluating the designed physical system in the context of its specifications. Behavioral modeling of physical system dynamics can be accomplished through signal-flow or network (circuit) representations. Recent approaches [27][28] have focused on the circuit representation due to interoperability with electronic circuits.

The development of a circuit representation requires identification of the types of quantities at the terminals of a “circuit” element, as well as the relationship between these quantities within the element. In the electrical domain, the voltage at the terminal (across variable), and the current into the terminal (through variable) are commonly used abstractions. Similarly, in the linear and rotational mechanical domain, one may use the force and torque and linear and rotational displacements as the through and across variables, respectively. Other physical domains can be handled by appropriate terminal natures (across and through variables) [29]. Once the terminal natures are defined, the element can be modeled as by relating the flow through the terminals to the potential across the terminals. This model is often called a *constitutive relationship* in network theory.

By using the same terminal natures at all levels of the design hierarchy, a composable design representation for mixed-level simulation is possible. This is particularly important as simulation of entire MEMS systems at the atomic level, though possible, may involve unnecessary long simulation times. A library consisting of the most common atomic and functional elements therefore supports both rapid simulation as well as the capability to represent a wide class of designs.

Physical system simulation capabilities that interoperate with electronics are a fundamental requirement for integrated MEMS design. These capabilities are possible through the use of mixed-signal hardware description languages, such as the nascent Verilog-AMS [30] and VHDL-AMS [31] standards. The examples in this paper are based on models written in Verilog-A for the Spectre™ behavioral simulator in the Cadence design framework (Verilog-A is the analog portion of Verilog-AMS) [26]. In addition to the constitutive relationships as in electrical elements, mechanical elements require position information within a reference frame. This is required both for simulation (as the transducers in inertial sensors detect displacement relative to the package, or chip, frame of reference which has to be translated into acceleration and rotation with respect to a

fixed frame of reference), and for layout generation. The location parameter is not a quantity at a terminal but rather a parameter of the element (similar to the element length and width).

The flexibility of this design methodology is shown by two design examples. The first example is a bandpass filter composed of three identical resonators, each resonating at 550 kHz, coupled by springs, based on [32]. The topology of the filter (Figure 4(a)) is captured in the schematic using the elemental symbols from the element library. Both mechanical structures and interface circuitry are included. Each of the three resonators is composed of a center proof mass, crab-leg springs, and differential electrostatic comb drives (for actuating and sensing). The stator fingers are connected to the input voltage V_{in} with DC bias at 0 V, and the rotor fingers are differentially DC biased at V+ and V-, therefore, the fingers theoretically will have no DC position offset. When a sinusoidal voltage is applied to the stator fingers, electrostatic forces will be generated to actuate the suspended microresonators. In the CMOS-MEMS implementation, the comb fingers consist of a stack of three metal layers and a polysilicon layer. These layers are electrically connected to the same voltage to maximize the active sidewall area of capacitance, therefore, the electrostatic force. The "O" shaped coupling spring topology employed in this design is composed of beams with metal-2 and metal-1 only, in order to obtain softer springs, and therefore, narrower bandwidth. The three resonators resonate in *x*-direction, and are coupled at the center plates of each resonator. The SEM of two released filters and the close-ups of the differential comb drive and "O" coupling spring is shown in Figure 4(b). The device was tested in air, with bias voltage at +/-20V. Figure 4(c) shows the frequency response of the entire filter system (output voltage of interface circuit), with comparison to simulation. The comparison shows that the nominal simulation result matches the experimental results to within 3%. Adding an overetch of 0.035 μm leads to a simulation that matches the experimental results even more closely [33].

An accelerometer schematic, also for the CMOS-MEMS process, is shown in Figure 5(a). It is a fully differential common-centroid accelerometer using the topology described in [34][35]. Sensing nodes are located at stators instead of rotors to

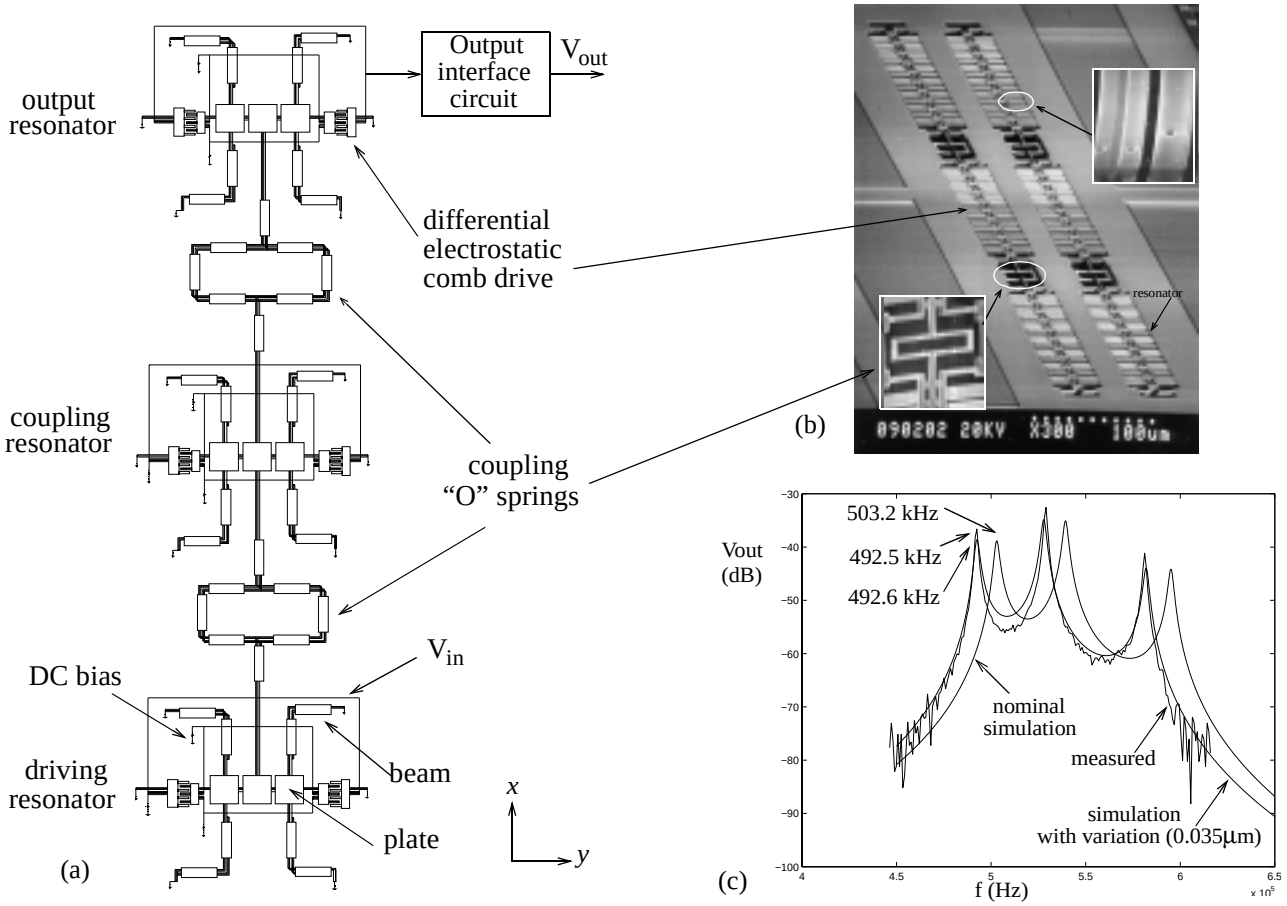


Figure 4 (a) Schematic Representation of Crab-leg resonator filter; (b) SEM image of CMOS-MEMS implementation (two separate filters were fabricated side by side); (c) Experiment vs. Measured filter characteristics.

minimize parasitic capacitance. Differential modulation signals are routed through the serpentine spring by the two metal layers under the top metal layer of the CMOS metal stack. The simulations using the integrated MEMS design methodology were compared with experimentally measured results as in Figure 5(c). The resonant frequency and sensitivity simulated results are within 10% of the measured data. Noise simulation in our current methodology only considers Brownian noise (an integrated simulation environment is still under development), and vastly underestimates the sensor noise.

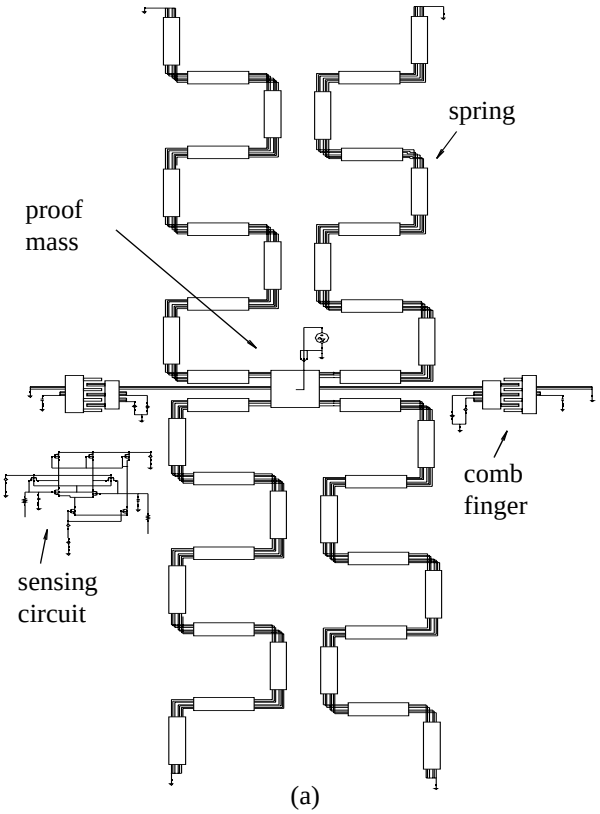
5. LAYOUT GENERATION

Once a MEMS schematic has been composed, and simulation results used to improve the design until the desired specifications are met, a layout needs to be generated. As manual layout generation is cumbersome and error-prone, automated approaches have been investigated.

Parametrized layout generation

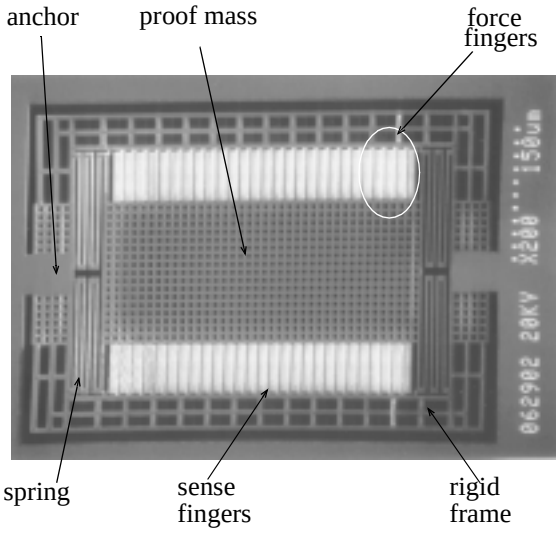
Parametrized layout generation for commonly used MEMS functional elements from a text file [36] or library palette in the layout editor have been demonstrated [37][38]. These functional elements still have to be manually placed and connected by abutment. For large MEMS designs, such as gyroscopes with many comb drives, layout errors due to mislocating an individual functional element by a few sub-microns may still occur. Such errors may lead to design asymmetry, and induce sources of quadrature errors. In contrast, a completely automatic layout generation methodology promises a “correct-by-construction” layout.

The one-to-one correspondence between the elements used in the MEMS schematic and the layout as shown in Figure 6, enables automatic generation of the entire layout. By associating a layout view with each of the elements in the schematic library, such that all the layout parameters match with the simulation parameters, parametrized schematic driven layout technologies in existing commercial CAD environments can be used for element level layout generation. The complete layout is constructed by abutting these individual parametrized elements the placement location of the elements and their layout geom-



(a)

(b)



	Simulated	Tested
Resonant frequency	5.9 kHz	6.1 kHz
Sensor sensitivity	0.6 mV/G	0.5 mV/G
Noise	$28\mu G/\sqrt{Hz}$ (Brownian only)	$1mG/\sqrt{Hz}$ (total)

(c)

Figure 5 (a) Schematic of CMOS-MEMS Accelerometer; (b) SEM image of (rotated) accelerometer; (c) Simulation vs. Measured results.

etry are intimately linked. The interface to the designer in our implementation asks for the element sizes as annotations on the element symbols and the device topology as a interconnection of the elements in the schematic, and proceeds to compute the location of each element automatically every time the design is saved. This location information is needed for the position parameter described in Section 4 as well as to automate layout generation.

For CMOS-MEMS, the progress towards sub-micron CMOS technologies is requiring filling of metal layers to eliminate dishing in open areas due to chem-mechanical polishing and slotting of wide metal to manage stress. As the top-most metal tends to be used as a mask for the MEMS structure, slotting above the circuit areas, and filling in the MEMS areas are required. Layout post-processing routines have been developed to automate this effort, while ensuring that the resulting fill does not affect surrounding microstructures and the slotting does not damage the electronic circuits.

Layout Synthesis

Layout synthesis tools that map engineering design specifications directly into the sizes of the layout elements for a given topology enable on-the-fly custom design of MEMS devices. Synthesis modules for commonly used suspended-MEMS components, such as resonators [39], accelerometers in polysilicon [40] and CMOS-MEMS [41] processes have been developed. Instead of redesigning these components each time a new system is proposed, engineers benefit from synthesizers which tackle the routine design of frequently-used components. From the system designer's point of view, such synthesizers take care of all the technology and device issues, and allow the designer to focus on the component performance, and its impact on system performance. In contrast, the freedom to develop new topologies in the simulation-based iterative integrated MEMS design flow is directed to the MEMS circuit-level designer.

Examples of synthesized layouts for CMOS-MEMS accelerometers with the same topology of Figure 5 are shown in Figure 7(a) and (b). The optimized accelerometer layouts have a common specification of 10 G range, 1 kHz bandwidth, 1% cross-axis sensitivity, and maximum allowed area of 500 x 270 $(\mu m)^2$. The area limits are specified based on a manual design [35]. In addition, the minimal sensitivity design has a 100 $\mu G/\sqrt{Hz}$ noise floor constraint, while the minimal noise design has a 0.5 mV/G sensitivity constraint. Furthermore, the circuit noise is specified to be 10 $nV/\sqrt{Hz}$, and the parasitic capacitance (at the preamplifier input) to be 270 fF. Also shown (Figure 7(c)) is the sensitivity *vs.* noise trade-off in accelerometer design optimization. The designs were optimized to minimize noise for different sensitivity values. The total system noise consists of mechanical Brownian noise and the electrical circuit noise. The minimum noise is obtained at a sensitivity of 0.4 mV/G. The discrete humps in the curves results from integer valued variables (number of comb fingers). Naively, one would think that larger mass leads to larger sensitivity and lower noise. But, as shown in Figure 7(c), for the given sensor configuration, the finger-gap dominates the noise figure rather than the mass [41].

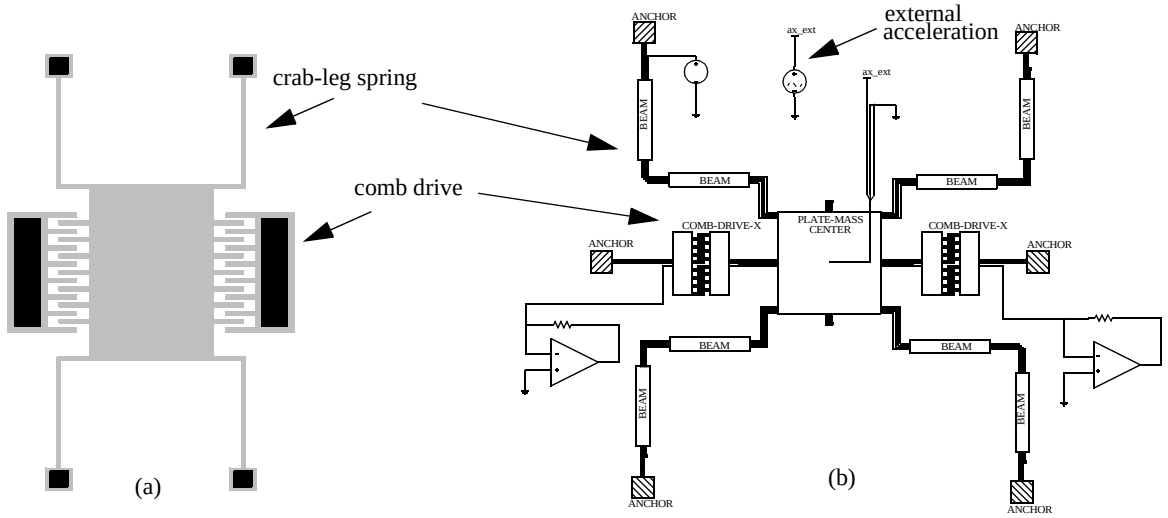
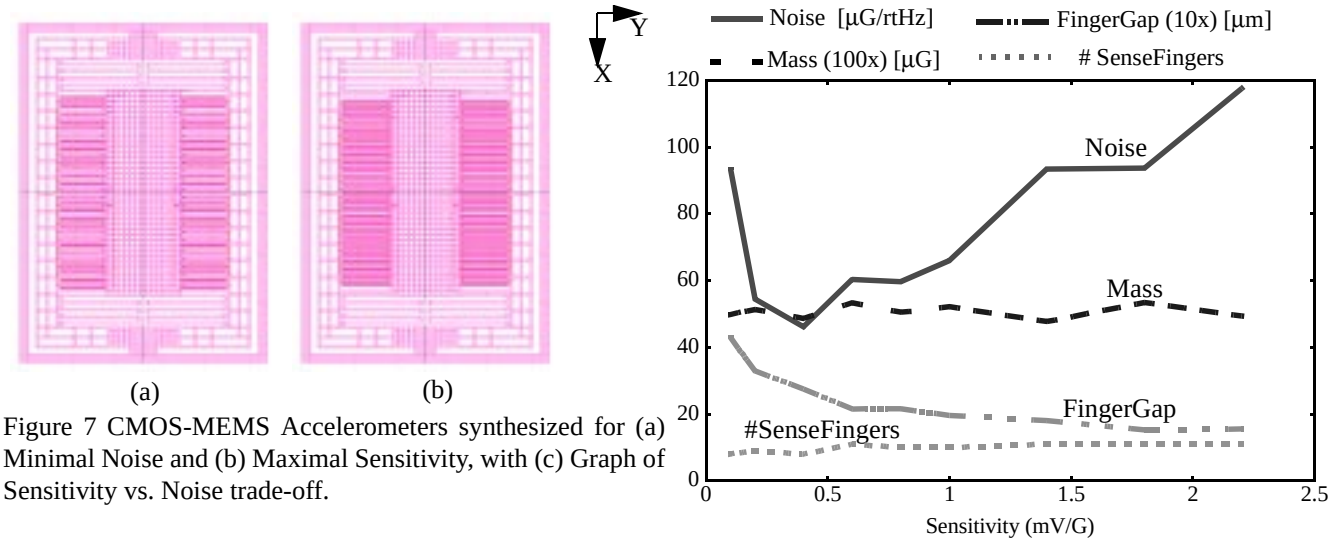


Figure 6 One-to-one correspondance between the (a) layout and (b) schematic view of a crab-leg accelerometer.



(a) (b)

Figure 7 CMOS-MEMS Accelerometers synthesized for (a) Minimal Noise and (b) Maximal Sensitivity, with (c) Graph of Sensitivity vs. Noise trade-off.

6. LAYOUT VERIFICATION

Once a layout is generated, it needs to be verified by design rule checking, electrical and mechanical rule checking and layout and parasitic extraction. Commercial design rule checking tools can be used for integrated MEMS as described in Section 2. The design rules that need to be checked in the MEMS areas are different from those in the circuit areas. Our methodology currently requires multiple rule checks with flags to enable or disable electronics or MEMS rule checking as desired by the designer. Context-dependent and global aspects of layout, such as checking for perfect symmetry of gyroscopes are not possible with commercial DRC tools, but can be easily implemented by considering asymmetry as a parasitic element during extraction, and simulating to check for the distortion arising from such asymmetries.

Layout Parasitics

Due to the lumped parameter modeling of the schematic elements, the joint between two beams in a flexure becomes a parasitic element. The compliance of the joint can be considered to be like a fringing effect, and can be modeled by extending the length of the beams incident at the joint. If one of the beams incident at the joint is significantly wider than the other beam, then the moment arms at the joint need to be considered. The use of a rigid plate to model this joint is often appropriate. Extension factors and the use of plate joints have been verified by comparing the MEMS circuit simulation with continuum finite element simulation for all the common flexure topologies and a range of beam sizes; in all cases the error in flexure compliance and resonant frequency was less than 2%.

Due to the sacrificial etch involved in releasing the MEMS, the interlayer parasitic per unit area capacitances in the MEMS portion will be different from those in the electronics portion. Integrated MEMS extraction therefore needs to partition the chip layout into the MEMS and electronics portion, and extract each portion separately for layout parasitics. The two portions can then be combined by linking the extracted MEMS and electronic schematics for the simulation. This integrated simulation to understand the effect of parasitics is crucial for most integrated MEMS devices as the parasitics on the comb sensor determine device sensitivity, and the resistive path from the sense fingers to the electronics affects the device's noise floor. These parasitics can also generate forces that can lead to undesirable mode coupling or device instability. Simply simulating the effect of the MEMS parasitics on the MEMS element and the electronics parasitics on the electronic elements ignores the potential interaction between these parasitics. For example, a closed-loop system's loop transmission, and hence stability, may be affected by the parasitics on both the MEMS and electronics side.

Layout Extraction

Extraction translates layout into a corresponding schematic representation for layout versus schematic against the original circuit and simulation-based verification of the layout including parasitics. In order to back-annotate a schematic with extracted parameters, the extraction tool must be able to recognize the atomic elements and the functional elements from the

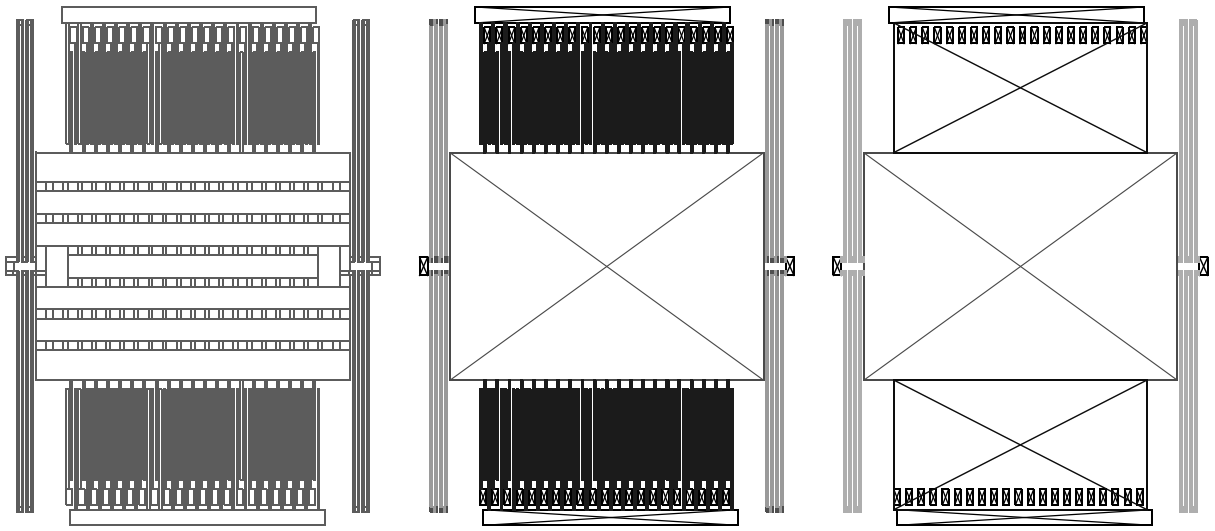


Figure 8 Accelerometer extraction showing (a) initial CIF layout, (b) recognized elements (anchors, plate, beams, joints, fingers, gaps), (c) detected functional elements (beams and joints as serpentine spring and fingers and gaps as differential comb-drive).

layout. General feature recognition algorithms for surface micro-machined MEMS have been developed to identify the atomic elements [42]. Technology-specific information from other layers, like location of anchor cuts, is used to help in this phase. Additional identification of the functional elements based on electrical connectivity analyses for comb-drives and mechanical connectivity analysis for flexures and has also been developed [43]. The extracted version of an accelerometer layout showing the recognized atomic elements, and the identified functional elements is given in Figure 8.

Meshing from Layout

Alternatively to extraction and simulation verification, the traditional solid-model and meshing approach for numerical simulation is also possible. Automatic meshing for CMOS-MEMS devices has been developed due to the complexity of manually meshing the multi-layer CMOS stack [44]. This meshing tool starts with the minimal mesh obtained from the same algorithms that are used for layout uniqueness during extraction. A mesh rules file then guides incremental mesh refinement until a computationally efficient mesh with little loss in accuracy is obtained. The resulting mesh can be used for numerical simulation to verify that the lumped parameter assumptions still hold for each new class of device designed using the integrated MEMS design flow. Eventually such verification will no longer be needed as designers become increasingly familiar and confident of a behavioral simulation based approach to design.

7. Conclusions

A composable integrated MEMS design flow has been presented. This flow is based on both existing commercial CAD tools and environments as well as novel MEMS-specific tools. Individual MEMS-specific point tools have been demonstrated, and are being integrated into a design framework suitable at meeting the needs of the integrated MEMS designer. This design flow enables rapid custom design of low volume MEMS. By reducing the time to a working design, this flow dramatically increases design productivity. Commercially supported design flows similar to this will become increasingly available as MEMS designs are inexorably embedded into the information appliances of tomorrow.

The modular basis for the design flow shifts the primary design entry point from solid modeling and/or layout to *schematic* entry. An extendible library of elemental schematic symbols, behavioral simulation models and layout and mesh generators forms the core of the design methodology. This library is process independent, and when coupled with process dependent technology abstractions, is able to support the coupling of custom-designed MEMS-enabled sensing and actuation with traditional electronics leading to application specific integrated microsystems.

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