CMOS Electrothermal Lateral Micromovers for Actuation and Self-Assembly

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ABSTRACT — A new CMOS electro-thermal actuator has been designed and fabricated. This design is capable of up to 6.8 µm lateral displacement with a length of 220 µm and a width of 22 µm. The structures were made from the CMOS interconnect stack using a maskless CMOS micromachining process. These 1st generation actuators were fabricated using Austria Microsystems (AMS) 0.6 µm CMOS process and Agilent 0.5 µm CMOS process. 2nd generation electro-thermal actuator designs in TSMC 0.35 µm CMOS Process have more area efficiency than the 1st generation designs. For 3.5 µm actuation, the 2nd generation actuators with a length of 224 µm and a width of 22 µm consume 18mW of power. The essential differences between this work and prior work are the high displacement magnitude with small geometry, pure lateral movement and the CMOS compatibility. The implementation in CMOS processes is particularly attractive for making tuning passives for RF applications. Several RF-MEMS tunable capacitor designs with these CMOS electro-thermal actuators have been fabricated and tested.

I. INTRODUCTION

Electro-thermal actuators have advantages, compared to the commonly-used electrostatic actuators, of lower driving voltages and providing larger forces. Several electro-thermal actuators were demonstrated over the past years [1-7]. For these designs, the common disadvantages of the thermal actuators were slower tuning, power consumption and space requirements.

In this paper, we describe a new CMOS electro-thermal actuator design, which is capable of up to 6.8 µm lateral displacement with a length of 220 µm and a width of 22 µm. The 6.8 µm lateral deflection for such dimensions is more area efficient than previous designs. One recent actuator design produced 2.7 µm deflection with 800 µm diameter circular area [1]. Bent-beam electro-thermal actuator designs 800 µm long and 13.9 µm wide demonstrated deflection of 5 µm [2].

There is an increasing demand on tunable on-chip passive components, as this is the one of biggest impediments for designing system on chip (SOC) receivers. The hardest part of designing tunable passives on chip is to increase the area efficiency. We integrated the new CMOS-compatible electro-thermal actuator into several tunable capacitor designs, which address the area efficiency.

II. CMOS MICROMACHING PROCESS

The high-aspect-ratio CMOS micromachining technology [8] begins with a conventional foundry CMOS process. Versions of these actuators were fabricated using Austria Microsystems (AMS) 0.6 µm CMOS, Agilent 0.5 µm CMOS and TSMC 0.35 µm CMOS. After the foundry fabrication, three dry-etch steps, shown in Figure 1, are used to define and release the structure. Figure 1(a) shows the cross section of the chip after regular CMOS fabrication. In the first step of post-CMOS processing (Figure 1(b)), dielectric layers are removed by an anisotropic CHF_3/O_2 reactive ion etch (RIE) with the top metal layer acting as an etch resistant mask. After the sidewall of the microstructure is precisely defined, silicon trenches around the device are micromachined into the substrate using a deep RIE step (Figure 1(c)). The final step is an isotropic SF_6/O_2 RIE used to etch away the bulk silicon and release the structure (Figure 1(d)). Multi-layer conductors can be built in the composite structure,

which enables more flexible designs than homogeneous conducting structures. The undercut of silicon in the release step (Figure 1(d)) requires the placement of sensing circuits to be at least 40 μm away from the microstructures.

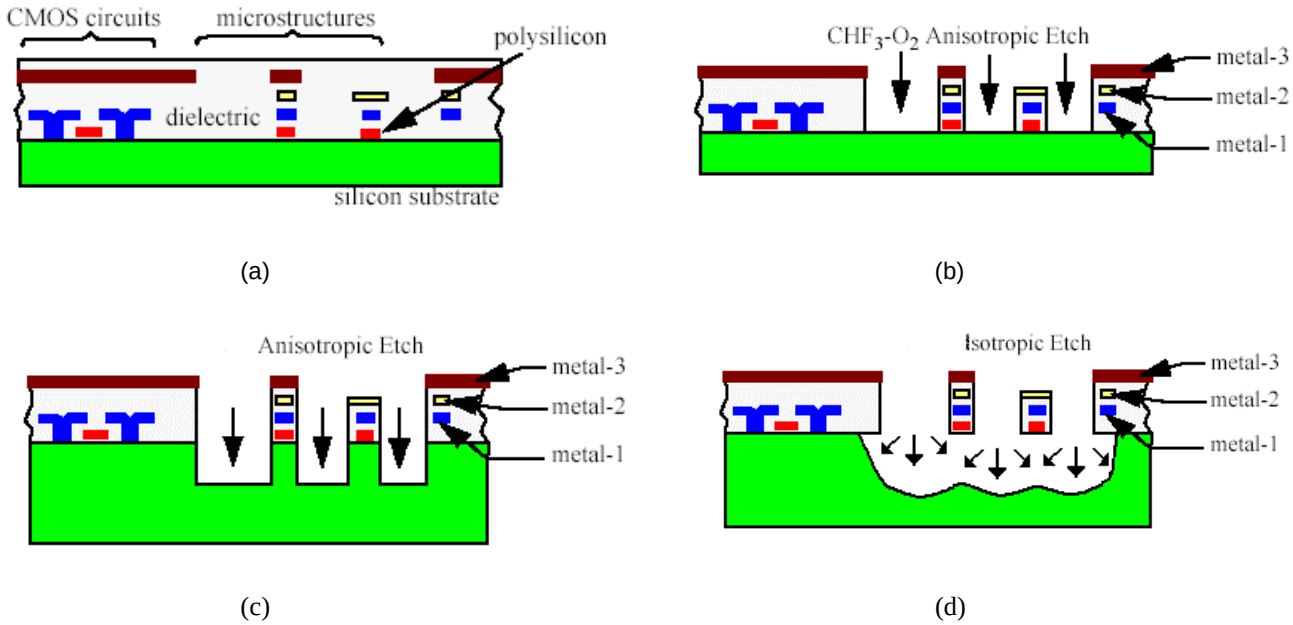

Figure.1. CMOS-MEMS process. (a) CMOS chip after fabrication, (b) anisotropic RIE removes dielectric layers, (c) anisotropic RIE removes substrate, (d) isotropic RIE undercuts silicon substrate.

III. DESIGN AND MODELING

A. DESIGN

Electro-thermal CMOS-MEMS designs are capable of large lateral displacement for tuning capacitors, self-assembly of small gaps, switches and other applications where micro-positioning on the order of 1 to 20 μm is desired. Motion is induced in specific beams by designing a lateral stress gradient within beam flexures. The lateral stress gradient arises from purposefully offsetting the lower metal layers with respect to the top metal layer of a CMOS-MEMS beam. A similar offset idea was presented for use in a lateral capacitive infrared sensor [9]. Of particular importance is the ability to tailor the lateral stress gradient, and therefore lateral moment, as a function along the beam length. This ability to set an internal moment along the beam arises from different offset and width of the embedded layers. The microstructures are made from the CMOS interconnect stack using a maskless CMOS micromachining process, however these beams could be made in alternate custom processes. The CMOS-MEMS beams are made from metal layers embedded within a dielectric (silicon oxide and silicon nitride). The offset layers do not have to be metal, and do not have to be embedded in dielectric. However, this particular design technique is particularly advantageous in CMOS-MEMS, since no special processing must be done to implement the designs.

The primary concept of the lateral actuator is illustrated in Figure 2. This particular design is a folded-flexure to relieve axial residual stress, as shown in Figure 2(a). The metal layers inside the flexure beams are offset to one side of the beam for half the beam length, and to the other side for the remaining half of the length. This arrangement provides a lateral stress gradient in one direction for half of the beams, then to the other direction for the other half. For many CMOS-MEMS processes, the residual stress gradient in the offset aluminum layers is tensile, while the residual stress gradient in the surrounding silicon oxide layers is compressive. Therefore, the aluminum expands and the silicon oxide contracts once freed to move. Upon release, this tailoring of stress provides a self-actuating operation, where the beams move into a “S” shape, as shown in Figure 2(b). This shape minimizes any moments at the ends of the beam, and therefore maximizes lateral motion. The design methodology for placement of the inner metal layers aims to set the beam moment so as to mimic bending from an external actuating force concentrated at the central piston.

The stiffness of the flexure in Figure 2 can be modified independent of the deflection. The particular design in Figure 2 employs 12 beams. Additional beams, ideally in a symmetric arrangement, may be added to increase the stiffness. This is a great advantage over electrostatic microactuation schemes. Electrothermal actuation can be applied to any designed actuator. The heating is implemented in CMOS-MEMS by embedding a polysilicon heater resistor inside the beam. Motion is induced from the different Temperature Coefficient of Expansion (TCE) of the metal offset layers and the rest of the beam material

(oxide). In the case of CMOS-MEMS, the offset aluminum layers have a much larger TCE than the surrounding silicon oxide. When heated, the side of the beam with the aluminum offset will expand relative to the other side. This effect leads to the actuated lateral motion, as illustrated in Figure 2(c).

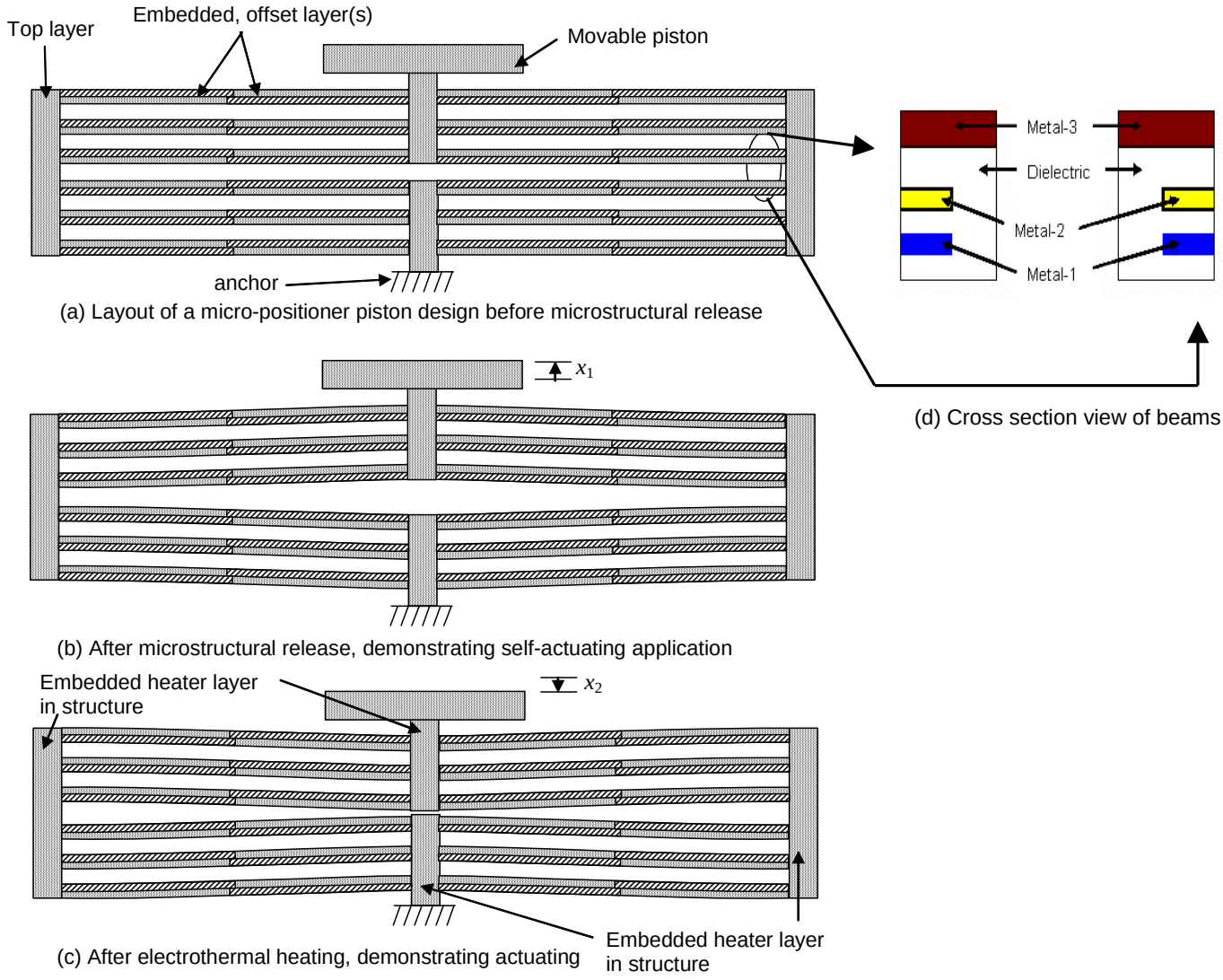

Figure.2. The concept of new electro-thermal actuator design.

B. MODELING

Displacement magnitudes of the lateral actuation are verified quantitatively by finite element analysis (FEA), using Coventorware [10]. For FEA, a simulation temperature, T_{set}, is calculated to model the lateral actuation magnitude upon release of the actuator.

$$T_{set} = -T_o + T_{sim} + T_d \quad (1)$$

where, T_{sim}, is the simulator initial temperature, usually 273 K, and T_d is the ambient temperature. T_o denotes the characteristic temperature at which the beam has zero deflection. Figure-3 is showing a simulation result for lateral displacement of the 1st generation actuator design in AMS 0.6 µm CMOS process with a length of 220 µm and a width of 22 µm at 113 °C. As it can

be seen from Figure-1, the lateral displacement magnitude at the tip of the actuator is 3.78 µm. Lateral displacements of this 1st generation actuator design at different ambient temperatures are given in Table-1.

Temperature (°C)	Simulated Lateral Displacement
27	7.36 µm
36	6.95 µm
70	5.5 µm
100	4.34 µm
135	2.88 µm
150	2.25 µm

Table.1. Simulated lateral displacements for actuator design in AMS 0.6 µm CMOS process with a length of 220 µm and a width of 22 µm at different ambient temperatures.

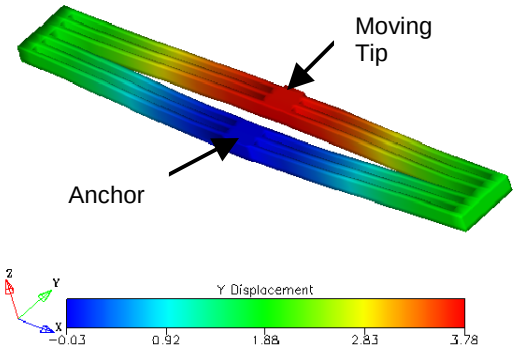

Figure.3. FEA simulation result for the lateral displacement (in µm) of the actuator design in AMS 0.6 µm CMOS process with a length of 220 µm and a width of 22 µm, at 113 °C.

IV. FABRICATION AND TEST

The lateral displacements are measured with an optical profiler and an MIT microvision system. For an area of 220 µm by 20 µm, the actuators in AMS 0.6 µm CMOS displaced 6.8 µm, upon release. Figure-4 is showing the scanning electron micrograph (SEM) of the released actuator. When this actuator is heated, the structure retracts back toward its layout shape. For a controlled actuation of 4.0 µm, the structure must be heated to 150°C. Figure-5 is showing a different electro-thermal actuator design, which is anchored from both sides. Upon release, this design with a length of 100 µm and a width of 11 µm displaced 1.2 µm, which is much less compared to the folded-flexure design. The extensional stress in the fixed-fixed design limits the effectiveness of the actuation.

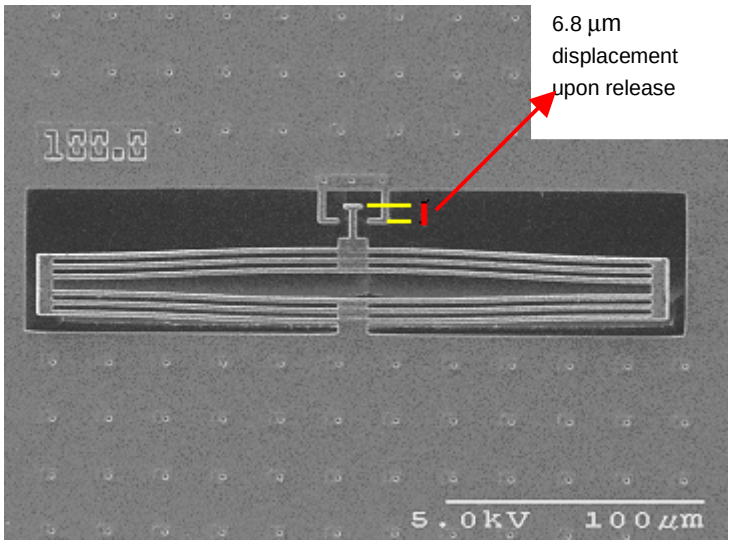

Figure.4. SEM of an actuator in AMS 0.6 µm CMOS process with a length of 220 µm and a width of 22 µm at room temperature, upon release.

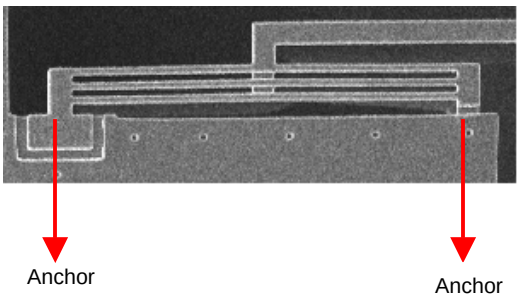

Figure.5. SEM of a released actuator in AMS 0.6 µm CMOS process, which is anchored from both sides.

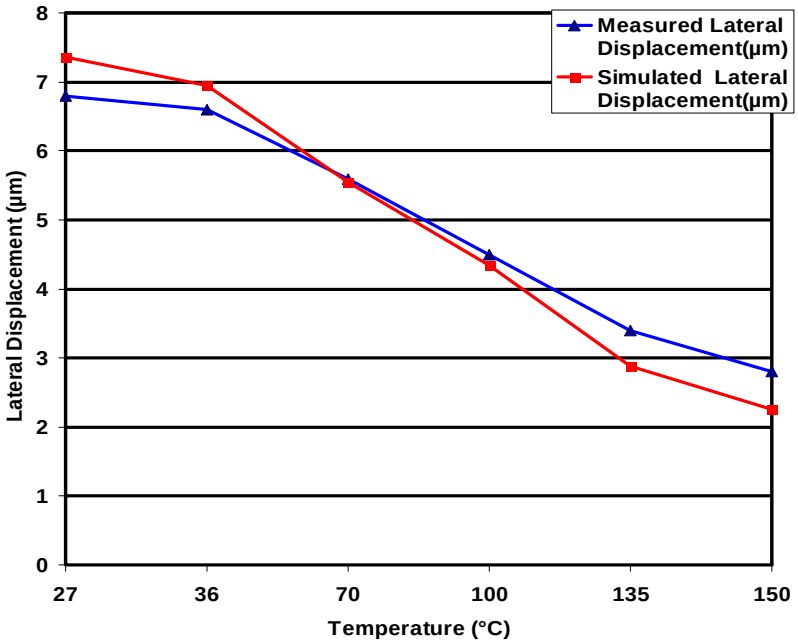

Figure.6. Measured and simulated (in Coventorware) lateral displacement comparison for the actuator in AMS 0.6 µm CMOS process with a length of 220 µm and a width of 22 µm at different temperature values, after it released.

Actuator Length × Actuator Width	Lateral Displacement
120µm × 22µm	2.9 µm
170 µm × 22µm	4.6 µm
220 µm × 22µm	6.8 µm

Table.2. Measured lateral displacement for different sizes of actuators in AMS 0.6 µm CMOS process.

Figure-6 is showing the simulated and measured lateral displacements for the actuator at different temperature values. There is a match between experiment and simulation data of within 10%. Table-2 is showing measured lateral displacement for different size of actuators in the AMS 0.6 µm process. In Figure-7, an actuator in the Agilent 0.5 µm CMOS process is shown. For most CMOS-MEMS processes, the residual stress gradient in the offset aluminum layers is tensile, while the residual stress gradient in the surrounding silicon oxide layers is compressive. In the Agilent process, the residual stress gradient in the aluminum layers appears to be more compressive than the surrounding silicon oxide layers, resulting in a residual stress gradient in the opposite direction when compared to the AMS process. Therefore, the actuator designs in the Agilent process displaced the opposite way of the intended direction.

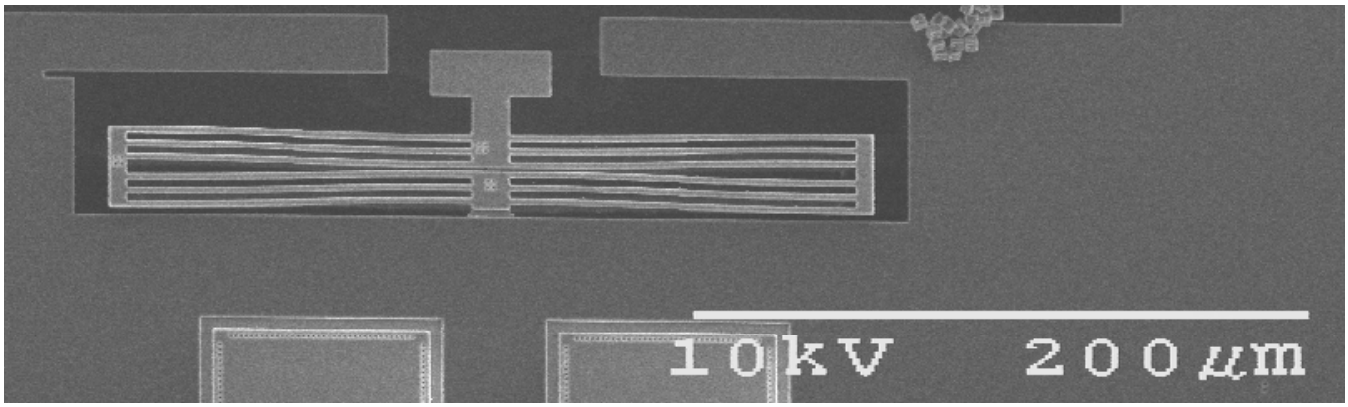

Figure 7. SEM of an actuator in the Agilent 0.5 µm CMOS process with a length of 216 µm and a width of 22 µm at room temperature, upon release.

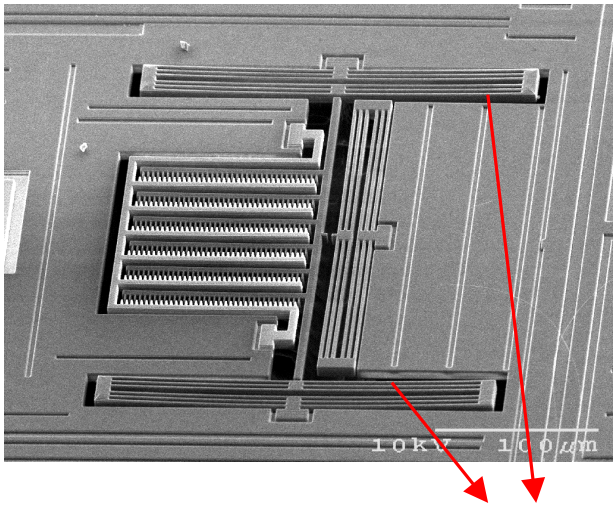

Figure 8. SEM of a released tunable capacitor in TSMC 0.35 µm CMOS process with full size actuators.

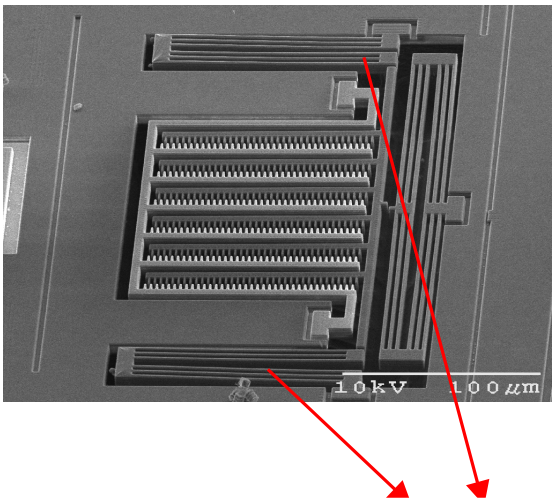

Figure 9. SEM of a released tunable capacitor in TSMC 0.35 µm CMOS process with half size actuators.

Second-generation electro-thermal actuator designs were fabricated in TSMC 0.35 µm CMOS. Figure-8 and Figure-9 show SEMs of two different actuator designs for RF MEMS tunable capacitors. In Figure-8, full-size actuators include embedded polysilicon heaters. In Figure-9, the half-size actuators are used. Again, the desired tuning operation is successfully tested with polysilicon heaters. Half-size actuators have advantages compared to full-size actuators of two times more area efficiency and almost half of the power consumption. The disadvantage of the half-size actuators is less stiffness. Additional beams, ideally in a symmetric arrangement, may be added into half-size actuators to increase the stiffness. Both kinds of actuators were tested by applying DC voltage to the polysilicon heaters. For full-size actuator with a length of 224 µm and a width of 22µm, 3.5 µm actuation is measured with 18 mW of heating power.

V. CONCLUSIONS

The important differences between this work and prior work are the high displacement magnitude with small geometry, pure lateral movement and the CMOS compatibility. The large actuation stroke in CMOS processes is particularly attractive for future tunable RF capacitors with large C_{on}:C_{off} ratio, and is an area of our active research. The impact of successfully creating such tunable on-chip passive components is in enabling the design of system-on-chip receivers. One of the biggest difficulties in designing tunable passives on chip is obtaining adequate area efficiency. Lateral displacement from the control of residual stress gradients can provide capability to self-assemble narrow nanometer gaps with zero input power. The nanometer-scale gaps are not possible to make through conventional lithography. These small gaps are essential for future applications of nanoresonator structures for use as RF filters and RF mixers. There can be other possible applications, such as RF switches and impedance matching networks.

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