INTEGRATED MEMS IN CONVENTIONAL CMOS

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1. Abstract

This paper provides an overview of fabrication and design of CMOS-based microelectromechanical systems with emphasis on inertial sensor and data storage applications. High-aspect-ratio (4.4:1) microstructures can be fabricated using conventional CMOS processing followed by a sequence of maskless dry-etching steps. The CMOS dielectric and metallization layers, normally used for electrical interconnect, serve a dual function as a composite metal/dielectric structural material. Reactive-ion etching produces near vertical sidewalls, enabling micromechanical beam widths and gap spacings down to 1.2 μm. The process is tailored for design of lateral electrostatic actuators as well as capacitive position and motion sensors. Tight integration of the microstructures with CMOS provides an opportunity to make low-noise sensor interface circuitry, and to include the signal processing needed to manage arrayed sensor-and-actuator systems-on-a-chip. Novel actuator and sensor topologies can be designed by embedding multiple isolated conductors into the microstructures. An additional post-CMOS processing sequence produces platinum tips on the movable microstructures. These tips are being explored for use in probe-based data storage and tunneling sensor applications.

2. Introduction

Future applications of MEMS are requiring microsystems that are increasingly complex and that are embedded with greater computational power. Applications include inertial measurement systems, digital light processors, infrared imagers, ultrasonic imagers, probe-based data storage, RF communications, and RF switching arrays. One promising approach to low-cost manufacturable integration of

MEMS and electronics is to start with a conventional CMOS process and build MEMS capabilities into it.

Direct integration of MEMS with electronics is desirable for systems with arrayed microsensors and microactuators on a single chip. On-chip electronics removes the interconnect bottleneck. For example, an array of 10,000 microsensors without integrated electronics requires at least 10,000 external connections. However, the signal processing needed to manage arrayed sensor-and-actuator systems can be placed on the chip in a CMOS-compatible MEMS process. Output signals can be electronically multiplexed or combined to reduce the number of off-chip connections.

Several key benefits to leveraging conventional CMOS processing for MEMS are that fabrication is fast, reliable, repeatable, and economical. There exist material limitations; most notable is the large vertical residual stress gradient in the microstructures, which must be overcome through design techniques. The CMOS-MEMS processes provide two specific performance advantages over similar technologies, such as integrated polysilicon MEMS. First, active devices can be placed directly next to microstructures, thereby virtually eliminating interconnect parasitic capacitance on high-impedance capacitive position sensor nodes. Second, multiple isolated conductors can be placed inside of suspended microstructures to create new capacitive sensors and electrostatic actuators for application in inertial sensors, resonator structures, and micropositioners.

3. Prior Work in CMOS-MEMS

In 1989, researchers at Simon-Frasier University were the first to report microstructures made from metal and dielectric thin films and directly integrated in standard CMOS processes [1]. In the basic process, illustrated in Figure 1 for two-metal CMOS, microstructures are made from combinations of aluminum, silicon oxide, and silicon nitride thin films. The metallization and dielectric layers, normally used for electrical interconnect, now serve a dual function as structural layers. Microstructural sidewalls are defined by stacking the drain/source contact cut and metal via cuts, and removing the metallization layers above the cuts. At the end of the CMOS processing, the substrate is exposed in the cut regions. Composite metal/dielectric (usually aluminum/oxide) microstructures are released by undercutting the silicon substrate, which acts as the sacrificial material. Wet-etch release may be accomplished using KOH, ethylene diamine pyrocatechol (EDP), or tetramethyl ammonium hydroxide (TMAH). Alternatively, researchers have used a dry etch release in a XeF_2 plasma [2] or in a SF_6:O_2 plasma [3] to prevent problems with sticking during release.

The contact-cut and metal-etch steps in the foundry CMOS process are tailored for planarized interconnect, not for creation of micromechanical structures. Since the contact cuts used to define the microstructures are not covered with

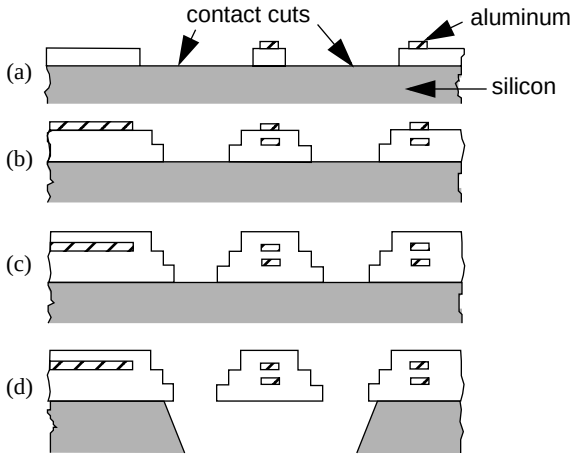

Figure 1. Cross sections of the stacked-contact-cut process. (a) After first metal, showing exposed oxide cuts. (b) After second metal, illustrating sequential stacking of cuts. (c) After pad overglass cut; microstructural sidewalls are fully defined. (d) After anisotropic wet silicon etch to release the microstructures.

metal, the layout violates the CMOS design rules. Incomplete etching of subsequent layers deposited on top of the cuts can result in formation of undesired metal and dielectric sidewalls. These sidewall films adversely affect the effective beam width by 1 μm or more. Very narrow lateral gaps cannot be fabricated because of the large topography of the oxide cuts, with the structure spacing being limited to about 10 μm for acceptable yield. Therefore, this process is primarily used for the manufacture of thermally isolated structures and vertically actuated structures. Current active research includes work on inertial sensors [4][5], biological cell force sensors [6], thermally operated gas flow sensors [7], and infrared detectors [8].

Various research groups have altered the basic post-CMOS process steps to form other kinds of MEMS. Micromechanical structures have been made using the gate polysilicon as the structural layer and field oxide as the sacrificial material [5]. Electrochemical wet etching has been used to fabricate thermally isolated transistors for true-rms power sensors [9]. The electrochemistry allows p-doped silicon to be preferentially etched, while not attacking n-doped silicon, thus resulting in suspended active devices in well regions undercut by the release etch. Microfluidic structures have been formed by wet etching the aluminum interconnect to form silicon dioxide capillaries on top of the substrate [10].

Currently, two foundry process services provide fabrication of CMOS-MEMS devices. In the U.S., MOSIS (the MOS Implementation Service) provides limited support to fabricate MEMS devices in certain CMOS processes (primarily AMI 1.2 μm) [11]. Future plans include full support of the post-CMOS silicon etch for release of microstructures. *Circuits Multi-Projets* (CMP) of France is the first

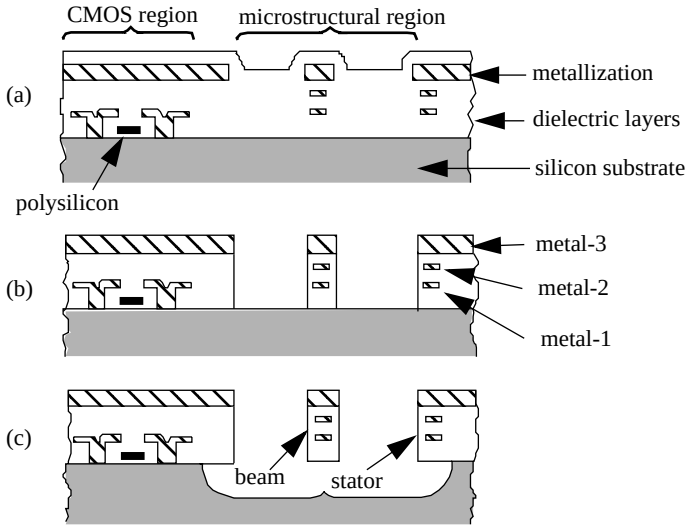

Figure 2. Flow for the high-aspect-ratio CMOS-MEMS process. (a) Conventional foundry CMOS. (b) After reactive-ion etch of the dielectric layers. (c) After dry plasma etch of the silicon substrate.

fabrication service outside of the U.S. to offer MEMS manufacturing in standard CMOS [12]. Their activity started in 1995, and has ramped to 16 MEMS multi-project runs in the ATMEL-ES2 1.0 µm CMOS process.

4. High-Aspect-Ratio CMOS-MEMS

One of the limitations of most CMOS-MEMS processes is the inability to create microstructures with narrow beam widths and narrow gaps for lateral electrostatic actuation and capacitive sensing. This drawback motivated our research group to develop a new set of post-CMOS process steps designed to create relatively high-aspect-ratio beams and gaps [3][13].

A simplified process flow is shown in Figure 2. First, standard CMOS is fabricated using the Hewlett-Packard 3-metal 0.5 µm n-well CMOS process available through MOSIS (Figure 2(a)). Separate areas must be partitioned for the CMOS electronics and for the microstructures. The first post-CMOS step is a CHF_3:O_2 reactive-ion etch (RIE), shown in Figure 2(b). The topmost metal layer acts as a highly selective mask which defines the microstructures. The RIE etches any dielectric (*i.e.*, overglass, intermetal oxide/nitride, and field oxide) that is not covered with metal. The Hewlett-Packard 0.5 µm process employs aluminum as the conductor material with tungsten-plug vias between metal layers. The top aluminum layer is partially eroded by ion milling during the RIE. The last process step,

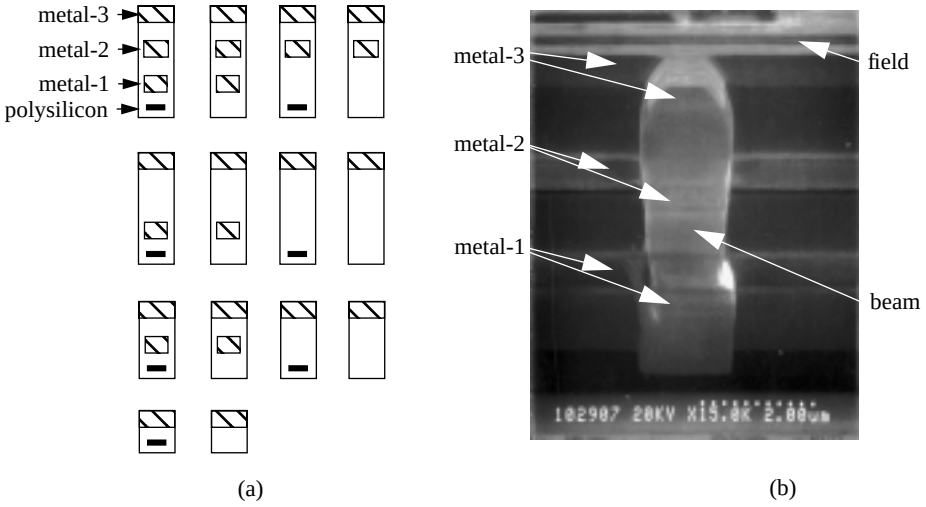

Figure 3. (a) The fourteen possible beam cross sections in the CMOS-MEMS process using 3-metal CMOS. An overlap between the top metal and underlying conductors is shown. (b) SEM of the end of a minimum width, metal-3/metal-2/metal-1 beam with no overlap (as drawn) between metal layers. Note the misalignment in the metal-1 layer causes a step in the sidewall. The 3-metal field can be seen in the background.

shown in Figure 2(c), is a dry SF_6:O_2 plasma etch of the silicon substrate. The plasma chemistry etches silicon without attacking the microstructural sidewalls. The etch is timed to undercut structures up to 16 µm wide. Larger structures must have etch holes for proper release.

The resulting microstructures are made of composite beams with near vertical sidewalls and beam widths and gaps down to 1.2 µm. As shown in Figure 3(a), it is possible to design fourteen different beam cross sections using combinations of the three metal layers and the gate polysilicon. The second-thickest beam section, shown in Figure 3(b), includes all three metal layers: metal-3, metal-2, metal-1; these beams are around 5.3 µm tall with an maximum aspect ratio of around 4.4:1. In principle, conventional electrical design rules dictate the minimum metal width and spacing, and therefore dictate the minimum beam widths and air gaps. However, the air gap is currently limited to 1.2 µm instead of the metal-to-metal spacing of 0.9 µm, because of polymerization issues stemming from the dielectric RIE. Narrow beams enable design of very compliant lateral suspensions, and the small air gaps enable design of lateral electrostatic actuators with relatively high force. These capabilities are useful in accelerometers, vibratory-rate gyroscopes, micropositioners, and micromechanical resonators.

One corner of a released electrostatically actuated lateral resonator, is shown in Figure 4. This device has very narrow beam widths and gap spacings, which are features normally associated with polysilicon microresonators [14]. The interdigi-

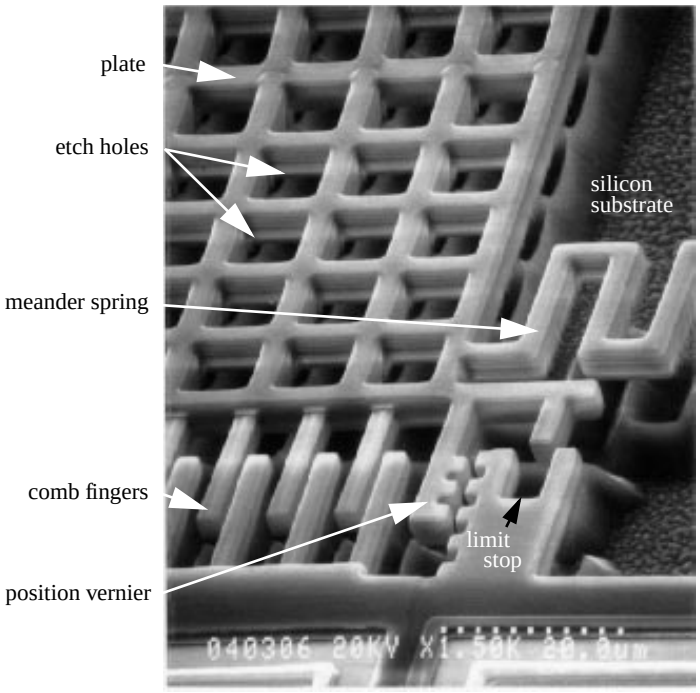

Figure 4. SEM of a section of a lateral comb-drive microresonator after the silicon etch has released the structure. The noted features demonstrate the successful fabrication of very small beams and gaps in conventional CMOS.

tated comb fingers and compliant meander springs are 2.4 μm wide and 4.8 μm thick with gaps of 1.6 μm between fingers. Etch holes allow the large plate to be released. Silicon ridges are present about 10 μm below the suspended structure and result from the slightly anisotropic release etch. Embedded aluminum traces wind through the meander springs to provide interconnect between the comb fingers and bond pads. The resonator plate mass experiences an electrostatic attractive force upon application of a potential across the gap between comb fingers.

Mechanical material properties are not a primary concern for CMOS foundries, which focus on reliably producing electronic circuits, not MEMS. As a result, CMOS-based microstructures can suffer from large residual stresses and stress gradients, which may vary from run to run. Residual stress has been measured using bent-beam strain test structures [15]. The 3-metal composite beam has an in-plane residual stress of 69 MPa, corresponding to a strain of 1.1×10^{-3} and a buckling length of 65 μm for a 1.2 μm-wide fixed-fixed beam.

Vertical stress gradients due to the composite nature of the structures cause curling out of the plane of the substrate. Curl of eight different kinds of beams are

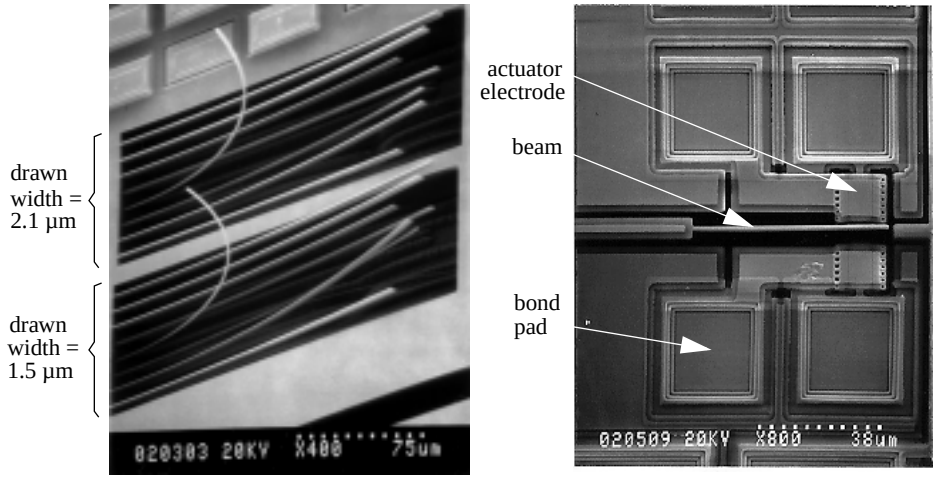

Figure 5. Initial CMOS-MEMS characterization structures. (a) Cantilever structures showing various amounts of curling depending on beam type. The beam type is from top to bottom: m1-m2-m3, m2-m3, m1-m3, m1-m2, m1, m2, m3, poly-m1-m2-m3. The metal-1 beam exhibits the maximum curl. Curling increases as the beams width decreases. (b) Cantilever beam resonator for stiffness measurement.

shown in Figure 5(a). The radius of curvature of these beams varies between 1 to 14 mm and depends on both the beam cross section and the beam width. The measured tip displacement of several 1.4 mm-long, 3.6 µm-wide, 4.8 µm-thick 3-metal beams over several process runs was 200 ± 30 µm, which corresponds to a nominal radius of curvature of 4.9 mm and a strain gradient of $2x10^{-4}$/µm. The variation is due in part to modification in the post-processing over time, which can alter the beam cross section. However, curling of beams on a given die is matched. A more systematic investigation of strain gradient variation from run to run is an important next step in our research.

The 3-metal composite beam in the HP 0.5 µm CMOS-MEMS process has an effective Young's modulus value of 52 GPa. This value was determined by fitting the resonant frequency of three matched cantilever beams of differing lengths. A typical beam resonator test structure is shown in Figure 5(b). The density of the aluminum, oxide, and nitride films are assumed to be 2700 kg/m^3, 2500 kg/m^3, and 3100 kg/m^3, respectively.

We have qualitatively observed deflected cantilever beams sticking to laterally adjacent surfaces. However, the beams can be pulled away from the surface using a micromechanical electrostatic actuator generating on the order of micronewtons of force. If this action can be shown to be reliable, then devices can be designed to

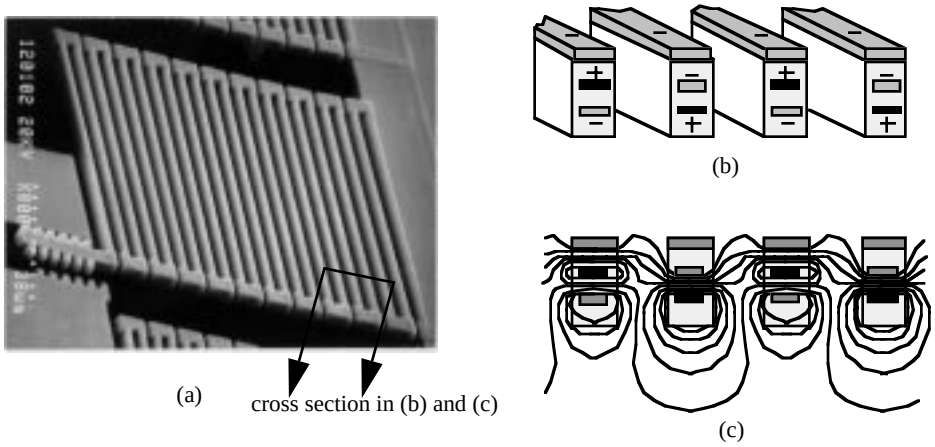

Figure 6. The self-actuating spring. (a) SEM of a self-actuating spring with 22 meanders. A vernier, shown at the left of the SEM, is used to measure position. (b) Schematic cross section showing voltage polarity of the embedded conductors. (c) Cross section showing electric equipotentials.

recover from contact. Future characterization and understanding of surface charging and lateral contact forces will be essential in developing robust devices.

5. CMOS-MEMS Design

As discussed previously, the CMOS-MEMS fabrication technology is a relatively low cost method for fabricating integrated MEMS. The primary drawback of CMOS-MEMS is the inability to optimize the mechanical properties of the microstructures, which can limit the performance of certain devices. The disadvantage of variability of the mechanical parameters can be mitigated through design in many important cases. In particular, microstructures can be designed with matched curling to ensure a high value of lateral air-gap capacitance between sensors and actuators. Although the mechanical structures pose challenging design problems, the CMOS-MEMS process does have two important performance advantages: multiconductor structures, and ultra-low parasitic capacitance. For some complex MEMS applications, these advantages may outweigh the disadvantages.

One performance advantage of CMOS-MEMS is that independent, isolated conductors may be embedded into a single suspended microstructure. This ability opens up new design possibilities like the self-actuating spring, shown in Figure 6. Two differential voltages (+ and -), applied to conductors embedded in the meanders, alternate connection between the metal-2 and metal-1 layers by swapping the wiring at the ends of each meander. The resulting electrostatic force laterally com-

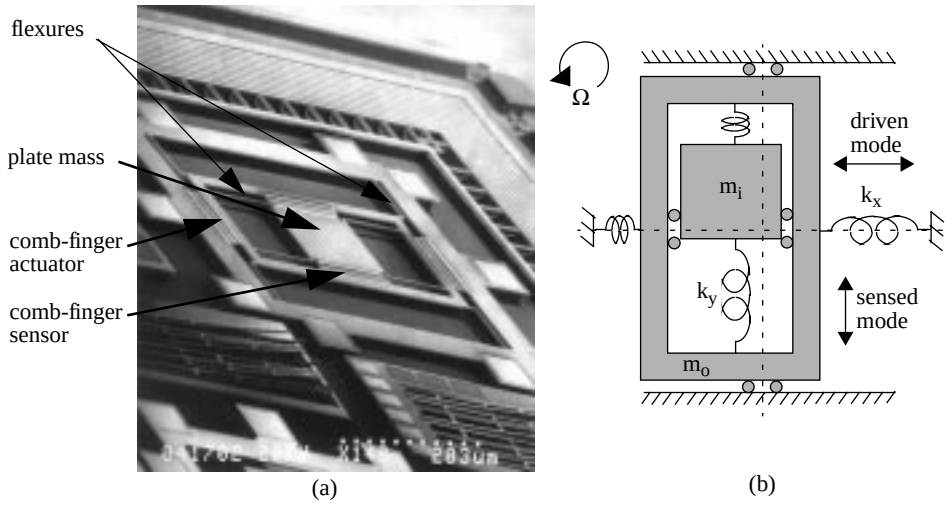

Figure 7. The elastically gimbaled gyroscope. (a) SEM. (b) Schematic of basic operation.

presses the spring with increasing applied voltage. Such actuators and sensors are impossible to design using homogeneous polysilicon microstructures.

In another example, completely independent electrostatic actuators and sensors are designed into the elastically gimbaled vibratory-rate gyroscope shown in Figure 7 [16]. The inner proof mass, m_i, and springs k_y are nested within a surrounding outer frame, m_o, and driven in resonance in the x direction by an electrostatic comb drive. A Coriolis force proportional to external rotational rate, Ω, is produced in the y direction of the rotating reference frame of the gyroscope. The resulting motion of the inner proof mass in the y direction is sensed with an independent comb-finger sensor. The actuator and sensor are mechanically decoupled, thereby eliminating mechanical crosstalk and reducing errors coupled into the sensor from the driven mode. The decoupled design also allows for independent optimization of the driving and sensing elements.

The second performance advantage of CMOS-MEMS is the very low parasitic capacitance of interconnect from the micromechanical device to the electronics. Current integrated polysilicon MEMS technologies suffer from junction capacitance of heavily doped silicon interconnect, or from anchor pad capacitance to substrate. Parasitic capacitance from external bond-wire or solder-bump flip-chip connections is between 100 fF-1 pF. For comparison, a moderate-sized micromechanical lateral capacitive sensor in a surface micromachining technology (including CMOS-MEMS) has a total capacitance value of around 10 fF. Therefore, even a few femtofarads of parasitic capacitance will degrade the sensitivity substantially.

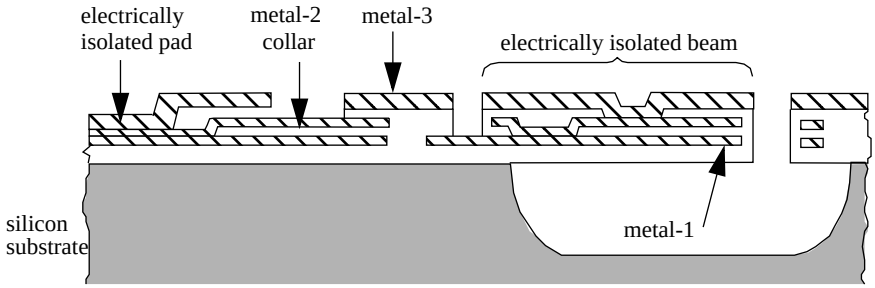

Figure 8. Cross-section of interconnect for electrical isolation.

In CMOS-MEMS processes, the minimum spacing between active devices (*e.g.*, transistors and diodes) and micromechanical components is dictated by the silicon release etch, since the active devices are made from the silicon. An anisotropic wet silicon release etch can preserve the silicon almost up to the edge of the etch pit, due to the high selectivity to <111> crystal planes. The isotropic dry plasma release in the high-aspect-ratio CMOS-MEMS process undercuts the silicon at the anchored edges. Typically, active devices can be placed as close as 12 µm from the microstructures, corresponding to a parasitic capacitance of 1.7 fF. This very low capacitance can be exploited to make ultra-sensitive displacement sensors.

Because a protective metal layer (usually metal-3) is required to prevent the CMOS electronics from etching, at most two unconstrained metal layers are left available for electrical interconnect. Measurements of transistor threshold voltage verify that there is no degradation from either the dielectric or silicon etch.

A gap in metal-3 is necessary for electrical isolation between external pads and the rest of the metal-3 plane. The interconnect arrangement is shown in Figure 8. A metal-1 or metal-2 collar is inserted underneath the break in metal-3 to prevent the silicon etch from reaching the substrate surface. Such gaps in metal are also used to electrically isolate different conducting areas on suspended structures.

6. Probe-Based Data Storage

The post-CMOS processing sequence may be modified to fabricate platinum tips on the movable microstructures as shown in Figure 9(a). These tips are being explored for use in probe-based data storage and tunneling sensor applications. In the probe-based storage application, the tips are used to write and detect pits on the surface of an amorphous carbon media, as illustrated in Figure 9(b). Initial tests using a commercial scanning tunneling microscope have been successful in writing pits as small as 3 nm in size by pulsing voltage in the range of 4-6 V. The pit can be

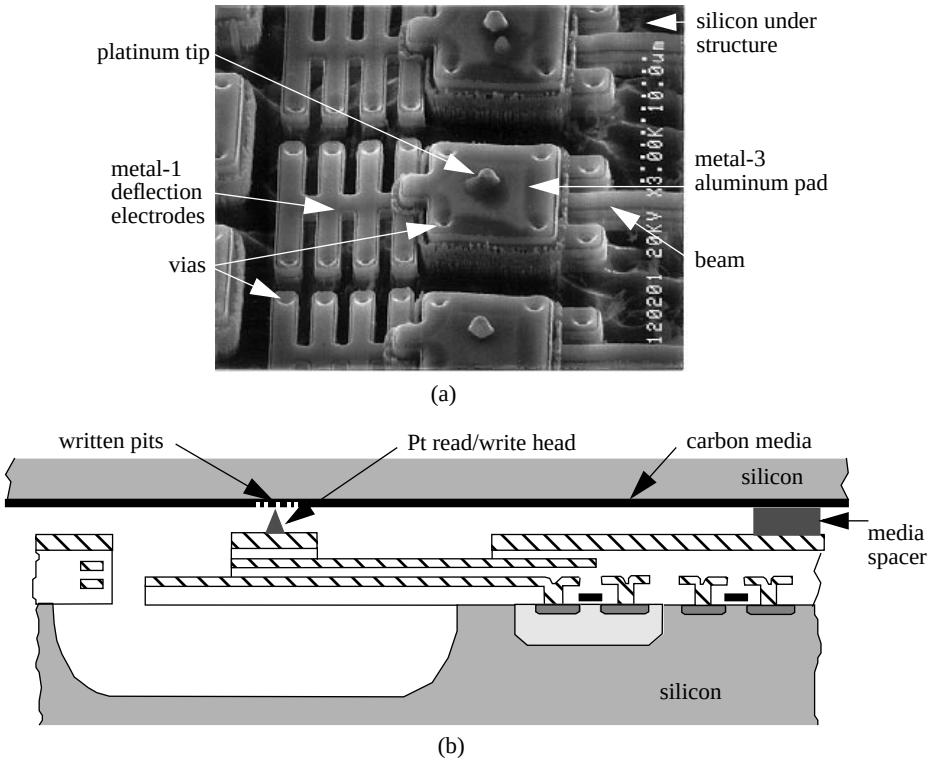

Figure 9. Probe-based data storage application. (a) Platinum tips deposited on CMOS-MEMS structures. (b) Schematic cross-section of the write-once-read-many (WORM) system.

subsequently read by detecting the change in tunneling current as the tip is scanned over the media. By controlling up to 10,000 tips on a single chip with each tip being scanned in a 10 μm by 10 μm area, data storage densities of 10 GB/cm^2 may be possible. Presently, we are studying narrow-gap lateral electrostatic actuators for microstages having a high percentage of swept area to device area. Cantilevered stages have moved up to ±5 μm linear static displacement with 15 V applied to the actuators. Reliable operation of future MEMS probe-based storage systems will require an understanding of the physical mechanisms underlying the reading and writing of data, as well as knowledge of the tribology of the contact surfaces between the tip and media.

7. Conclusions

Many of the manufacturing difficulties with fabricating MEMS in a standard CMOS process stem from the inability to control the microstructural sidewall

geometry when using the stacked-contact-cut technique. These problems are solved by moving the microstructural etch from the main CMOS flow to an optimized post-processing step. The resulting process can produce microelectromechanical devices with narrow beam width and gap spacing as required for lateral electrostatic actuation.

We have developed several CMOS-MEMS that take advantage of the multiconductor structures and low parasitic capacitance, and demonstrate the potential for inertial sensor and probe-based data storage applications. Further work must be done on characterizing the composite material of the CMOS-MEMS structures, however design matching techniques can compensate for problems with out-of-plane curling and residual stress. Future designs will integrate sense electronics with efficient actuation mechanisms for higher performance.

The probe-based data storage is an important future MEMS application. WORM data storage can be accomplished using the platinum-tip and carbon media system, but other combination of tip and media must be developed for read-write storage. Research in read-write physical mechanisms and in tribology of such tip and media systems is critical for implementation of reliable MEMS data storage systems.

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