

Preface

Market competition and the astounding pace of technological innovation exert tremendous pressure on circuit design engineers to turn ideas into products quickly and get them to market. In digital Application Specific Integrated Circuit (ASIC) design, computer aided design (CAD) tools have substantially eased this pressure by automating many of the laborious steps in the design process, thereby allowing the designer to leverage his design expertise. For example, general purpose digital synthesis techniques that can reliably transform a behavioral circuit description into a collection of gates allow designers to focus on the more abstract and understandable behavioral description of the design.

But the world is not solely digital.

Cellular telephones, magnetic disk drives, neural networks and speech recognition systems are a few of the recent technological innovations that rely on a core of analog circuitry and exploit the density and performance of mixed analog/digital ASICs. To maximize profit, these mixed-signal ASICs must also make it to market as quickly as possible. However, although the engineer working on the digital portion of the ASIC can rely on sophisticated CAD tools to automate much of the design process, there is little help for the engineer working on the analog portion of the chip. With the exception of simulators to verify the circuit design when it is complete, there are almost no general purpose CAD tools that an analog design engineer can leverage to automate the analog design flow and reduce his time to market.

This does not mean that no one has attempted to create general purpose analog CAD tools. Although there is little discussion of synthesis of analog circuits from a behavioral model, there has been significant effort in the area of synthesis for performance. This kind of synthesis assumes a known qualitative behavior, such as amplification, and seeks to design a circuit that meets the many performance specifications that quantify that behavior. Unlike digital design, a set of 30 or more different performance specifications is not unusual for a single circuit, and most of these are difficult to evaluate even when given the circuit solution, making for a daunting synthesis task. Despite the best efforts of researchers, to industrial analog designers most of the analog synthesis tools published to date have been little more than a curiosity. These tools typically encode circuit-specific performance evaluation code or even a customized design strategy. As a result, these tools work for only a predetermined handful of circuits and over a limited range of performance. Moreover, the circuits produced are not comparable to those produced by the manual design process, often suffering from poor performance or the inability to tolerate the inevitable variations in manufacturing process or operating environment. Because of these limitations, these analog synthesis tools are poor cousins to their digital counterparts. Analog designers continue to wait for an analog synthesis tool that is practical: a tool that can automate part of the design process, leveraging the efforts of an experienced analog designer; that does not have a fixed circuit library but can be applied to a broad range of analog design problems; and that can synthesize variation-tolerant, high-performance circuits.

In this book, we present a new variation-tolerant analog synthesis strategy that we believe is a significant step towards ending the wait for a practical analog synthesis tool. We present a new synthesis strategy that can automate fully the path from a circuit topology and performance specifications to a sized variation-tolerant circuit schematic. This strategy relies on asymptotic waveform evaluation to predict circuit performance and simulated annealing to solve a novel non-linear infinite programming optimization formulation of the circuit synthesis problem via a sequence of smaller optimization problems. We have implemented this strategy in a pair of tools called ASTRX and OBLX. ASTRX is a circuit compiler that generates a performance prediction module that maps the component and voltage values in the circuit to the performance metrics specified by the user. More exactly, ASTRX generates code that implements a cost function that is carefully constructed so that its minimum value occurs at a circuit design that best meets the input specifications. This cost function code is then compiled and linked to OBLX, which uses simulated annealing to solve numerically for its minimum, thereby designing the circuit.

To show the generality of our new approach, we have used this system to re-synthesize essentially all the analog synthesis benchmarks published in the past decade; ASTRX/OBLX has re-synthesized circuits in an afternoon that, for some prior approaches, had required months. To show the viability of the approach on difficult circuits, we have re-synthesized a novel, published, patented, high-performance operational amplifier; ASTRX/OBLX achieved performance comparable to the expert manual design. To test the limits of the approach on industrial-sized problems, we have synthesized the component cells of a pipelined A/D converter; ASTRX/OBLX successfully generated cells 2X-3X more complex than any published to date. Finally, to show the ability of our tools to create variation-tolerant circuits, we use them to design analog cells that are insensitive to operating range and manufacturing line variations; ASTRX/OBLX completed the novel synthesis task of designing a band-gap circuit that is stable over temperature and process variations.

This work is the culmination of more than five years of research in the Center for Electronic Design Automation (CEDA) at Carnegie Mellon University. The research groups within CEDA provided a forum to discuss the many ideas on which this book is based: Team Rob, the Analog Circuit Group, the ACACIA Group, the AWE Group, and in particular the optimization group that formed briefly for the summer of 1991 helped guide this research in a profitable direction. We would also like to thank the many people who have contributed to this work through direct guidance or simply via beneficial conversations over the years. Our thanks go to Bulent Basaran, Erik Carlson, Dennis Ciplickas, John Cohn, Peter Feldmann, Dave Garrod, Ramesh Harjani, Rajeev Jayaraman, John Lee, John Kibarian, Kannan Krishna, PC Maulik, Sujoy Mitra, Sudip Nag, Katsu Nakamura, Vivek Raghavan, Bob Stanisic, Professor Stephen W. Director, Professor Ignacio Grossman, Professor Ron A. Rohrer, and Scott Kirkpatrick.