MECHANICAL NOISE-LIMITED CMOS-MEMS ACCELEROMETERS

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ABSTRACT

The latest generation of CMOS-MEMS accelerometer has measured mechanical Brownian noise-limited resolution of 45 μg/$\sqrt{\text{Hz}}$ at 1 atm. A modified pre-amplifier design with sub-threshold transistor dc biasing is robust against leakage paths to positive and negative supplies and has an input referred noise of 14.6 nV/$\sqrt{\text{Hz}}$ at the 2 MHz modulation frequency. The accelerometer proof mass is purposely sized to have equivalent mechanical Brownian noise. An array approach to improve the noise floor further is proposed and fabricated.

INTRODUCTION

There has been considerable research effort on capacitive MEMS accelerometers made directly within foundry CMOS metal and dielectric layers [1][2][3]. Due to the integration of sensing circuits and MEMS transducers, CMOS-MEMS accelerometers have potential advantages over hybrid solutions of smaller die size, higher sensitivity and ability to place digital signal processing on chip for semi-custom applications. Some of these integration advantages are exploited in commercial thermal-based CMOS-MEMS accelerometers, achieving 1 mg/$\sqrt{\text{Hz}}$ resolution with 30 Hz bandwidth [4]. A CMOS-MEMS piezoresistive accelerometer achieved 3 g equivalent noise in a 500 Hz bandwidth [5]. A best performance of 50 μg/$\sqrt{\text{Hz}}$ for a CMOS-MEMS capacitive accelerometer was achieved with chopper-stabilized sensing and periodic bias reset [6].

The CMOS-MEMS microstructures are made with a matured post-CMOS fabrication flow [7]. All process steps use dry chemistry and therefore avoid stiction problems after release. First, custom designed chips from CMOS foundries are etched by directional RIE with etchant gases of CHF_3 and O_2 until the silicon substrate is exposed. Structural sidewalls are defined by the first metal layer encountered by the RIE. The circuits are protected with the top metal layer or by a thick photoresist mask. The extra photoresist mask is necessary for release of die greater than about 9 mm^2 to suppress sidewall polymerization from resputtered aluminum incorporated in the plasma. Multi-thickness structures are achieved by using different metal layers as the mask (four metal layers are available in the processes used here). In the second process step, the silicon substrate is etched by DRIE to set a fixed distance from the substrate, then isotropically etched with SF_6 RIE [7]. In order to prevent the circuits from being destroyed during the release etching process, a conservative distance of 60 μm is maintained between transistors and the nearest etch pit opening.

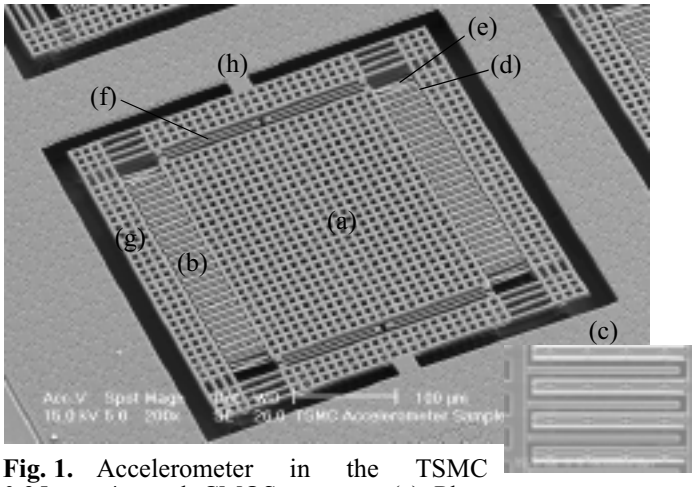

Fig. 1. Accelerometer in the TSMC 0.35 μm 4-metal CMOS process. (a) Plate mass. (b) Sense fingers. (c) Sense finger close-up. (d) Self-test fingers. (e) Finger limit stops. (f) Spring. (g) Stator curl-matching frame. (h) Anchor.

Capacitive sense circuits for accelerometers adopt either continuous-time or switched capacitor architectures. The continuous-time topology, explored here, is simple and avoids noise sources from switching and aliasing. A pre-amplifier detects the signal, which is modulated electronically at 2 MHz, from the sense capacitor bridge. However, achieving a robust dc bias of the pre-amplifier, while simultaneously minimizing parasitic capacitance to substrate, is a challenge. Approaches to biasing include connecting the bias reference voltage to the high-impedance node through long-channel transistors, diode-connected transistors, and periodic switching transistors. The pre-amplifier used here is adopted from the design in [3], which is biased through a sub-threshold transistor to the drain of the input transistor.

ACCELEROMETER DESIGN

An accelerometer micromachined from the 4-metal TSMC 0.35 μm CMOS process, is shown in Fig. 1. Similar accelerometers were also designed in the Jazz Semiconductor 4-metal 0.35 μm SiGe BiCMOS process with identical topology and similar transducer sizing. The accelerometer has four major sections: a curl match frame, comb sense and self-test fingers, meander springs and a plate mass. The curl match frame is employed to align the sidewalls of the rotor and stator comb fingers in the presence of out-of-plane curling arising from residual and thermal stress gradients [3]. To be most effective, the curl match frame has the same beam geometry and layer composition as the plate mass and comb fingers. As seen in Fig. 2, although the maximum displacement above the substrate due to residual stress gradient is 3.87 μm at the corners of the frame, the curl

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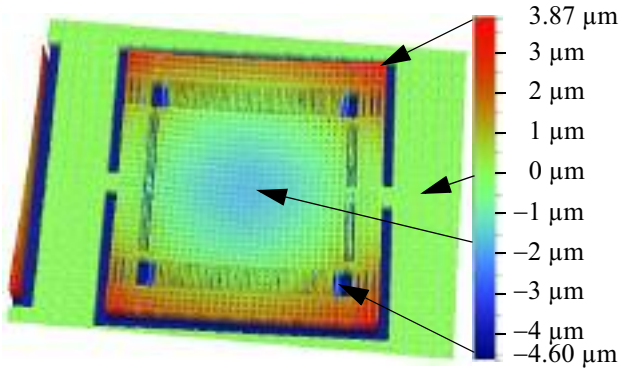


Fig. 2. Out of plane curl measurement from WYCO profilometer. The metal-1 beams start -4.6 µm below the field.

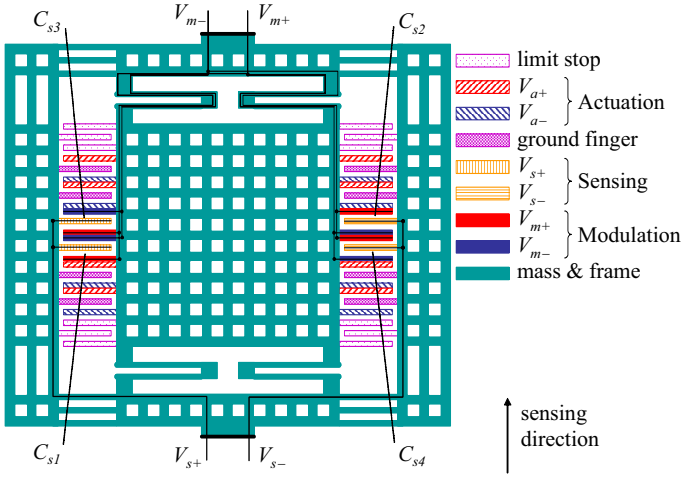


Fig. 3. Simplified layout of the CMOS-MEMS accelerometer. There are 20 sensing fingers on each side of the stator frame, although only 2 sensing fingers are shown here on each side.

matching keeps adjacent comb finger sidewalls aligned to within 0.1 µm. The finger topology is illustrated in Fig. 3. To reduce the parasitic capacitance to substrate, the high-impedance sense fingers are located on the curl match frame (i.e., the stator). The stator routing is shorter since it does not meander through the springs. Single actuation fingers are located at each corner of the plate to provide electrostatic force for self-testing. Shock protection fingers have slightly smaller gaps to act as limit stops. These fingers are made from the CMOS metal-1 layer and bend upward to inhibit jump over and mechanical latching of fingers after high-shock events.

Narrow spring beams can suffer from in-plane curling caused by manufacturing misalignment of embedded metal layers that creates a stress gradient. Slight displacement as small as 10 nm is equivalent to several g of offset. To minimize the offset, spring beams are designed to have a tapered cross-section [8]. Metal cut-in of 0.2 µm is adequate to compensate the misalignment, as evidenced by the equal gaps seen in Fig. 1(c).

The sensing fingers are connected as a fully differential capacitive bridge with balanced modulation, V_m, as shown in Fig. 4. The high-impedance capacitive divider lines are routed to the on-chip differential pre-amplifier. The arrangement of the sense capacitors, $C_{S(1,2,3,4)}$, is noted in Fig. 3. Parasitic capacitances, C_p, in the schematic include routing capacitance to substrate and the pre-amplifier input capacitance.

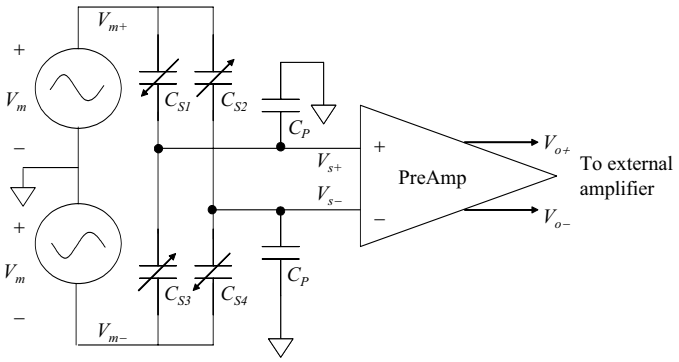


Fig. 4. Simplified sensing schematic.

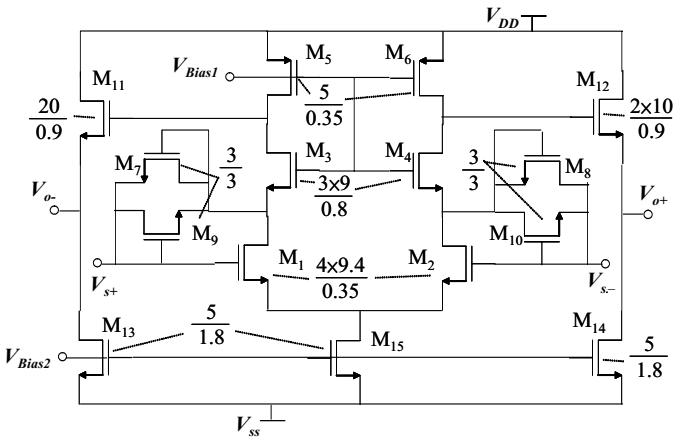


Fig. 5. Pre-amplifier schematic. The values are W/L ratios for the transistors in the TSMC 0.35 µm CMOS accelerometer.

PRE-AMPLIFIER DESIGN

The pre-amplifier circuit schematic is shown in Fig. 5. The differential output from the first stage is taken between the M_3 and M_4 cascode transistor drains and the p-channel load transistors M_5 and M_6. Source follower circuits using M_{11}-M_{14} drive bondpad capacitance. Replica biasing sets the bias voltages, V_{Bias1} and V_{Bias2} for 200 µA current in M_{11} to M_{15}. The supply voltage is 5 V.

Transistors M_7-M_{10} operate to stabilize the dc bias of the pre-amplifier input nodes to remain at the drain voltage of the input transistors, M_1 and M_2. The cascode transistors M_3 and M_4 are necessary to fix these drain voltages. Without the bias stabilization transistors, leakage current paths would charge the input gate capacitance to the power supply rails. A leakage current path to the negative supply lowers the voltage on the input gates, causing transistors M_7 and M_8 to turn on, while M_9 and M_{10} remain off. The leakage current is very small, so the transistors sustain bias while remaining in their sub-threshold region of operation. A leakage current path to the positive supply raises the voltage on the input gates, causing transistors M_9 and M_{10} to turn on, while M_7 and M_8 remain off. The prior design in [3] did not incorporate M_9 and M_{10} and was susceptible to bias drift toward the positive supply. To simulate the leakage current, a

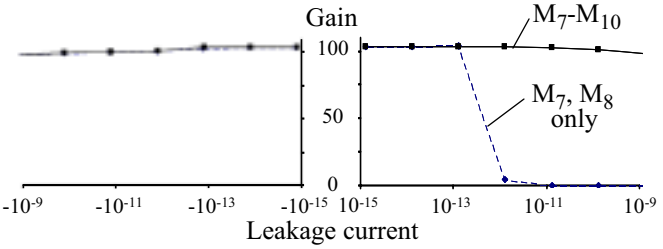


Fig. 6. Simulated pre-amplifier gain as a function of leakage current. The circuit with a single n-channel feedback dc bias transistor on each input saturates at around 5 pA leakage current, resulting in a loss of gain.

resistor is added between the output node of the capacitive bridge and V_{dd} or V_{ss}. The simulated results of pre-amplifier dc gain with different leakage currents are shown in Fig. 6. The circuit bias with M_7-M_{10} is stabilized in the presence of nA leakage current to either supply rail.

ANALYSIS

The transducer equivalent differential voltage seen at the pre-amplifier input is

$$V_{s+} - V_{s-} = \frac{C_{S1} + C_{S4} - C_{S2} - C_{S3}}{C_P + 2C_{So}} V_m \qquad (1)$$

where C_{So} is the nominal sense capacitance.

The major noise sources are Brownian noise and input-referred noise of the pre-amplifier. The Brownian noise is dominated by the squeeze film damping between the sensing fingers,

$$B = \mu \frac{L_{ov} h^3}{g^3} \qquad (2)$$

where μ is air viscosity, L_{ov} is the finger overlap (38.4 μm), h is the finger thickness (6.9 μm) and g is the gap (layout 1.5 μm, measured 1.2 μm). The equivalent acceleration noise is

$$\frac{a_n^2}{\Delta f} = \frac{4 k_B T B}{m^2} \qquad (3)$$

where k_B is Boltzmann's constant and T is temperature. The calculated Brownian noise is 43 μg/$\sqrt{\text{Hz}}$.

CMOS transistor electronic noise is well known to be dominated by flicker noise at low frequency and thermal noise at high frequency. The 2 MHz modulation frequency used in operation is high enough that flicker noise can be neglected. The pre-amplifier input referred noise is

$$\frac{v_n^2}{\Delta f} = \frac{8}{3} k_B T \frac{1}{g_{m1}} \left(1 + \frac{g_{m3} + g_{m5}}{g_{m1}}\right) \qquad (4)$$

where g_{mi} is the transconductance of transistor M_i, adjusted for short channel FETs (L < 1.7 μm) [9].

Transistors in the pre-amplifier are sized to minimize the total input-referred noise while keeping −3 dB bandwidth well above 2 MHz and maintaining a large enough dc gain to reduce the noise effect caused by the cascading stages. A series of parametric analysis for width and length of each transistor were performed in the TSMC 0.35 μm CMOS technology.

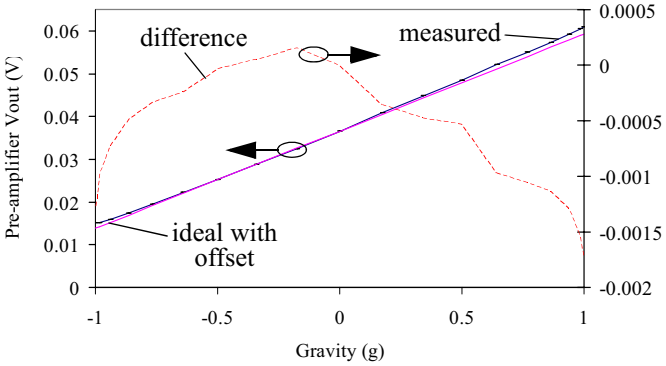


Fig. 7. Static sensitivity measurement from tilt test.

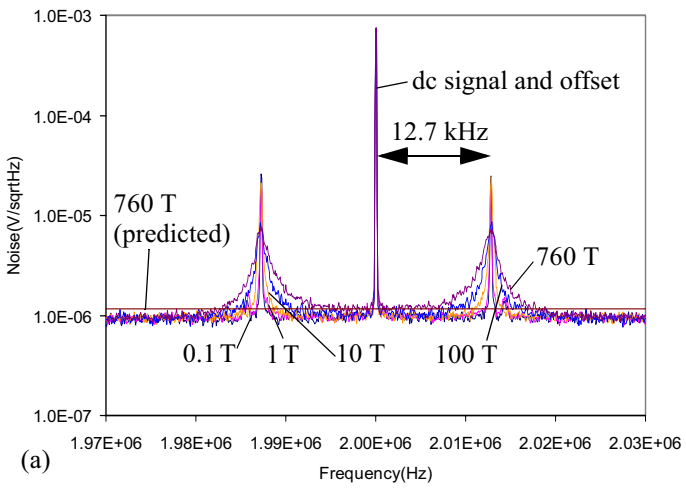
Since transconductance scales roughly as $\sqrt{W/L}$, noise is decreased and gain increased by designing larger W/L for M_1 and M_2 and smaller W/L for M_3 through M_6. There is a trade off in bandwidth when increasing the length of the M_5 and M_6 loads and width for the cascode M_3 and M_4 transistors. The size of the source follower may be decreased to compensate, at the expense of less ability to drive output bondpad capacitance.

The pre-amplifier input-referred SNR was simulated, with fixed settings of $\Delta C_S = 0.01$ fF, $C_S = 40$ fF, $C_P = 100$ fF and $V_m = 1$ V. The lowest noise pre-amplifier does not result in the largest SNR design. From (1), the transducer gain is attenuated by the input gate capacitance, included as part of C_p, and thus there is an optimal point where SNR is largest. The optimal values for widths and lengths, given in Fig. 5, were found using the optimizer in Cadence Spectre with a goal to have maximum SNR and bandwidth with the same weighting. This pre-amplifier in the TSMC process has simulated 13.3nV/$\sqrt{\text{Hz}}$ input referred noise, a DC gain of 104, and a −3dB bandwidth of 37.1 MHz.

RESULTS

The measured pre-amplifier gain was 68.7 and input-referred noise was 14.6 nV/$\sqrt{\text{Hz}}$ at 2 MHz. The accelerometer resonant frequency was 12.7 kHz measured by a MIT microvision system, corresponding to a mechanical gain of 1.5 nm/g. Parameters calculated from layout measurements include a proof mass of 1.04 μgram and $C_p = 65.9$ fF. Static sensitivity, shown in Fig. 7, was measured with modulation voltage of 1 V at 2 MHz on a rotational table to adjust the tilt angle. The gain was 23 mV/g. The 35 mV offset is from 2.3 nm of average lateral offset, which could be from a number of factors including lateral curl or surface roughness.

The noise behavior was measured with a spectrum analyzer under different pressure and modulation voltage as shown in Fig. 8. No external forces aside from Brownian noise are driving the accelerometer. The peaks at both sides of the 2 MHz carrier agree with the mechanical resonant frequency of 12.7 kHz. By changing environment pressure and modulation voltage, the noise floor from mechanical limits is verified. The peaks narrow at lower pressure, as expected. The noise floor between 1.98 MHz and 2.02 MHz is primarily mechanical noise with an equivalent value of 45 μg/$\sqrt{\text{Hz}}$ at 760 T at mechanical frequen-



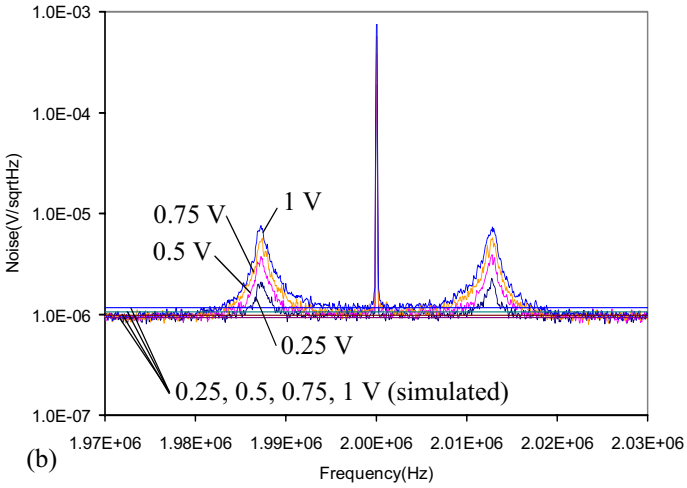


Fig. 8. Noise measurement (a) with varying pressure and (b) with varying modulation voltage amplitude.

cies below resonance. The predicted noise level at 760 T in Fig. 8(a) is found by combining (3) with the preamplifier electronic noise. Predicted and measured data agree. Lowering the modulation voltage, as in Fig. 8(b), decreased the transducer gain and reduced Brownian noise seen at the input of the pre-amplifier.

The optimal design for lowest noise occurs when Brownian noise and electronic equivalent acceleration noise are equal. Although increasing mass is the most effective way to decrease Brownian noise, the maximum realizable size in CMOS-MEMS is limited to around 500 µm on a side due to in-plane compressive stress and stress gradients. Another technique for reducing Brownian noise is to decrease damping force by reducing the sense capacitor height or increasing the gap. The optimal sense capacitance, for a fixed pre-amplifier design, occurs when $C_{so} = C_P$, since further reduction will also reduce sensitivity.

If N accelerometers are arrayed, noise can be reduced still further. Brownian noise drops with a slope of $1/\sqrt{N}$ while electronic noise drops with a slope of $1/N$. For large N, the accelerometer will always become Brownian noise limited. A fabricated out-of-plane 40-accelerometer array designed for high bandwidth is shown in Fig. 9. Each accelerometer cell is a simple cantilever beam spring and folded-finger mass. The spring serves as a curl match element while the mass serves as the electrode for the capacitive pick-off. Testing of these devices is underway.

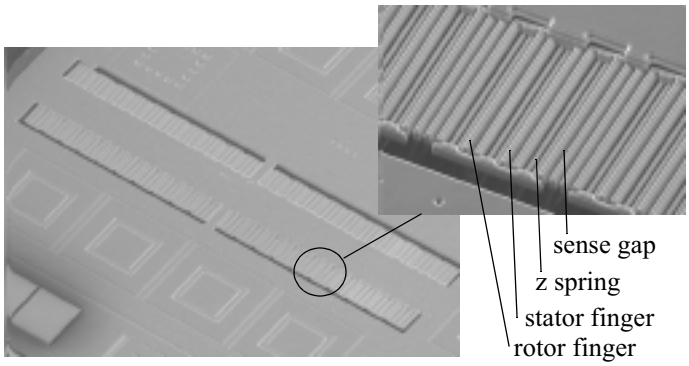


Fig. 9. CMOS-MEMS 40-accelerometer array in Jazz SiGe60 process.

CONCLUSIONS

This is the first time this mechanical noise limited behavior has been verified in a foundry CMOS-MEMS inertial sensor, opening the path to integrated accelerometers and accelerometer arrays with lower manufacturing cost compared to custom fabricated polysilicon devices. The noise performance is predictable through first-order theory, so other designs may be sized according to the desired minimum detectable signal.

ACKNOWLEDGEMENT

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