MICROMACHINED ON-CHIP INDUCTOR PERFORMANCE ANALYSIS

X. Zhu[1], R. Groves[†], S. Subbanna[†], D. Jadus[†], T. Mukherjee, G. K. Fedder
Carnegie Mellon University, Pittsburgh, PA
IBM Microelectronics, Hopewell Junction, NY[†]

ABSTRACT

Based on measurements of inductors fabricated in the IBM SiGe process with different add-on process modules, a Moments EM field simulator is used to predict inductor performance in the entire process space of different fabrication techniques, which are chosen to improve the quality factor of inductors. These fabrication techniques include different metal thickness, different wafer resistivity, a polyimide spacer and an air spacer as a thick dielectric layer(up to 200 μm). The simulated inductors range from 0.1 nH straight line designs to 5 nH spiral designs.

I. INTRODUCTION

The ever increasing competition in the wireless communication market has pushed for low-cost RF systems. Integration of on-chip inductors is one of the key efforts. This includes modeling and layout optimization[1][2][3], and process technology enhancements to improve performance[4]. Previous works related to inductor performance optimization have focused on layout/design improvements. Performance improvement through different technologies have also been explored[4][5][6][7]. Most published results demonstrate data by introducing a particular type of technique upon the existing fabrication process. However, the potential capabilities to enhance inductors' performance by these new techniques are left un-evaluated.

Relying on high frequency structure simulation tools, this paper investigates potential performance enhancements by scanning the entire process parameter space. Based on inductors fabricated in the IBM SiGe process, the process specification information and inductor layouts are imported into Sonnet®, a commercial Method of Moments EM field simulator[8]. Then the simulator was tuned to match the measurement data. By varying setups of material properties and structure geometric parameters in the simulator, the entire achievable range of process parameters are covered. The simulation results are used to project the most promising avenues for improvement, and to offer a guideline for fully and economically exploiting each fabrication technique.

II. SIMULATION SETUP

The inductors being examined include 0.1 nH, 0.3 nH, 0.6 nH straight line inductors and 1 nH and 5 nH square spiral inductors. As in Fig. 1(a), the spiral inductor consists of a top metal layer as the spiral and a 2.3 μm copper as the return path, while the straight line inductor only consists of the top metal layer, as in Fig. 1(b). In most cases, the top

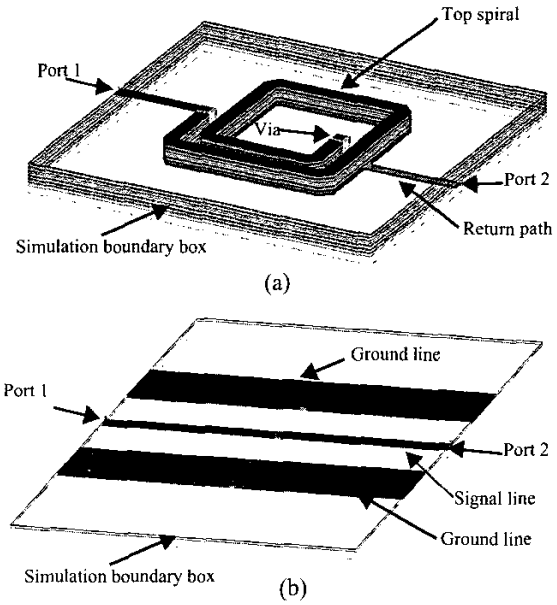


Fig. 1. Typical inductors' designs in the simulation (the substrates is not shown in the figures).
(a) a spiral inductor design.
(b) a straight line inductor design.

metal layer is made of 4 μm aluminum, except for the thick spiral layers simulation. Other shape spiral inductors, *e.g.* octagonal, are not included in this work due to the exponential increase of simulation time, and they are not expected to provide additional insight. The substrate is 700 μm thick silicon. It is separated from the inductor by the dielectric material, which is usually 12 μm thick dioxide as in the SiGe process specifications. Between the spiral and the return path is a 4 μm thick oxide layer. All the oxide layers have dielectric constance equal to 4.1.

In the device fabrication, the wafer resistivity can be varied from 0.1 Ω·cm to 1000 Ω·cm; the metal thicknesses used in spiral inductors can range from 2 μm to 34 μm; in the fron-end-of-line (FEOL), the engraved substrate can be filled with polyimide (loss tangent around 0.001) where inductors sit above; and the MEMS technology can create free standing inductors above the substrate. These fabrication variations can be represented in the simulation by changing parameters of metal and dielectric layers in the simulation setup. Nominal values of metal layer sheet resistance, wafer resistivity, dielectric constant and dielectric loss

1. Now with Akustica, Inc, Pittsburgh, PA. Email: xzhu@akustica.com

are used in the simulations. Book values are adopted for the metal conductance to calculate skin effect[9]. The simulation of thick metal layers is approximated by paralleling multiple infinitely thin conducting layers, with metal track width to metal track height aspect ratio less than 1:5, as suggested in the manual[8]. Some adjustments in the simulation are required to guarantee the simulation accuracy from 100 MHz to 50 GHz frequency range[10]. Two-port inductor layouts are imported into the simulator through GDSII format. The quality factor (Q) definition follows the single end Q configuration, with $Q = -image(Y_{11})/real(Y_{11})$[1] to be comparable with previous data. The simulation of typical spiral inductor designs, e.g. an inductor with 25 μm wide spiral and 45 μm wide pitch, matches the measurements very well, as shown in Fig. 2.

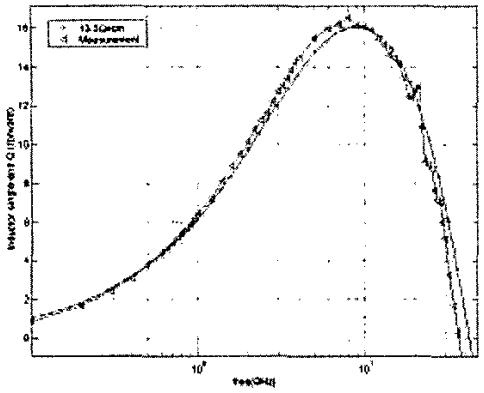
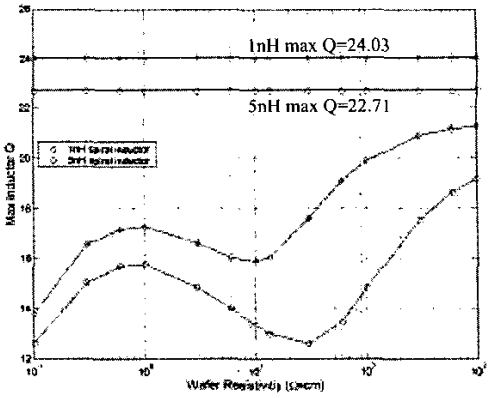


Fig. 2. A typical simulation results of a spiral inductor (1nH) with wafer resistivity of 13.5 Ω•cm *vs.* the measurement data.

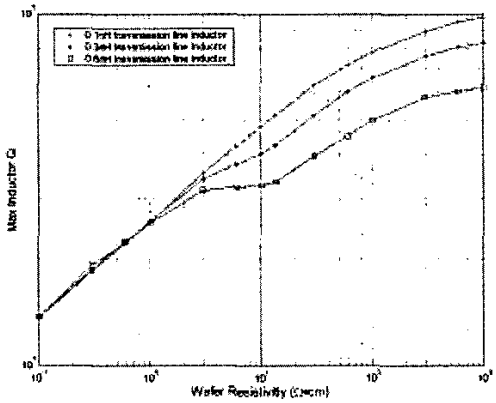
III. SIMULATION RESULTS AND DISCUSSIONS

Fig. 3 shows the simulations results of the peak inductor Q *vs.* the wafer resistivity. For a spiral inductor design, higher wafer resistivity yields higher Q. However, even 1000 Ω·cm substrates cannot yield the maximum achievable Q (defined as the inductor standing in the air). For spiral inductors on 10 Ω·cm and 1000 Ω·cm wafers, the observed Q increases by maximum 50%, and this is similar to the previous data[4]. The Q of spiral inductors has a local maximum with wafer resistivity value around 1 Ω·cm. Larger spiral inductors have longer substrate loss path, therefore its Q has larger improvement than that of small inductors, due to the increased substrate resistivity. This local maximum behavior is much less significant in straight line inductors. The EM field pattern of straight line inductors penetrates much more deeply into the substrate than that of spiral inductors, resulting in a longer loss path and larger loss.

Fig. 4 shows the measured and simulated results for Q *vs.* metal thickness. The measurement data are from octagonal designs while the simulation uses square spirals due to the memory and simulation time constraints. The Q increases almost linearly with the geometrical increase of metal thickness. This indicates that thickening metal reaches a point of



(a)



(b)

Fig. 3. Maximum inductors' Q *vs.* wafer resistivity.
(a) Spiral inductor designs.
(b) Straight line inductor designs.

diminishing returns for Q improvements. There are a couple of reasons. First the wire resistance does not decrease as the $\sim 1/t$ with the increase of metal thickness(t) due to skin effects as in Fig. 5(a). Second, with the pattern of EM field generated by the coil[11][12], the current crowding effects steer the current to flow only on one side of the metal trace. Usually, the current flows on the outer sidewalls for the outer turns, swings to the inner sidewalls as the metal trace spiraling inward, and flows on the inner sidewall for the inner turns. The switching from outer surface to inner surface is due to the pattern of the magnetic field, as in Fig. 6(a). Third, for identical layouts, the inductance drops when the thickness increases as in Fig. 5(b). This is due to reduction of the self-inductance and decrease of the effective spiral radius due to the aforementioned current crowding effects. Finally, the substrate affects the current distribution. As in Fig. 6, at high frequency due to the capacitance coupling effect, more currents flow at the bottom surface of the metal traces. The current density distribution is not uniform along and across the spiral wires, and it is concentrated on

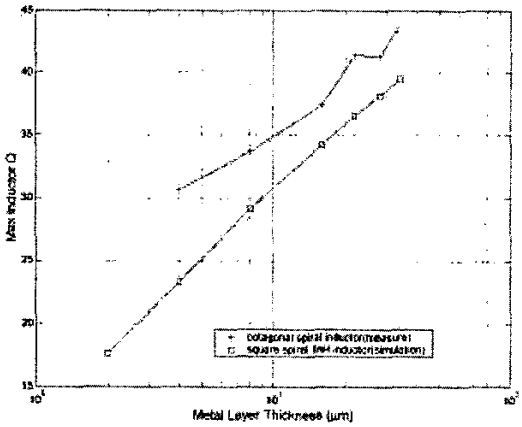


Fig. 4. Maximum spiral inductors' Q *vs.* metal thickness.

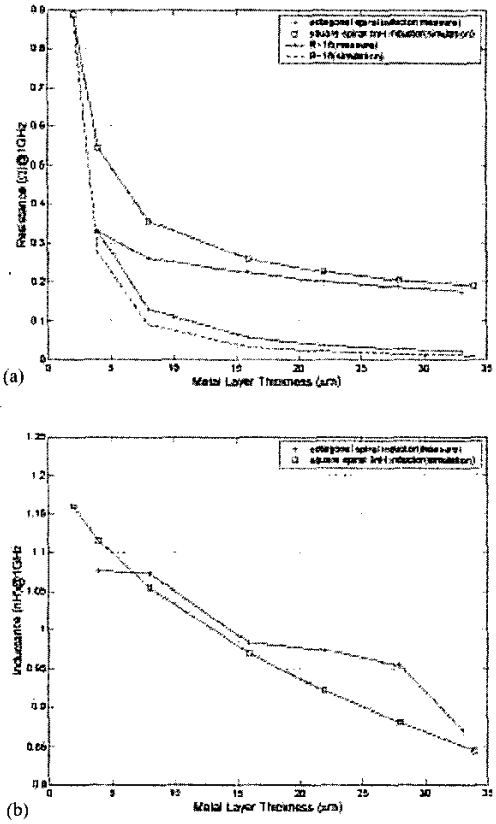


Fig. 5. Simulated and measured spiral inductor resistivity(a) & inductance(b) *vs.* metal layer thickness at 1GHz. In the simulation, the square shape is used to approximate the octagonal design.

the corners of the cross section. Of course, the fixed resistance of the return path starts to dominate total series resistance, and contributes to the slow down of Q increase as well.

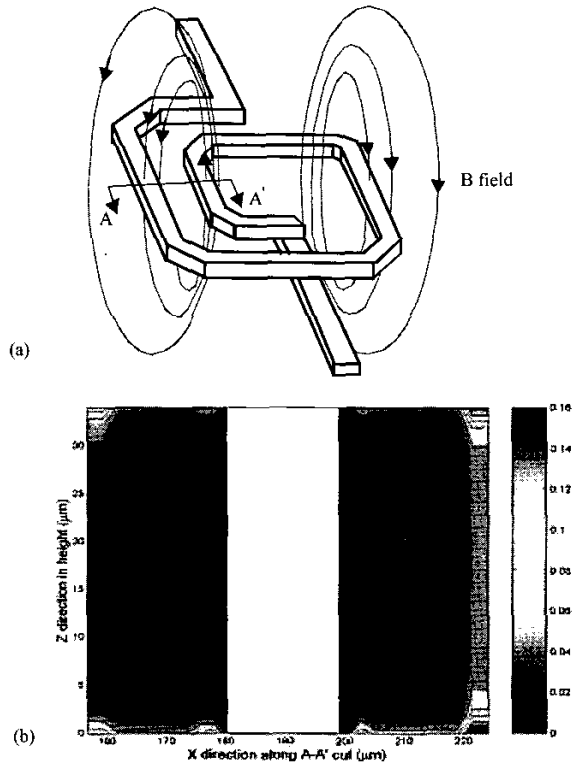


Fig. 6. The current distribution in a thick metal spiral inductor caused by current crowding effects.
(a) B field distribution induced by the current flowing in the spiral.
(b) The current density distribution at the cross section of A-A' in (a). Also noticed is that the current flow switch from left side to the right side due to the B field pattern shown in (a). The color bar illustrates the relative current flow density.

In order to reduce substrate loss induced Q degradation, several techniques are used to remove the substrate underneath the inductor. These include removal of the substrate from the backside by wet etch[5], or from the front side by vapor phase etch[6] and RIE dry etch[7]. In the simulation, an air dielectric layer is inserted above the silicon substrate to emulate this. The thickness of the layer corresponds to the air gap. The substrate thickness is subsequently reduced by this amount. The backside Si removal is treated as an infinite air gap. It is clear from Fig. 7 that substrate removal effectively improves the Q, and the Q value reaches the maximum at the 100 μm air gap for a 400 μm inductor O.D. with inductance value of 1 nH and 5 nH. This indicates that the EM fields are concentrated in a 100 μm range below spiral inductors. Instead of performance improvement, extra etch into the substrate will reduce the mechanical strength of the chip. It is obvious that larger O.D. inductors benefit more from substrate removal. With an inductance value of 5 nH, the Q value increase is by 100%. This matches the previous data mentioned above[7].

A thick dielectric layer can be inserted above the Si sub-

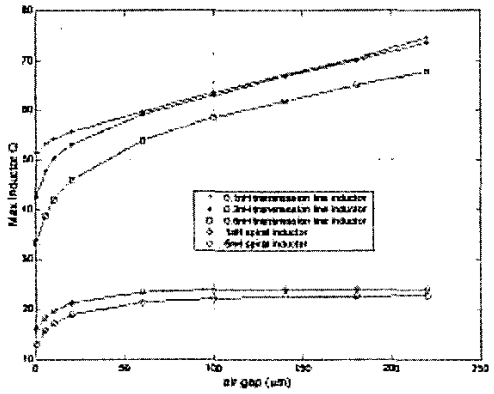


Fig. 7. Maximum inductors' Q vs. air gap depth.

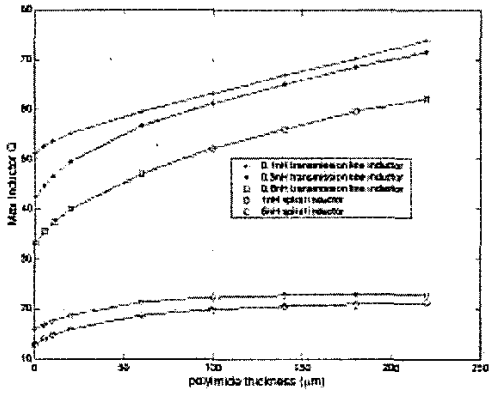


Fig. 8. Maximum inductors' Q vs. thickness of polyimide.

strate with dielectric constant 3.4 and loss tangent 0.001 (Dupont PI5878) to act as a spacer[13]. This material functions the same as the air gap dielectric. It is expected that the Q values as a function of polyimide thickness should behave similar to that in Fig. 7. However, the Q will reach a maximum later than the air dielectric, because the air has the lowest dielectric constant. This is verified in Fig. 8. Slight reduction of maximum Q value in this case is due to larger capacitive coupling from one portion of the spiral to another. Again, the Q improvement matches the previous data[13].

It is noticed that Q curves of straight line designs have not become flat with 200 μm thick dielectric, comparing with that of spiral designs. The reason is that the EM field generated by the straight line inductors penetrates much more deeply into the substrate than that for spiral designs, therefore a larger spacing between the inductor and the substrate is required.

Increasing the oxide thickness between inductors and the substrate reduces substrate loss in a similar fashion as inserting a layer of air or polyimide. Due to stress issues in the wafer, the maximum thickness is limited to around 10~20 μm, and it is far below the separation requirement for the maximum Q.

IV. CONCLUSION

We demonstrated the capability to accurately simulate spiral and straight line inductors by the Method of Moments tool. Different fabrication techniques can be presented in the software by changing the parameter setups. The substrate coupling loss is a major loss mechanism besides wire resistance, especially in the straight line case. In addition to increasing metal thickness, any added fabrications steps in the FEOL or BEOL, which can locally increase the space between the inductors and substrates, will dramatically improve inductors' performance. For most spiral designs, around 100 μm is sufficient, however, more spacing are required for straight line designs. Thus, the combination of these process modules will achieve the desired requirements much more efficiently.

REFERENCE

[1] K.B. Abshy, et al., "High Q inductors for wireless applications in a complementary silicon bipolar process," IEEE J. Solid State Circuits, vol. 31, pp. 4-9, Jan 1996.

[2] C.P. Yue, et al., "Physical model for planar spiral inductors on silicon," Proceedings IEDM 1996, pp. 155-158.

[3] J. R. Long, et al., "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," IEEE JSSCC, vol. 32, no. 3, March 1997.

[4] J. N. Burghartz, et al., "Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates," IEEE Trans. Microwave Theory Tech., vol. 45 no. 10, pp. 1961-1968, Oct 1997.

[5] K. T. Ng, et al., "Characterization of a bulk-micromachined post-process module for silicon RF Technology," IEEE Tropical Meeting on Si Monolithic Integrated Circuits in RF systems, pp. 99-102, Apr. 2000.

[6] J. Y. C. Chang, et al., "Large suspended inductors on silicon and their use in a 2 μm CMOS RF amplifier," IEEE Electron Device Letters, Vol. 14, No. 5, May 1993, pp.246-248.

[7] H. Lakdawala, et al., "Micromachined high Q inductors in 0.18um Cu interconnect low-K CMOS," CICC2001, pp.1549-51, May 2001.

[8] Sonnet® On-line User's Manual, release 6.0.

[9] D. M. Pozar, "Microwave Engineering," 2nd Edition, Jon Wiley & Sons, Inc.

[10]Technical notes from Sonnet Inc.

[11]Huan-Shang Tsai, et al., "Investigation of current crowding effect on spiral inductors," IEEE Trans. Microwave Theory Tech., vol. 49 no. 1, pp. 31-38, 2001.

[12]William B. Kuhn, et al., "Analysis of current crowding effects in multiturn spiral inductors," IEEE Transactions on Microwave Theory and Techniques, vol. 49 issue 1, pp. 31-38, Jan.2001.

[13]D. C. Laney, et al., "Low-loss microwave transmission lines and inductors implemented in a Si/SiGe HBT process," IEEE BCTM 5.4, pp.101-104, 1998.