STRUCTURED DESIGN OF INTEGRATED MEMS

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ABSTRACT

MEMS design methodologies in wide use today do not support hierarchical representations suitable for verification-based iterative design. Adoption of a structured design methodology which borrows hierarchy from the electronics design paradigm enables rapid design verification of complex electronic and micromechanical trade-offs inherent in integrated MEMS. A hierarchical MEMS circuit representation is analogous to and compatible with transistor-level circuits for electronics. Design of a capacitive lateral accelerometer illustrates the structured design flow from a system description, to circuit representation, layout and fabrication. Tools for layout synthesis, layout extraction, and verification specifically tailored for MEMS are an integral part of the design flow. The accelerometer is fabricated in a low-cost CMOS micromachining process that is especially suited to rapid prototyping of integrated MEMS.

INTRODUCTION

Much excitement in MEMS arises from the variety of sensing and actuation capabilities that can be embedded into information systems. Numerous applications are being researched, however the realization of MEMS to exacting commercial specifications remains a tedious multi-disciplinary task. Practical methodologies to design and fabricate MEMS application-specific integrated circuits (ASICS) at a comparable cost to digital ASICS will represent an enormous advance in commercializing of MEMS in the various application areas in which MEMS is ideally suited.

Bringing MEMS to market at very low cost has so far only been justified in markets requiring extremely large quantities of parts, on the order of tens of millions or higher. These markets include automotive accelerometers and gyroscopes, pressure sensors, ink-jet print heads, optical and RF switching networks, data storage, and disposable chemical analysis systems.

Smaller markets for MEMS are currently served by using a commercially available product, or designing custom systems at great time and expense. The development and maintenance of customized processes must be amortized over relatively few parts. These manufacturing constraints are similar in analog electronics, where custom processes can only be justified in markets like computer peripherals.

Design of commercial MEMS has remained an art form that requires a large team of skilled engineers spanning several disciplines, with the concomitant overhead in management costs. Time to product yield is relatively slow because of the need for simultaneous design iterations in process, devices, and system. Many of these iterations occur with fabrication in the loop.

Several items are required for commercialization of integrated MEMS ASICs:

- inexpensive access to microstructural processes, preferably integrated with electronics;
- computer-aided design tools for partitioning design to handle complexity;
- materials and process characterization encoded in design and technology files;
- improved testing methods and equipment;
- improved packaging methods and equipment.

All of these topics present very hard problems, for which general solutions are elusive. The MEMS research group at Carnegie Mellon is addressing the first two issues listed above by developing a hierarchical design methodology, computer-aided design tools to support this methodology, and low-cost CMOS-based micromachining technology.

MEMS DESIGN METHODOLOGIES

A: Unstructured MEMS Design Flow

The design flow in Fig. 1 is commonly followed for MEMS that have an interplay between electronics and micromechanical components. The top-level system specification is usually in the form of a datasheet. Design concepts in all but very simple components are then embodied in an abstract system description. For purposes of discussion, the system description refers to a high level of abstraction, not to the implementation which may be in the form of a circuit (*i.e.,* a network of lumped-parameter ele-

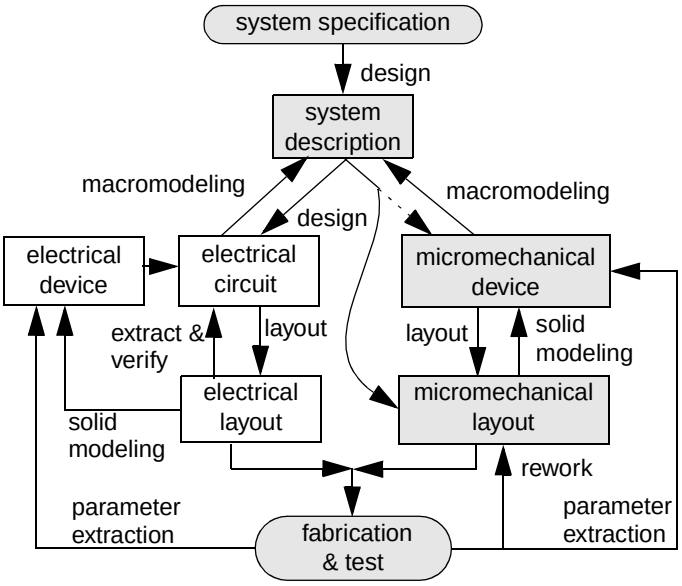

Fig. 1. Commonly used MEMS design flow. The portion of the flow that is unique to micromechanics is shaded.

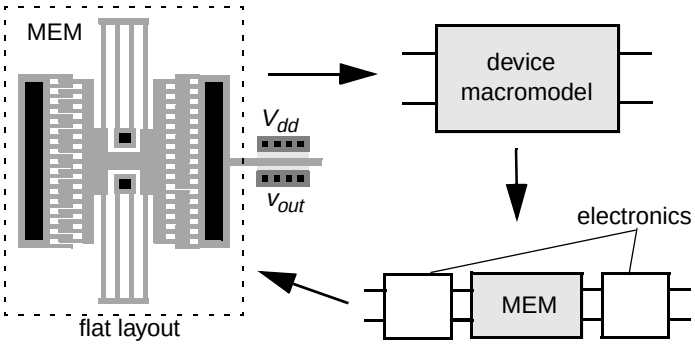

Fig. 2. Illustration of lack of hierarchy and of one-way design flow in unstructured MEM design.

ments), a signal-flow block diagram, or a bond graph (*i.e.,* a directed graph explicitly showing power flow). Aside from the system description in the design flow of Fig. 1, the MEM design and electronics design are decoupled, due to the lack of computer-aided design (CAD) tools that mix electronic and MEM representations.

Highly developed tools for electronic design exist to ensure first-pass success in silicon by having a well defined "top-down" design path and "bottom-up" verification path. The tool suite includes circuit representation, extraction from layout of devices and parasitics, and verification of interconnect between layout and schematic. Reduced-order modeling, or macromodeling, of analog circuits is primarily a manual procedure, and remains a bottleneck in large system design. Device modeling is out of the design loop unless a new device or underlying process is developed for which models do not exist. The term "device" is meant to signify a component represented by a non-hierarchical, or flat, macromodel. Therefore, a device may be an accelerometer system or a simple beam, as long as the underlying macromodel is indivisible.

A comprehensive suite of similar design tools for micromechanics is not commercially available, however, a handful of CAD companies that now cater to the MEMS market are starting to address this issue.

Current MEM design manipulates two primary representations, the physical geometry and the device macromodel, as shown by the one-way flow illustrated in Fig. 2. Design usually takes a direct path to layout (or 3D solid modeling) from the system description, since there has been no alternative. Several companies now provide tools to automate the construction of solid models from a combination of layout and process description, and then couple this geometry into direct numerical simulation (*e.g.,* finite-element analysis or boundary-element analysis). New macromodels must be created for any change in topology, and for any change in geometric or process parameters in the case of non-parametric modeling approaches. A good overview of macromodeling and associated simulation requirements is presented by Senturia [1]. Automation of macromodeling as a link to the system level is being researched by several groups, and is beginning to show up in commercial tools [2][3]. However, since the device modeling is in the primary design loop, iterative MEM design remains slow and tedious with current tools.

B: Structured MEMS Design Flow

Complexity in electronics is handled through a hierarchy of devices, components and blocks, all of which can share the same circuit (or layout) representation. Electronic design automation tools support this design hierarchy. Transistor circuits can be grouped together to form functional components, such as operational amplifiers. Components can be grouped to form functional blocks, and so on. Because of the uniform nature of the representation, the designer can move between levels of abstraction with agility, and the iterative design process is rapid. Hierarchical cell design is standard practice in analog design, however hierarchical modeling concepts are still in their infancy. Both are ultimately required for design of very complex systems.

In a practical design sense, even simple MEMS have greater complexity than many electronics circuits, because of the mixed-domain nature. The existence of hierarchical levels of abstraction for MEMS is essential in dealing with complexity of all but very small systems, or systems with multiple copies of one fixed MEM device (such as the Texas Instruments Digital Micromirror Display [4]).

A hierarchical cell design approach for suspended MEMS has been developed over the past four years at Carnegie Mellon University [5][6] as well as in work by Pister *et. al.* at U. C. Berkeley [7] and Antonsson at Caltech [8]. Suspended MEMS span a wide range of applications including pressure sensors, accelerometers, gyroscopes, resonators, relays, RF filters, variable capacitors, micromirrors, microactuators for data storage, and acoustic and ultrasonic transducers. An example of the hierarchical representation of a resonator filter, designed by Nguyen *et. al.* at U. Michigan [9], is shown in Fig. 3. The partitioning of the filter into three separate resonators, then into electrostatic comb-finger actuators, plate masses, flexural beams and anchors is an accepted design practice today, but it is only common in terms of layout representation. MEM layout cell generators for hierarchical construction of surface-micromachined MEMS include the CaMEL library developed at MCNC [10], and those in CAD frameworks by Mentor Graphics/MEMSCap [11] and Tanner Research [12].

In order to fully leverage the hierarchical decomposition in design, a partitioning of behavioral models corresponding to the geometric partitioning must take place. To this end, similar hierarchical circuit representations of suspended MEMS are being developed by the present author's students (Nodal Design of Actuators and Sensors - NODAS) [13][14][15], by Pister *et. al.* at the Berkeley Sensor and Actuator Center (the tool is called Sugar) [16][17], and by Lorenz *et. al.* at Bosch, GmbH [18][19]. Behavioral macromodels may be defined at any level of the hierarchy. At the lowest level of the hierarchy are plate masses, beam springs, electrostatic air-gaps and anchors, which are at a similar level to resistors, capacitors and inductors in electronic design. Systems lying in a very large and useful design space can be evaluated all the way to the top of the hierarchy if this finite set of low-level elements are pre-defined with sufficiently general geometric parameters and material properties. The underlying macromodels can be formed *ad hoc* without loss of generality. Basic linear and nonlinear nodal models for beams and plates are found in mechanics texts [20]. Electrostatic gap models require careful attention to energy considerations.

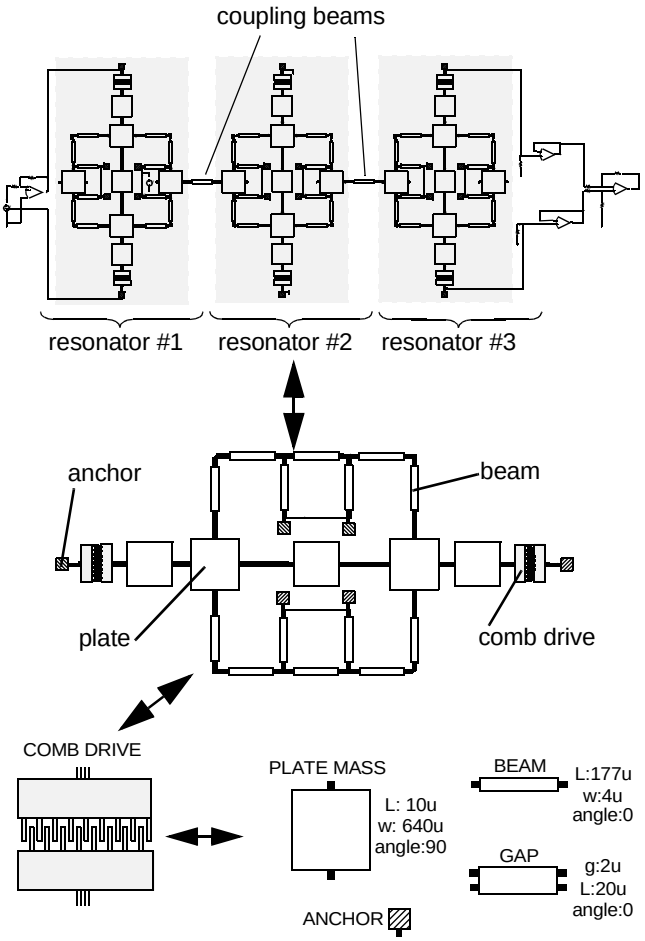

Fig. 3. MEMS cell hierarchy for a high-Q resonator filter analogous to the electronic design hierarchy. The filter is partitioned into three separate resonators, the resonator is partitioned into sub-components, and the comb drive may be further partitioned into plates, beams and gaps.

The example circuit representation of the cantilever beam shown in Fig. 4 is formed by connecting an anchor component to a two-dimensional beam component. In-plane displacements *(x, y, θ)* are across variables, and forces and torques (F_x, F_y, M_θ) acting on the element are through variables. Sign convention of the *x* and *y* across variables is positive along the positive-axis direction and θ is positive in a counterclockwise rotation (right-hand rule) around the *z* axis. Positive-valued through variables going *into* a node are interpreted as providing force in the positive-axis direction or providing torque in a counterclockwise rotation around the *z* axis. In contrast to electrical simulation, MEMS simulation requires inclusion of geometric and layout position parameters (X_o, Y_o, and Θ_o) since the micromechanical behavior is directly linked to shape of components, and, in the case of inertial sensors, is linked to absolute layout position. Automated tool is available in NODAS to generate layout position parameters for the designer [15].

In principle, the MEMS circuit representation can be implemented in electrical circuit simulators such as SPICE, however forming the equivalent electrical models is difficult and translation between voltages and currents to other physical variables is cumbersome. General behavioral circuit simulators allow interaction between components from multiple energy domains in terms of specialized across and through variables defined for each domain. Component models are expressed in an analog hardware description language (AHDL). Commercial simulators include Saber with MAST AHDL [21][22], Spectre with Verilog-A AHDL [23], and ELDO with HDL-A [24]. An emerging IEEE standard 1076.1 called Very High Speed Integrated Circuit (VHSIC) HDL-Analog Mixed Signal (VHDL-AMS) is expected to provide interoperability between vendors [25].

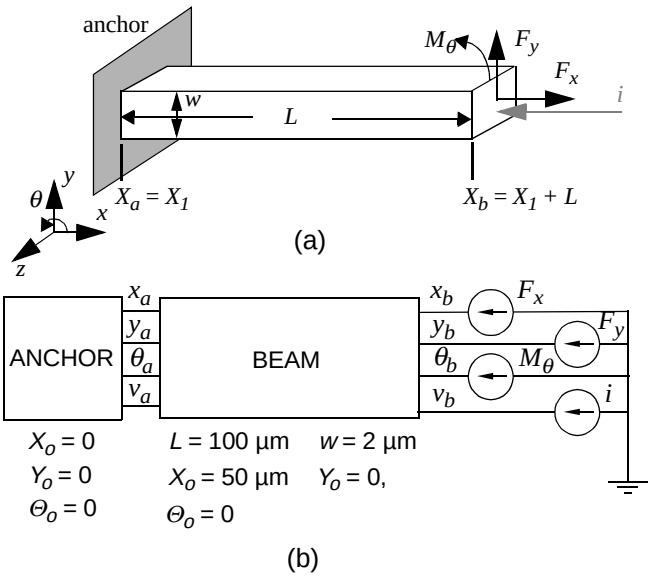

Fig. 4. Circuit representation of a simple cantilever beam with in-plane layout position *(X, Y, Θ)* and displacements *(x, y, θ)*. (a) Physical view showing applied forces, moment and current. (b) Schematic view showing corresponding across and through variables and illustrating sign convention.

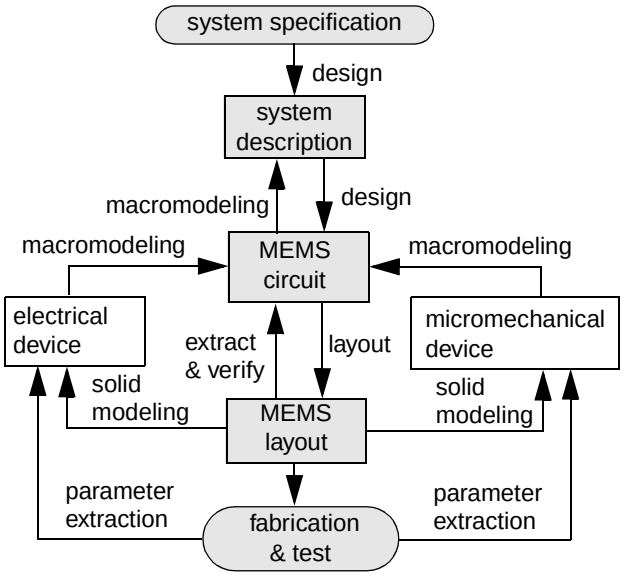

Fig. 5. Structured MEMS design flow. The shaded blocks indicate the primary design path.

The structured design methodology shown in Fig. 5 combines the design of micromechanics and electronics into a single flow in which the MEMS circuit representation plays a central

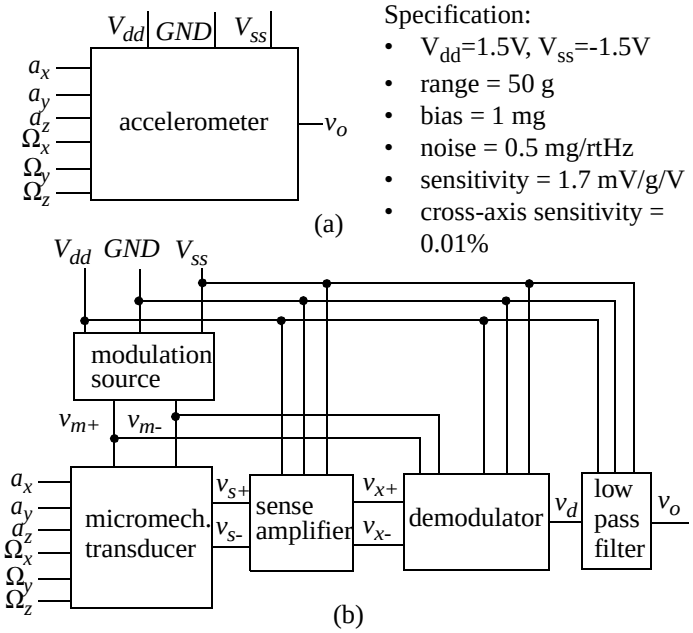

Fig. 6. (a) Accelerometer specification (*i.e.*, datasheet). (b) System description of the accelerometer.

role. The primary advantages are the reusability of the parametric circuit models and the ability to iterate relatively quickly and precisely between system, circuit and layout representations. As with electronic design, modeling intervention during design iterations is required when a designer insists on component topologies that cannot be constructed from parts in the library. Parameter extraction from experimental test structures can provide the appropriate geometric and materials property values for use in the device macromodels.

Partitioning of function as one descends the hierarchy may exclude "far-field" effects. This is especially true of the beam/plate/gap level where electrostatic fields or fluidic interactions from components other than nearest neighbors may not be included. Fortunately, for these cases, the structured design methodology is compatible with the customized flat macromodeling depicted in Fig. 2. High-precision models can be inserted as desired into the circuit representation at any level. This activity may best be done after the overall system design and micromechanical topology is finalized.

AN ACCELEROMETER DESIGN EXAMPLE

A: System Description

The structured design methodology is exemplified in the design of a lateral capacitive accelerometer. Specification from the top down is essential in identifying and understanding the numerous design trade-offs. The design process starts with specification at the system level, followed by partitioning into subsystems, as shown in Fig. 6. A design decision is made to use balanced modulation voltage sources, v_{m+} and v_{m-}, to drive a micromechanical capacitive bridge. The bridge sense outputs, v_{s+} and v_{s-}, are amplified and demodulated to generate the accelerometer output, v_o. The micromechanical transducer is affected by external acceleration signals (a_x, a_y, a_z) and by rotational rate signals (Ω_x, Ω_y, Ω_z) which generate centripetal acceleration.

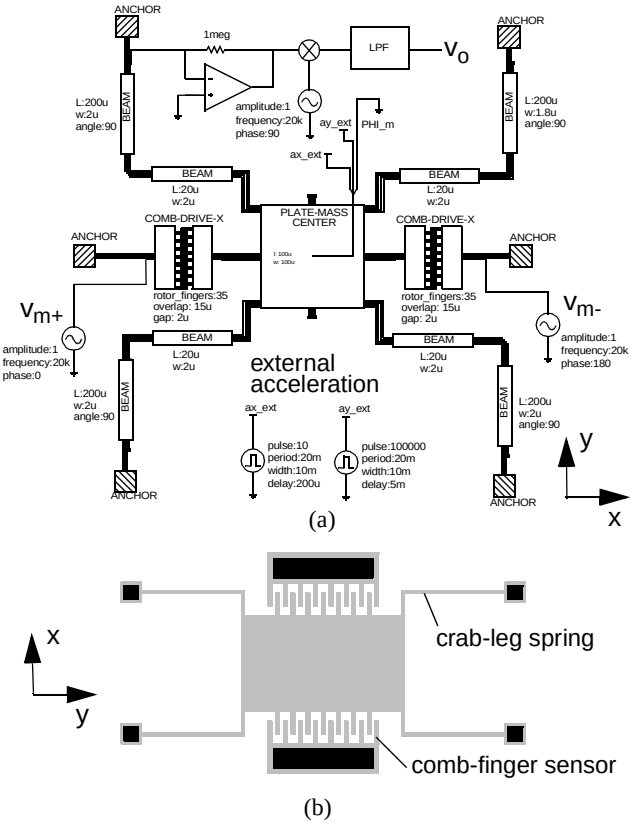

Fig. 7. A crab-leg lateral capacitive accelerometer design. (a) Two-dimensional MEMS circuit view (rotated by 90°) with electronics represented as functional blocks. (b) Simplified layout of the transducer.

B: MEMS Circuit Representation

Although signal-flow representation may be used, a circuit representation maintains the cell hierarchy to lower levels. The micromechanical transducer design in Fig. 7 is represented using the two-dimensional NODAS component library, and implemented using Saber. Placement of the schematic symbols is arbitrary, however the components are sensibly placed to reflect the correspondence with layout. External accelerations are applied as acceleration sources, while the external z-axis rotation is set to zero. Transistor-level circuits for the electrical blocks are not included in the circuit to speed up simulation. Evaluation of different topologies (*e.g.*, using different flexures) or sizing of components is trivial due to the low-level representation.

The simulation of the accelerometer in Fig. 8 illustrates the utility of the MEMS circuit representation. Manufacturing variation on cross-axis sensitivity is explored by setting the width of the upper right crab-leg beam to be 10% smaller than the other flexural beams. The on-axis acceleration, a_x, is set to a 10 ms 1 g pulse. After 10 ms, the plate responds to an overlapping 10,000 g pulse in cross-axis acceleration, a_y. The electrical effects of the cross-axis displacement of the plate are cancelled to first order by the balanced capacitive bridge formed from the comb-finger sensors located on opposite sides of the plate. However, the imbalance in the flexure causes the plate to move along the x-axis in response to the cross-axis acceleration. This displacement propagates through the sense amplifier, demodulator, and appears as an undesirable cross-axis coupling at the output

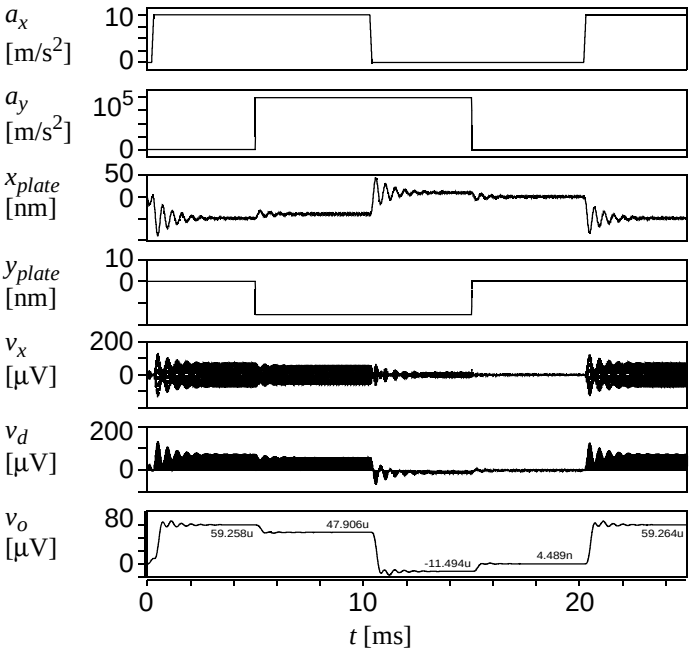

Fig. 8. Transient simulation of the crab-leg accelerometer circuit, where a_x is the on-axis acceleration, a_y is the cross-axis acceleration, x_{plate} and y_{plate} are the proof-mass displacements, v_x is the modulated output voltage, v_d is the demodulated voltage, and v_o is the filtered output.

of the filter. Most circuit simulators have Monte Carlo simulation capability so that a scatter plot of sensitivities from random manufacturing variations can be automatically generated.

C: Layout Synthesis

Layout is a time consuming task which may at least be partly automated. Generation of layout cells from geometric parameters is supported by many CAD vendors, as noted earlier. Optimization-based synthesis tools generate custom layout to meet all performance specifications while optimizing some combination of specifications. Examples of this approach include shape synthesis of comb drives [26], compliant mechanisms[27], springs [28], and bulk-micromachined structures [29].

Mukherjee *et. al.* [30][31] have developed optimization-based synthesis modules for electrostatic folded-flexure resonators, which have multiple nonlinear design constraints. Given the fixed topology, layout is generated by sizing the constitutive beams, plates and gaps. A gridded-multistart approach overcomes local minima in the nonlinear optimization function. An extension of this work is in synthesis of lateral capacitive accelerometers, reported in depth elsewhere in this proceedings [32]. The layout in Fig. 9 is of a synthesized accelerometer meeting the system specifications and with minimized thermomechanical (Brownian) noise. Process and design-rule constraints are for a CMOS micromachining process [33] described in the next section. The component is of maximum size and the capacitive sense fingers are sized to just meet the sensitivity specification. Exploration of the design space quantitatively identifies performance trade-offs such as between sensitivity and noise performance. For an optimized fixed-size lateral capacitive accelerometer, a reduction in noise floor necessitates a reduction in the transducer sensitivity.

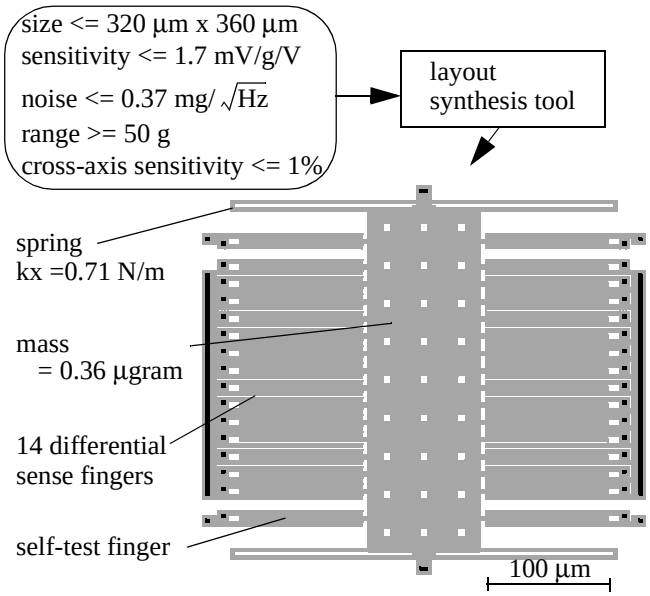

Fig. 9. Synthesized layout of a lateral capacitive accelerometer, derived from performance specifications and optimized to minimize noise (0.13 mg/rtHz).

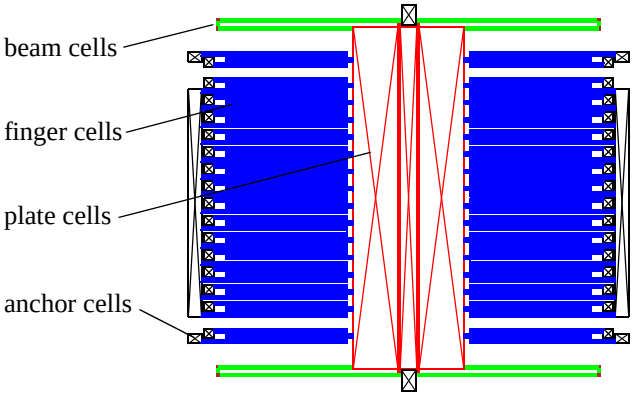

Fig. 10. Extracted view of the synthesized accelerometer illustrating the recognition of beam-spring, plate-mass, cantilevered-finger, and anchor cells.

D: Layout Extraction

Extraction translates layout into a corresponding circuit representation (*i.e.*, a netlist). It serves two purposes. 1) Layout correctness can be verified against an existing circuit representation. 2) An extracted netlist can be evaluated to verify functionality of the system. A particularly important example is the extraction of sidewall and parallel-plate capacitances on the sensitive high-impedance nodes corresponding to the micromechanical sense capacitors. In order to back-annotate circuits with these extracted parameters, the extraction tool must be able to recognize functional elements from the layout.

General feature recognition algorithms for surface micromachined MEMS have been developed by Baidya *et. al.* [34]. The extracted version of the synthesized accelerometer layout is given in Fig. 10. The input layout in CIF format is partitioned into a unique canonical representation, where each rectangle (or cell) has only one neighbor on each side. Plate cells are combined using a modification of corner stitching [35]. Fingers are recognized as cells with a connection on only one side (*i.e.*, a cantilever) and beams as cells with connections on opposing

sides. The resulting netlist directly corresponds to the lowest-level MEMS circuit representation.

CMOS MICROMACHINED FABRICATION

Integrated MEMS have been fabricated using custom processes with microstructures made of aluminum [4], polysilicon, and single-crystal silicon. A good review of recent activities in monolithic integration motivated by high-performance inertial sensors is given by Yazdi *et.al.* [36]. Most of these processes require dedicated facilities to handle the special MEMS process steps.

Formation of microstructures out of CMOS interconnect layers was first explored ten years ago [38] and is currently being researched in several groups including ETH [39], NIST [40], and U. C. Berkeley [41]. Structures in these processes are made by stacking vias in the CMOS process and etching away the metal, thereby exposing silicon. If the CMOS process allows variable sized vias and is not a tungsten plug process, then arbitrary shaped microstructures can be defined. The microstructures are undercut in a timed isotropic wet or dry silicon etch.

A high-aspect-ratio CMOS micromachining process has been developed at Carnegie Mellon that decouples the micromachining steps from the CMOS process flow [42][43]. The resulting structures allow beam and gap widths down to 1.2 µm, and aspect ratios greater than 4:1. Layout follows design rules of conventional CMOS processes. The process is being used to fabricate integrated inertial sensors [44][45] and probe-head actuators for on-chip mass data storage [33].

Fabrication steps for a simple cantilever beam are illustrated in Fig. 11. Prototype structures begin with the Hewlett-Packard 0.5 µm three-metal n-well CMOS process available through the MOS Implementation Service (MOSIS) [46]. Anisotropic reactive-ion etching (RIE) of the dielectric layers precisely defines the structural sidewalls. The top metal interconnection layer acts as an etch-resistant mask for the microstructure definition. The process recipe is 125 mTorr pressure, 0.55 W/cm^2 power, 22.5 sccm CHF_3 and 16 sccm O_2 flow. This etch recipe strikes a delicate balance between manufacturable etch rate, excessive aluminum mask erosion and via failure from ion milling, and unwanted polymerization [47]. It takes about 2 hrs to etch through all the dielectric layers at the etch rate of 425 $\mathring{A}$/min. Next, a nearly isotropic SF_6/O_2 etch undercuts the silicon substrate and releases the structure. Fourteen different composite structures can be made by using different combinations of the embedded metal layers and polysilicon. A released composite beam with three metal conductors and polysilicon is shown in Fig. 12.

Advantages of CMOS micromachining include low-cost fabrication of integrated MEMS, an ability to place multiple isolated conductors within suspended structures, and an ability to make extremely sensitive capacitive detectors. The latter is enabled by placing transistor circuits next to the silicon etch pit, which results in extremely low parasitic capacitance to substrate on high-impedance sense nodes. Experiments have shown absolutely no degradation in transistor threshold voltage or leakage current is caused by the micromachining steps. Materials characterization of 3-metal test structures provides a nominal Young's modulus of 60 GPa, compressive residual stress of 69 MPa, and

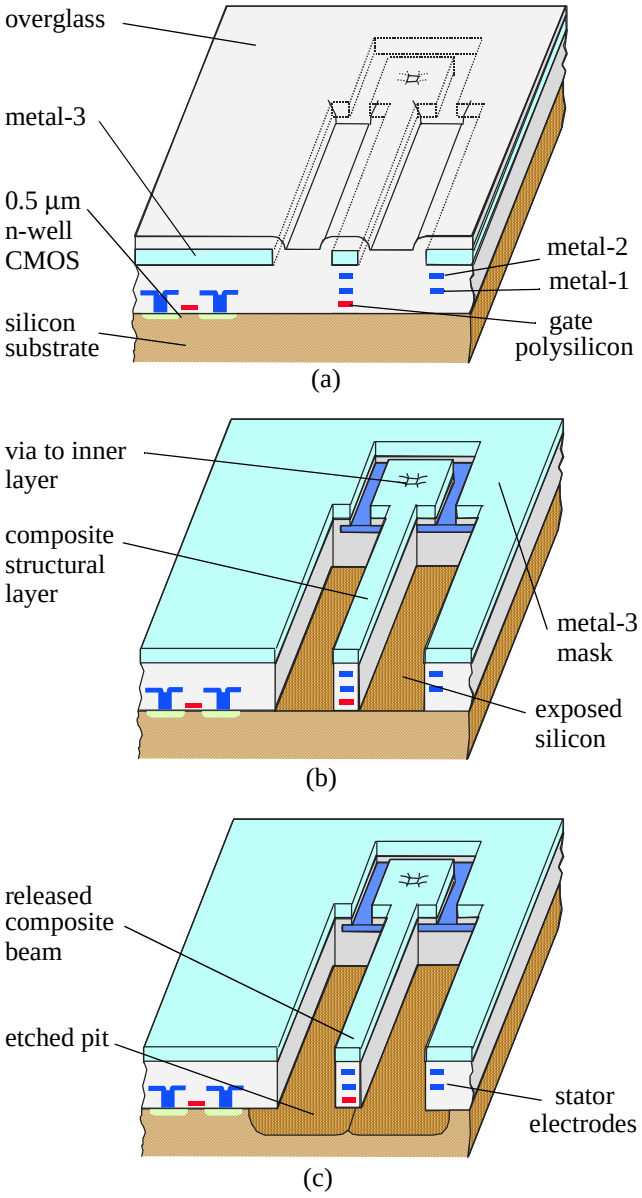

Fig. 11. The high-aspect-ratio CMOS micromachining process flow. (a) After CMOS processing. (b) After dielectric reactive-ion etch for definition of structural sidewalls. (c) After isotropic silicon etch for structural release.

vertical residual stress gradients resulting in radius of curvature of 1.8 mm [48].

The CMOS-micromachined accelerometer shown in Fig. 13 is the first lateral capacitive inertial sensor to be built directly in CMOS. Experimentally measured noise is 0.5 mg/$\sqrt{\text{Hz}}$ and sensitivity is 1.2 mV/g/V. Details of the design are reported elsewhere in this proceedings [45]. A fully differential capacitive bridge is implemented using multiple wiring in the proof mass. A major challenge is overcoming effects of vertical curl due to residual stress gradients in the composite microstructure. The accelerometer design uses curl matching of stator and proof-mass fingers to solve the problem to first order. Once material properties are extracted from test structures, vertical curl of the composite structure can be predicted prior to fabrication, as evidenced by the results in Fig. 14 showing finite-element analysis using MEMCAD [49].

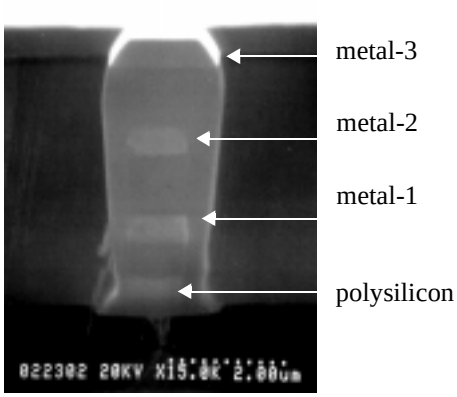

Fig. 12. Cross section of a composite CMOS microstructural beam with three CMOS metallization layers and gate polysilicon embedded.

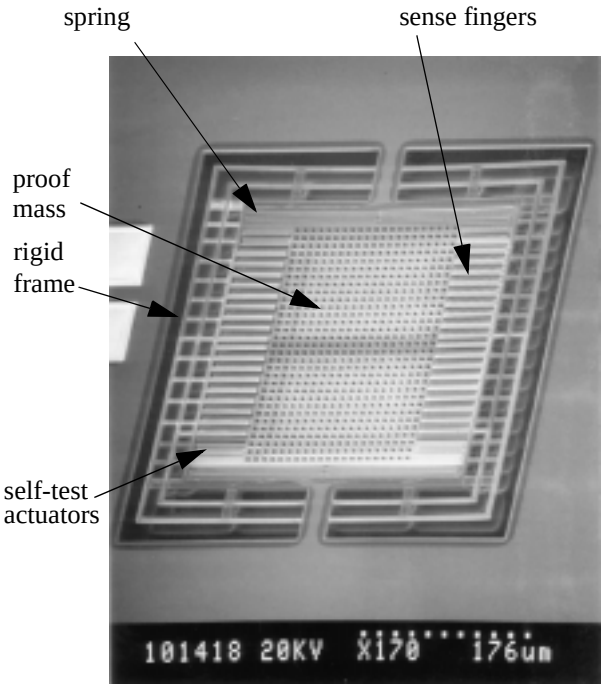

Fig. 13. SEM of the CMOS-micromachined accelerometer described in [45].

CONCLUSIONS

A structured design methodology for MEMS in which cell hierarchy is propagated down to the lowest level of beams, plates and gaps is an efficient way to design integrated and complex MEMS. The methodology will become more widely used once robust hierarchical circuit representations for MEMS and such supporting tools as layout synthesis and extraction are made commercially available. The CMOS micromachined accelerometer design example illustrates that rapid MEMS design is possible, but it also identifies issues such as residual stress that are required in hierarchical macromodels before they are accepted by MEMS designers.

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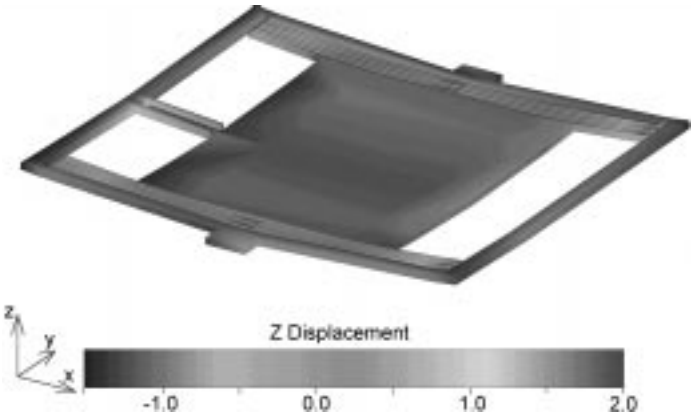

Fig. 14. Finite-element analysis of vertical stress gradient in the composite CMOS microaccelerometer.

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