LAMINATED HIGH-ASPECT-RATIO MICROSTRUCTURES IN A CONVENTIONAL CMOS PROCESS

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ABSTRACT

Electrostatically actuated microstructures with high-aspect-ratio laminated-beam suspensions have been fabricated using conventional CMOS processing followed by a sequence of maskless dry-etching steps. Laminated structures are etched out of the CMOS silicon oxide, silicon nitride, and aluminum layers. The key to the process is use of the CMOS metallization as an etch-resistant mask to define the microstructures. A minimum beam width and gap of 1.2 μm and maximum beam thickness of 4.8 μm are fabricated in a 0.8 μm 3-metal CMOS process available through MOSIS. Structural features will scale in size as the CMOS technology improves. An effective Young's modulus of 63 GPa is extracted from resonant frequency measurements. Cantilevered structures slightly curl up with a radius of curvature of about 4.2 mm. Multi-conductor electrostatic micromechanisms, such as self-actuating springs and nested comb-drive lateral resonators, are successfully produced. Self-actuating springs are self-aligned multi-conductor electrostatic microactuators that are insensitive to curl. The resonance amplitude is 1 μm for an 107 μm-wide x 109 μm-long spring with an applied 11 V ac signal. Finite-element simulation using the extracted value for Young's modulus predicts the resonant frequency of the springs to within 6% of the measured values.

INTRODUCTION

Microstructures integrated with CMOS are commonly made from combinations of aluminum, silicon oxide, and silicon nitride thin films by undercutting the silicon substrate, which acts as the sacrificial material [1]. The metallization and dielectric layers, normally used for electrical interconnect, now serve a dual function as structural layers. There are many advantages to leveraging conventional CMOS processing for MEMS. Fabrication is fast, reliable, repeatable, economical, and available through external foundries. Integrated MEMS capabilities, built into the process, will improve with the scaling of CMOS technology.

Previously, conventional CMOS processing has been used to make thermal flow sensors [2], accelerometers [3],

thermally isolated transistors [4], infrared sensors [5], and 3D assembled structures [6]. Structures have been released by dry etching, wet etching, and electrochemical wet etching of the bulk silicon. The previous work has resulted in static structures for thermal isolation and movable beams and plates having vertical actuation. Formation of aluminum and oxide structures has relied on a stacked via cut in the CMOS process, which is not optimized for micromechanical sidewalls. Etching steps in the foundry process are tailored for planarized interconnect. The uncovered stacked vias violate the CMOS design rules, produce very non-planar topography, and result in the formation of metal and dielectric sidewall stringers. These stringers adversely affect the effective beam width by 2 μm or more and can produce a large strain gradient in the structure. Very narrow lateral gaps cannot be fabricated because of the topographical constraints. In past processes where we had used stacked vias, the structure spacing was limited to about 10 μm for acceptable yield. Structural yield was highly dependent on the CMOS vendor and varied from run to run.

In contrast to structural definition within the CMOS process, structural definition performed after completion of the CMOS process can be optimized for etching of high-aspect-ratio beam suspensions and narrow-gap electrostatic actuators. We use the top metal interconnect layer as an etch-resistant mask for the microstructure definition. A series of dry etches creates the microstructures and releases them from the substrate. In this paper, the fabrication results are presented first, followed by a discussion of design issues, and characterization of some example devices that take advantage of the unique aspects of this process.

FABRICATION

Structures are made using the Hewlett-Packard 0.8 μm 3-metal CMOS process available through MOSIS. The process flow in Fig. 1 shows development of a high-aspect-ratio beam in cross-section [7]. The dice which come back from MOSIS have CMOS circuits covered by the metal-3 and oxide layers as shown in (a). The top metal layer is used as the etch-resistant mask during the
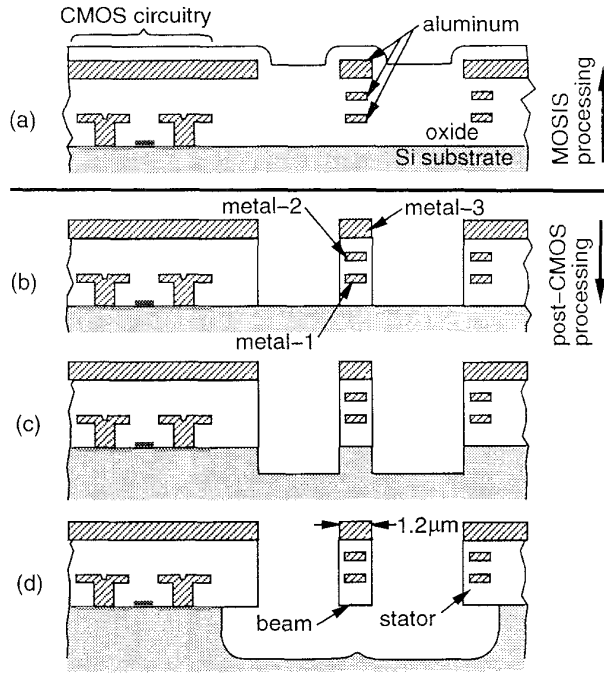
Fig. 1. Process flow cross-sections. (a) after MOSIS processing. (b) anisotropic oxide etch. (c) anisotropic silicon etch. (d) isotropic silicon etch for beam release.

Table 1. Post-CMOS dry etch steps.

	1) anisotropic oxide etch	2) anisotropic Si etch	3) isotropic Si etch
gas flow [sccm]	47 CHF_3 3 O_2	50 SF_6 12.5 O_2	50 SF_6 5 O_2
pressure [mT]	25	150	50
power [W]	200	100	100
etch rate [Å/min]	440	5000	9750

subsequent dry etching steps that create the laminated microstructures. All three of the dry etch steps take place in a Plasma-Therm 790 reactor and are summarized in Table 2 with the operating parameters. Oxide areas not covered by metal are anisotropically etched in a CHF_3/O_2 reactive ion etch (RIE) for 90 min, resulting in cross-section (b). Approximately 3500 Å of the aluminum mask is etched in this step. In (c), an optional anisotropic etch of the exposed substrate is performed using SF_6/O_2 RIE. Optimal etch parameters for this step were set using Jansen's 'Black Silicon Method' [8]. The etching characteristics are sensitive to silicon loading in the reactor, so dummy silicon wafers are added. A combination of rela-
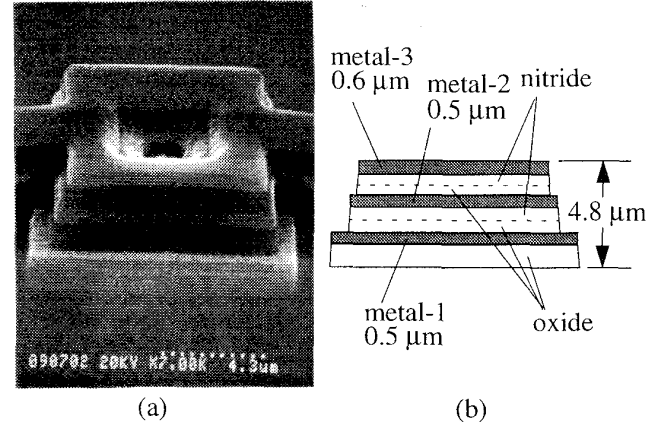

Fig. 2. Side view of a laminated structure after release. (a) SEM. (b) Schematic cross-section with approximate film thicknesses.

tively high O_2 flow and high pressure produces a SiO_xF_y passivating film on the silicon sidewalls that inhibits lateral etching. In (d), a final SF_6 isotropic plasma etch of the silicon releases the structure with a minimum amount of underlying surface roughness.

A scanning electron micrograph (SEM) of a released microstructure in shown in Fig. 2. The corresponding schematic details the laminated structure and gives approximate dimensions. Layout of the metal layers was overlapped deliberately to produce the sidewall stair-step pattern and highlight the various layers. (A nested via produces the indentation at the top of the structure.) The oxide RIE removes all material above the topmost metal layer and thins the metal-3 layer from its original thickness of 0.95 μm to about 0.6 μm. The dielectric between metal layers is a laminate of approximately 0.5 μm-thick oxide and nitride films.

A lateral comb-drive microresonator is shown in Fig. 3 after the anisotropic silicon etch and in Fig. 4 after the final release etch. Fine features usually associated with polysilicon micromechanics [9], such as interdigitated comb fingers and compliant meander springs, are made from the laminated structural material. The beams in the figure are 2.4 μm wide and 4.8 μm thick with gaps down to 1.6 μm between structures. Bulk silicon walls support the microstructure until after the final release etch. However, the holes in this particular plate are too small for proper release. We believe the failure to etch inside of very small holes is due to a build-up of passivating film in the holes during the oxide overetch. Careful inspection of Fig. 4 also reveals some preferential etching of the aluminum over the shuttle mass that occurs during the final release etch. The additional aluminum etching is due to a localized Si loading effect in the plasma. We are
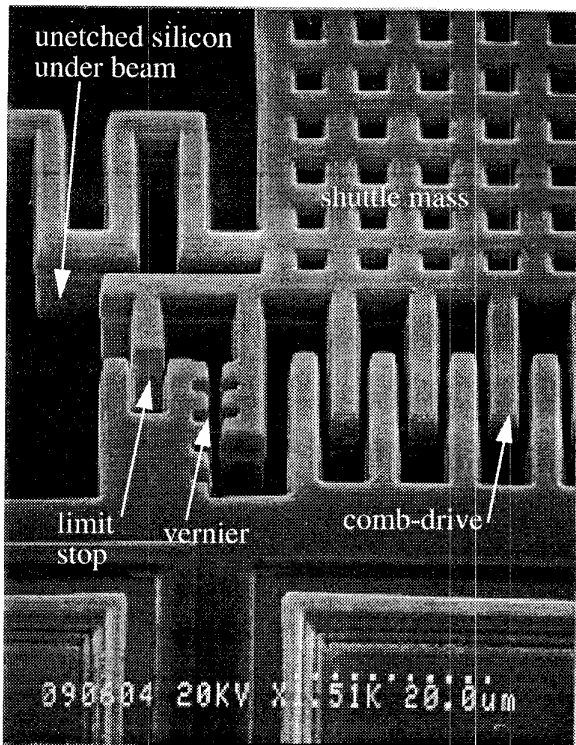
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Fig. 3. SEM of a section of a lateral comb-drive microresonator after the anisotropic etch of the silicon substrate (refer to the cross-section in Fig 1(c)). Several features of the microresonator are identified.
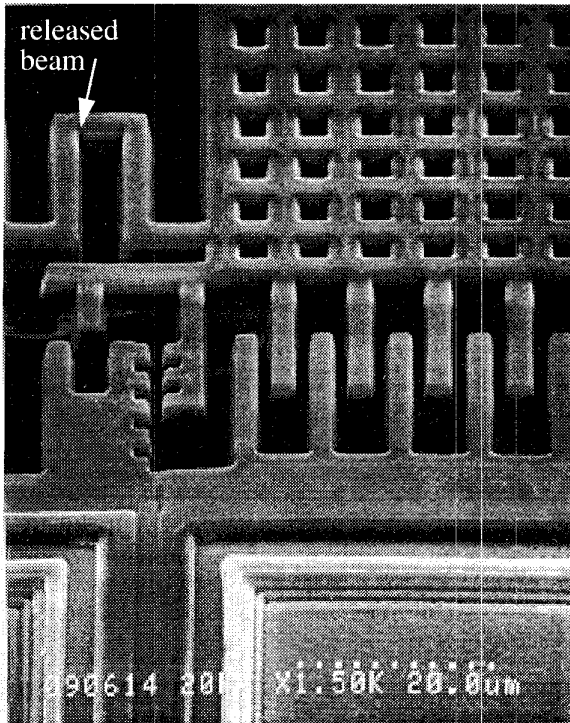

Fig. 4. SEM of the microresonator from Fig. 2 after the isotropic silicon release etch.

currently exploring a CF_4 oxide etch to eliminate the etch-resistant film in the holes. Other Si-etch plasma chemistries, such as XeF_2 may help alleviate the problem of aluminum etching [10].

The sidewall passivating film is not completely removed in the final release etch and appears as 'cobwebs' of less than 50 Å in thickness hanging off of the structures. These cobwebs are removed with a brief puff of compressed nitrogen. An alternate remedy that is used in our most recent runs is to eliminate the anisotropic silicon etch step completely. The original purpose of the anisotropic silicon etch was to prevent premature microstructure release; however deletion of the step has not adversely affected the structures.

MICROSTRUCTURE DESIGN AND CHARACTERIZATION

In most cases, minimum beam widths and gaps are set by the CMOS design rules. The scaling factor for the HP 0.8 µm process is $\lambda = 0.4$ µm. The minimum beam width is limited to 3 λ (1.2 µm), although then the design rule for metal-3 lines (5 λ) is broken. Beams need not be made with all three metal layers. Thinner, more compliant beams can be made by omitting the metal-3 and using either metal-1 or metal-2 as the top mask layer. The minimum gap between structures is 3 λ (1.2 µm). However, plates must be perforated with square holes that are at least 4 µm wide for release. The large holes avoid the dry-etch loading effects described in the previous section.

Anywhere a metal layer is not present the substrate will be etched. A sheet of metal-3 is used to cover all regions containing active MOS devices or other electronic components. However, a gap in metal-3 is necessary for electrical isolation between external pads and the rest of the metal-3 plane. The interconnect arrangement is shown in Fig. 4. A metal-1 or metal-2 collar is inserted underneath the break in metal-3 to prevent the silicon etch from reaching the substrate surface. Such gaps in metal are also used to electrically isolate different conducting areas on suspended structures.

Resonant frequency values of three cantilever beams were measured optically to extract a preliminary value for
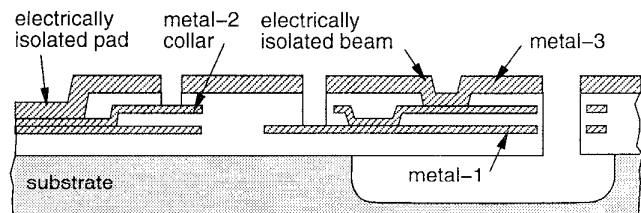

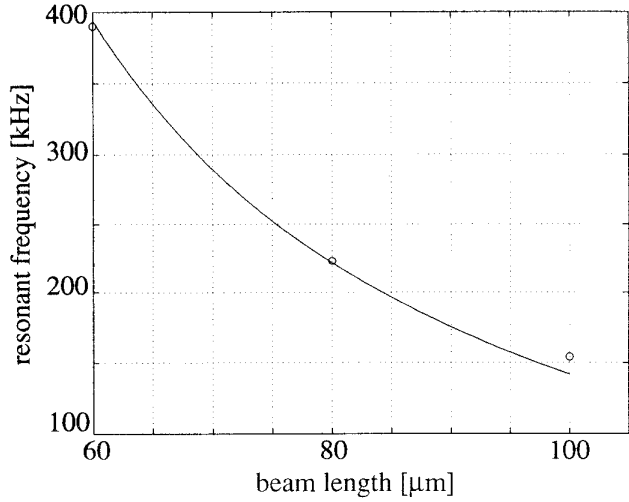Fig. 5. Schematic cross-section view of interconnect for electrical isolation.

Fig. 6. Resonant frequency vs. cantilever beam length. Points are measured values, the solid line is an analytic best fit using 63 GPa as the effective Young's modulus.

an effective Young's modulus. The beams were excited by lateral electrostatic actuators placed near the tips. Resonant frequency values are plotted as a function of beam length in Fig. 6. The data is fit with the analytic equation for resonant frequency of a homogeneous beam,

$$f_r = 0.56 \sqrt{\frac{EI}{mL^4}} \quad (1)$$

where L is the beam length, EI is the effective lateral beam stiffness, and m is the mass per unit length. The beams are of width 1.2 μm, height 4.8 μm, and have lengths of 60, 80, and 100 μm. An effective stiffness value of 1.5×10^{-13} N-m^2 gives a least-squares fit to the data, where the density of the aluminum, oxide, and nitride films are assumed to be 2700 kg/m^3, 2500 kg/m^3, and 3100 kg/m^3, respectively. The stiffness corresponds to an effective Young's modulus of 63 GPa. Future measurements will determine how much the effective Young's modulus of the beams depends on the bending direction and the laminated structure.

Polysilicon microstructures are restricted to application of a single voltage on the movable structure, since it is made from a homogeneous conductive material. Multiple independent electrostatic actuation is enabled by the laminated microstructure process.

One example of multi-conductor electrostatic actuation is the self-actuating spring shown in Fig. 7. A multiple conductor meander spring alternates the order of conductors along the 93 μm-long suspension beams. By applying a voltage across the conductors, a dipole pattern is formed which produces an attractive electrostatic force. The integrated force along each meander compresses the
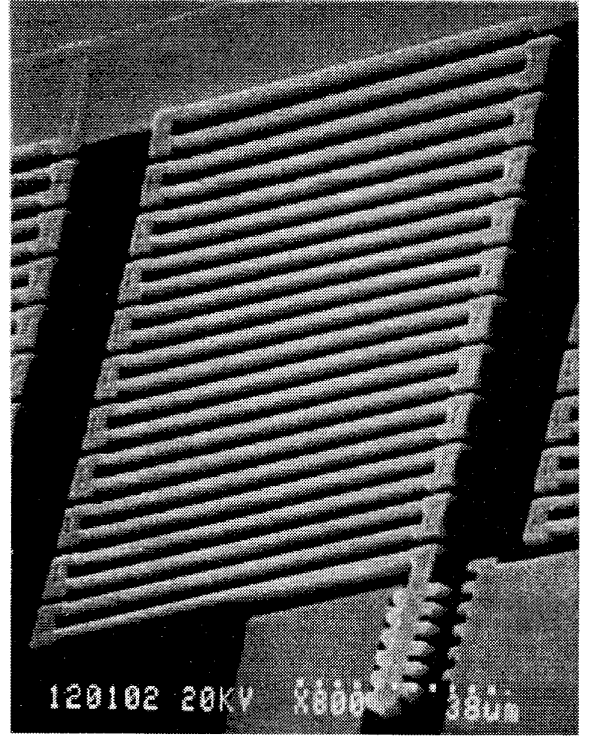

Fig. 7. SEM of a self-actuating spring test structure with 22 meanders. The spring compresses with applied voltage. A vernier, shown near the bottom of the micrograph is used to measure position.

spring. Similar piezoresistive self-actuating springs made from quartz have been reported previously [11].

In resonant operation, the third eigenmode of the spring is the lowest excited mode. Higher-order lateral spring modes are observed at higher excitation voltages and frequencies. Measured and simulated resonant frequency values are given in Table 2 for the lowest-order resonance. The finite-element simulation uses the effective Young's modulus value extracted from the cantilever measurements. Cross-section measurements from the cantilever beams are used to predict the sidewall geometry of the self-actuating spring in the simulations. Measured and simulated values match to within 6%, demonstrating reasonable accuracy of the effective Young's modulus value in predictive design. The systematic error is attributed to a small error in the spring cross-section extraction.

An 11 V sinusoidal signal applied to the 22-meander spring in air gives a tip-displacement amplitude of 1 μm. No series dc voltage is applied. The displacement is substantial for an electrostatic actuator fitting in an 107 μm-wide, 109 μm-long area. Polysilicon resonators of comparable size and thickness have a lower resonant amplitude for the same applied voltage. The test structures have withstood up to 90 V without experiencing breakdown.

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Table 2. Lowest-order resonant frequencies of the self-actuating spring test structures. Measured results and finite-element simulation are compared.

Meanders	f_v (measured)	f_r (simulation)	Δf_r
12	27.5 kHz	25.8 kHz	-6.2%
22	14.9 kHz	14.2 kHz	-4.7%
32	10.3 kHz	9.7 kHz	-5.8%

A charging effect is observed in the springs which lessens the effect of dc voltage on the static force. For the self-actuating springs, the time constant is on the order of 1 s. We believe that built up charge in the beam oxide and nitride layers are shielding the dc field lines. A dc force can be obtained by chopping the applied voltage with balanced high-frequency square-wave modulation.

Curling of the structural material arises from the residual vertical strain gradient in the laminated structures. The measured tip displacement of several 1.4 mm-long, 3.6 µm-wide, 4.8 µm-thick beams is 200 ± 30 µm, which corresponds to a nominal radius of curvature of 4.2 mm. Beams made from other laminated combinations of layers will have different values of strain gradient. The self-actuating spring in Fig. 7 is curled out of the substrate plane by about 4 µm at the tip. However, since the distributed actuation mechanism is self-aligned throughout the spring structure, the curling does not adversely affect the electrostatic force.

An x-y stage is shown after the oxide etch in Fig. 9. The stage is suspended by eight self-actuating springs which provide differential x-y actuation of the center beams. Several other electrical connections are routed to the structure through thin two-metal meander springs. Perforated plates mounted on two sides of the structure provide parallel-plate electrostatic actuation in the vertical direction.

Another example of multi-conductor x-y actuation is the nested two-axis comb-drive resonator, shown in Fig. 9 after being released from the substrate. Multiple aluminum interconnect lines are routed through the suspension to provide independent electrical connections to the inner comb fingers.

CONCLUSIONS

The simple new method for fabricating high-aspect-ratio microstructures in standard CMOS is an attractive technology with which to make low-cost high-performance integrated sensors and actuators. The dry release
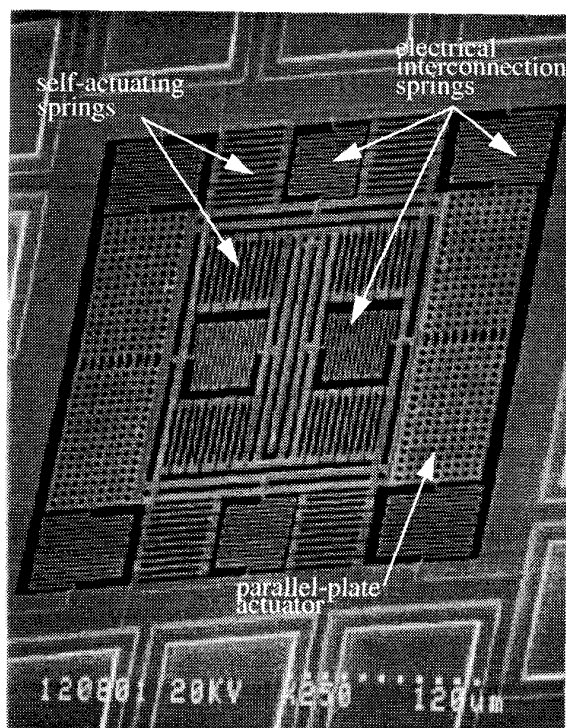

Fig. 8. SEM of an x-y stage suspended by self-actuating-spring electrostatic actuators.
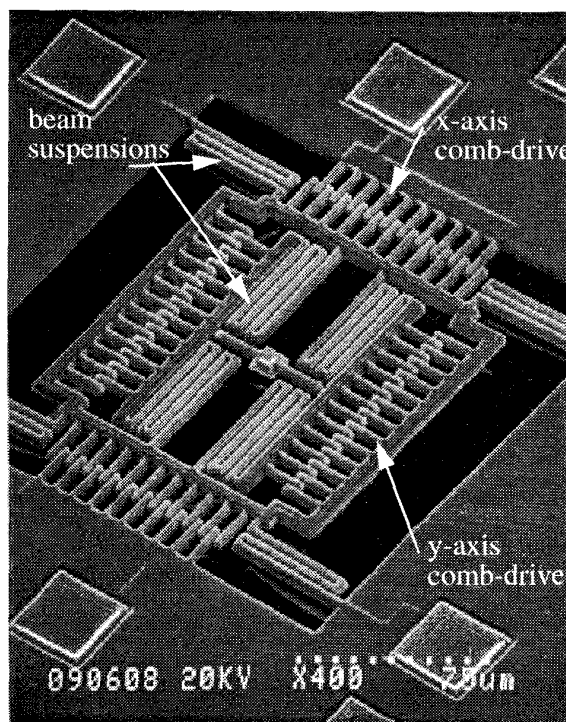

Fig. 9. SEM of a released two-axis nested comb-drive resonator.

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process side-steps the sticking and yield problems associated with competing bulk wet-etch release methods. Beam widths are limited by the minimum allowable metallization linewidths in a given CMOS process. The laminated microstructure process leverages continuing advances in CMOS technology. Microstructures and CMOS devices both scale with the process, enabling subsequent performance improvements in microsensors and microactuators made with this technology.

Multi-conductor laminated microstructures provide additional design flexibility. The conductors can be used for 3D actuation, sensing, and shielding. However, charging is an issue that must be understood thoroughly before robust microsystems can be designed. Self-aligning lateral microactuators, such as the self-actuating springs, avoid problems with out-of-plane curl.

ACKNOWLEDGEMENT

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