INTEGRATED MICROELECTROMECHANICAL SYSTEMS IN CONVENTIONAL CMOS

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Abstract

Electrostatically actuated microstructures with high-aspect-ratio laminated-beam suspensions are fabricated using conventional CMOS processing followed by a sequence of maskless dry-etching steps. The metallization and dielectric layers, normally used for electrical interconnect, now serve a dual function as a structural layer. The post-CMOS microstructural reactive-ion etch produces near vertical sidewalls, enabling micromechanical beam widths and gap spacings down to 1.2 μm. The process is tailored for design of lateral electrostatic actuators and sensors integrated with 0.5 μm CMOS. The fabricated *x-y-z* microstage devices demonstrate the technology for future use in inertial sensor and probe-based data storage system applications.

Introduction

In recent years, researchers have demonstrated a variety of microsensors and microactuators based on mature VLSI process technology. One promising approach to manufacturable integration of MEMS and electronics is to start with a mature CMOS process and build MEMS capabilities into it. In 1989, researchers at Simon-Frasier University were the first to report microstructures made from thin films in standard CMOS processes [1]. Several researchers are actively working in this area on devices such as inertial sensors [2][3], cellular force sensors [4], thermal flow sensors [5], thermally isolated transistors [6], and infrared detectors [7].

At Carnegie Mellon, we have developed a unique process to fabricate high-aspect-ratio microstructures suitable for lateral electrostatic actuation and compatible with standard CMOS. Applications include inertial sensors, resonant sensors, and probe-based data storage.

Our current application focus is to create a probe-based data storage system on a chip using our high-aspect-ratio CMOS microstructure technology. In particular, we are studying narrow-gap lateral electrostatic actuators for microstages having precision *x-y-z* position control. Probes, such as tunneling tips, are fabricated on the stages to enable precision manipulation with respect to a storage media surface. Ultimately, we envision arrays of thousands of tips operating in parallel for rapid overall data access and with system storage densities approaching 10 GB on a single 1 cm^2 chip module.

CMOS-Based High-Aspect-Ratio MEMS

We have developed a unique CMOS-based process that produces laminated oxide/aluminum structures with near vertical sidewalls and beam widths and gaps down to 1.2 μm [8][9]. The minimum beam widths and gaps are limited only by the CMOS interconnect design rules and not by structural sidewall etch limitations. This process allows fabrication of very compliant lateral (and vertical) suspensions and narrow-gap lateral electrostatic actuation. The lateral actuation capability is useful in design of sophisticated microaccelerometers, gyroscopes, and microstages for probe manipulation or optical beam steering.

A simplified process flow for making the fine-line microstructures is shown in Fig. 1. First, standard CMOS is fabricated using the MOS Implementation Service (MOSIS) [10]. Currently, we

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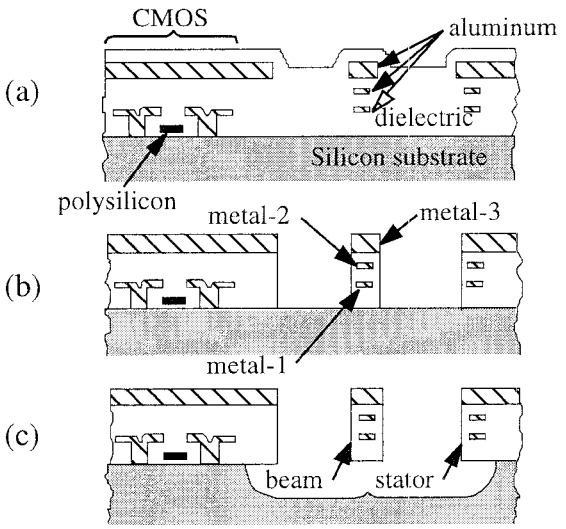

Fig. 1. Cross-sections of the process flow for making high-aspect-ratio microstructures in standard CMOS. (a) First, standard CMOS chips are fabricated using the MOSIS process service, (b) After RIE of the dielectric layers. (c) Last, a dry plasma etch of the silicon substrate releases the beams.

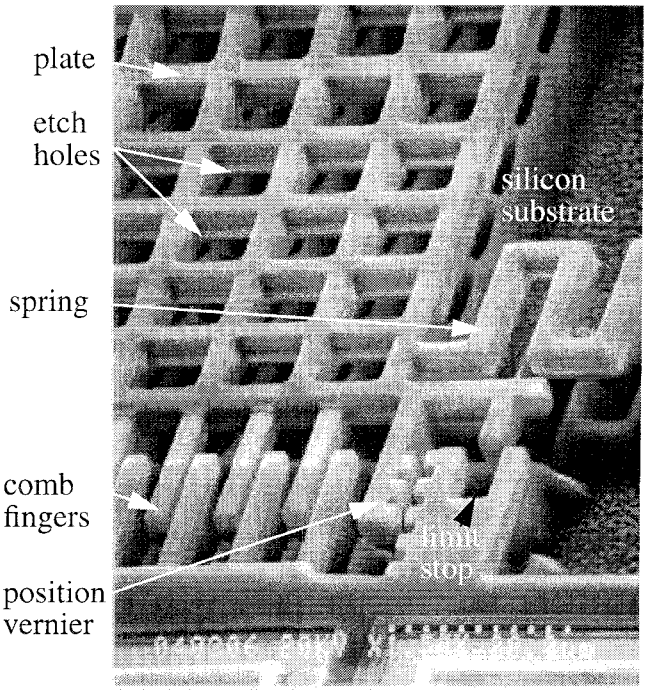

Fig. 2. SEM of a section of a lateral comb-drive microresonator after the silicon release etch. The noted features demonstrate the successful fabrication of very small beams and gaps in standard CMOS.

are using the Hewlett-Packard 3-metal 0.8 μm and 0.5 μm n-well CMOS processes.

After the dice are received from MOSIS, they are placed in a CHF_3/O_2 reactive-ion etch (RIE). The topmost metal layer acts as a highly selective mask which defines the microstructures. The RIE etches the dielectric that is not covered with aluminum, including the overglass, intermetal dielectric, and field oxide. Some aluminum is eroded by ion milling during the etch process. However, through proper adjustment of the etch power, pressure, and gas flows, near vertical dielectric sidewalls are formed without fully eroding the top aluminum layer.

The last process step is a dry SF_6/O_2 plasma etch of the silicon substrate for microstructural release. The plasma chemistry etches silicon without attacking the microstructural sidewalls. The etch has a vertical to lateral etch rate of about 2:1, thereby releasing sufficiently narrow structures from the substrate. Typically, we etch down about 25 μm into the silicon, which undercuts structures up to 16 μm wide. Larger structures must have etch holes for proper release.

Silicon is etched wherever the aluminum layers are absent. Therefore, the CMOS circuitry must be protected by the top metal layer, leaving only two electrical interconnect layers available. Measurements of transistor threshold voltage verify that there is no degradation from the RIE etching.

A corner of an example microstructure, an electrostatically actuated lateral resonator, is shown in Fig. 2 after the silicon release etch. This device has very narrow beam widths and gap spacings, which are features normally associated with polysilicon micromechanics [11]. The interdigitated comb fingers and compliant meander springs are 2.4 μm wide and 4.8 μm thick with gaps down to 1.6 μm between structures. Etch holes allow the large plate to be released. The Si ridges under the suspended structure result from the 2:1 vertical to lateral silicon etch ratio.

The spring is made of laminated beams with alternating metal and dielectric layers, as shown in Fig. 1(c). The effective Young's modulus of the laminated beams is approximately 61 GPa, about the same value as solid aluminum. Embedded aluminum traces wind through the meander springs to provide interconnect between the comb fingers and bond pads. The resonator plate mass experiences an electrostatic attractive force upon application of a potential across the gap between comb fingers.

Applications

An example of a microstage for *x-y-z* position control of a tip is shown in Fig. 3. A central tip pad is suspended from a rigid frame by four meander-beam springs that are more compliant in the *y* direction than in the *x* direction. Likewise, the outer frame is suspended from the substrate by four other meander-beam springs. These outer springs are more compliant in the *x* direction.

The outer frame of the stage is actuated in the *x* direction by two interdigitated comb-finger electrostatic actuators [11]. Independently, the inner section of the stage is actuated in the *y* direction by a second set of comb drives. Wiring is routed through the suspension to provide electrical connections to the inner comb fingers. The nested *x-y-z* actuation is enabled by the ability to put multiple conductors inside a single mechanical structure. Similar devices cannot be created with polysilicon surface micromachining since polysilicon structures are made from a homogeneous conducting material.

Currently, the best microstages we have tested resonate about ±2 μm in *x* and *y* with an applied ac voltage of 16 V. We are developing a new generation of compact actuators with a target of ±5 μm static displacement with 15 V.

Conclusions

Many of the manufacturing difficulties with fabricating MEMS in a standard CMOS process stem from the inability to control the microstructural sidewall geometry when using the stacked-

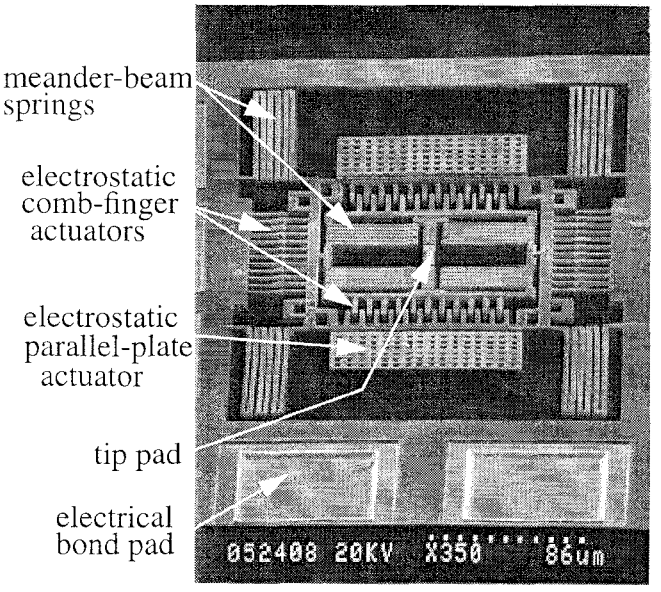

Fig. 3. Scanning electron micrograph of a released *x-y-z* microstage.

via etch. These problems are solved by moving the microstructural etch from the main CMOS flow to an optimized post-processing step. The resulting process can produce microelectromechanical devices with narrow beam width and gap spacing as required for lateral electrostatic actuation.

We have developed several *x-y* microstage devices using our high-aspect-ratio CMOS microstructure process. These devices demonstrate the potential for inertial sensor and probe-based data storage applications. Future designs will integrate sense electronics with efficient actuation mechanisms for higher performance.

Acknowledgment

The author gratefully acknowledges the work of L. R. Carley, D. Guillou, M. S.-C. Lu, S. Santhanam, and M. L. Reed. The fabrication work was supported in part by the National Science Foundation under grant ECD-8907068. The research effort was sponsored by the Advanced Research Projects Agency under the Air Force Office of Scientific Research, Air Force Materiel Command, USAF, under grant number F49620-94-1-0192. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained

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