

CMOS-Based Sensors

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Abstract—This paper provides an overview of CMOS-based sensor technology with specific attention placed on devices made through micromachining of CMOS substrates and thin films. Microstructures may be formed using either pre-CMOS, intra-CMOS and post-CMOS fabrication approaches. To illustrate and motivate monolithic integration, a handful of microsystem examples, including inertial sensors, gravimetric chemical sensors, microphones, and a bone implantable sensor will be highlighted. Design constraints and challenges for CMOS-MEMS devices will be covered.

I. INTRODUCTION

Motivation for monolithic integration of sensors with electronics primarily stems from four themes: lowering manufacturing cost, solving interconnect bottlenecks, miniaturizing total systems and improving performance. Integration enables manufacture of very high volume products (i.e. millions of units per year) at per-unit manufacturing cost that is driven lower by moving as much manufacturing as possible to batch processing. Good examples are the inertial sensors made by Analog Devices (ADI) [1] and MEMSIC [2]. Second, integration can readily handle interconnect from parallel sensors through time multiplexing of signals or by performing on-chip signal processing to perform data reduction. For example, optical and uncooled infrared imagers have much greater interconnect than is available to take off chip via bondpads. Although the Texas Instruments digital mirror display is not a sensor, it also exemplifies the need for electronics integration to handle its millions of data and actuator voltage signals [3]. Third, integration can address the ultimate miniaturization that is highly valued in future applications such as implantable medical sensors and wearable embedded sensors. Cell phone manufacturers are already demanding such component miniaturization. Fourth, integration can improve sensors, primarily through reduction and repeatability of the capacitive parasitics. For example, Freescale Semiconductor integrated their line of tire pressure sensors with the capacitive sense interface electronics to minimize the influence of variable capacitive parasitics in the harsh environment [4].

CMOS has by far made the largest impact of all microfabrication technologies to date, being responsible for the vast majority of electronics. Its easy availability has spawned a large assortment of methods to integrate microsensors with CMOS. This overview will cover the basic approaches taken to creating microsensors in accessi-

ble foundry CMOS and highlight some advantages of CMOS MEMS by discussing a handful of specific devices from Carnegie Mellon.

II. INTEGRATED MEMS FABRICATION

Several CMOS-based sensors, such as CMOS imagers, Hall effect magnetic sensors and piezoresistive stress sensors, directly exploit transistor or resistor properties. In these cases, modifications to the CMOS process may not be necessary. For other kinds of sensors, some form of MEMS processing is required to enable the transduction. Numerous process flows have been developed to incorporate MEMS into CMOS. A nearly comprehensive discussion is given in [5]. CMOS-based MEMS processes are generally binned as having pre-CMOS, intra-CMOS and post-CMOS micromachining.

Only a few attempts have been made to perform MEMS processing prior to the CMOS steps. To be accepted into a foundry CMOS run, the micromachining steps must end with a clean, flat, device-grade silicon surface. No contaminants or low melting point metals (such as aluminum) may be incorporated. As a result of these constraints, the few process flows to date with MEMS steps embedded within the CMOS flow have utilized captive foundries willing to accept unorthodox substrates or integrate MEMS process steps within their flow.

Modular fabrication approaches have been tried where polysilicon layers were deposited first, followed by uninterrupted CMOS processing [6]. A hydrofluoric acid etch of the sacrificial oxide was performed after CMOS as part of a final MEMS release process module. An alternative modular integration method was demonstrated through bonding of a silicon device wafer onto a handle wafer having etched cavities [7]. The exposed backside of the device wafer was then polished and electrochemically etched to thin down to the uniform 10 μm -thick epitaxial silicon on its front side for subsequent CMOS processing. Further modular approaches exist where the microstructures are deposited on top of CMOS. Compatible low-temperature materials include sputtered aluminum [8], LPCVD polysilicon germanium [9], and electroplated nickel [10].

Most of the approaches to post-CMOS micromachine structures starting with unaltered foundry CMOS are summarized in Fig. 1. The seminal work in Fig. 1(a) used fron-

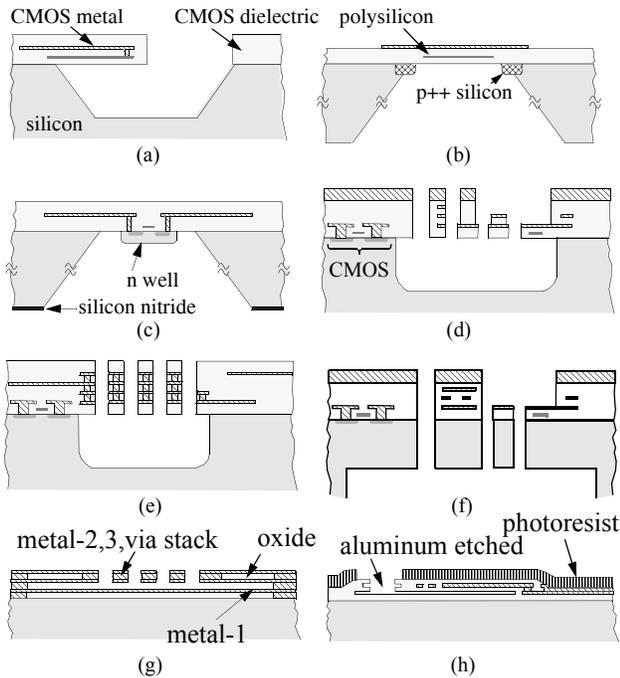


Figure 1. Processes using unaltered foundry CMOS processes as modules: (a) frontside wet etched CMOS-MEMS [11], (b) backside wet etched CMOS-MEMS [12], (c) backside electrochemical etch stop on n-well [13], (d) frontside dry etched with CMOS metal mask [14], (e) frontside dry-etched with photoresist mask [15], (f) frontside silicon DRIE CMOS-MEMS [16], (g) sacrificial oxide etch [17], sacrificial aluminum etch [18].

side wet silicon etch to release microstructures and is commonly used for microhotplate sensors [11]. Backside etch approaches in Fig. 1(b) and (c) have given rise to many devices, primarily using thermally isolated plates and resonant beams [12][13]. The high-aspect-ratio CMOS MEMS process in Fig. 1(d) created structures through a sequence of frontside dry etch steps [14]. Structural sidewalls are defined by RIE and masked by the first metal layer encountered. A subsequent DRIE of the exposed silicon substrate sets the spacing from the microstructures to the substrate followed by a timed isotropic silicon etch to undercut and release the structures. The process in Fig. 1(e) used photoresist instead of the metal as the structural mask. Bulk silicon structures in Fig. 1(f) were formed by first performing a backside DRIE etch to thin the substrate and then releasing the structure through frontside silicon DRIE [16]. In Fig. 1(g), microstructures made from CMOS metal bounded by continuous vias were released by an inductively coupled plasma etch of the surrounding CMOS dielectric layers [17]. The process in Fig. 1(h) employed select CMOS aluminum layers as the sacrificial material, thereby releasing metal structures encased in oxide [18].

III. FRONTSIDE DRY-ETCHED CMOS-MEMS

In this section, an overview of some device examples from the Carnegie Mellon frontside CMOS-MEMS process in Fig. 1(d) will help to illustrate issues with design of CMOS-based MEMS. The primary attributes of the process

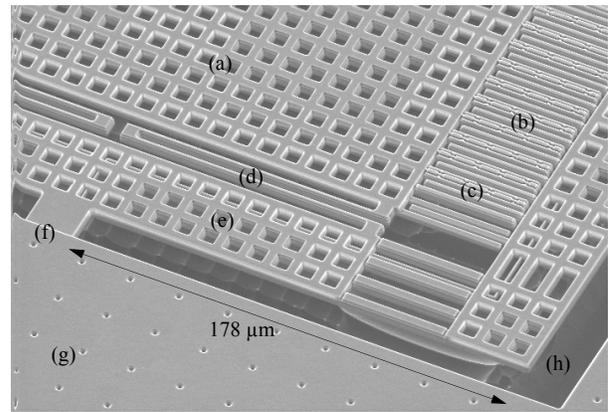


Figure 2. One quadrant of a 376 μm by 400 μm lateral capacitive accelerometer in the Jazz Semiconductor 0.35 μm 4-metal CMOS process. The primary features are (a) plate mass, (b) sense fingers, (c) self-test fingers, (d) folded beam spring, (e) stator curl-matching frame, (f) anchor, (g) aluminum in field, (h) silicon etch pit. [SEM by S. Santhanam]

are the ability to make narrow beams and gaps, the use of the multi-level interconnect within the microstructures for routing sensor and actuator signals, and the proximity to electronics to minimize parasitic capacitances. The minimum width of beams is set by the CMOS metal width design rules, which in some cases extend below 0.5 μm . CMOS metal-to-metal spacing rules can also extend below 0.5 μm , which can be challenging though possible to etch with aspect ratios of 10:1. A well-known issue with oxide etching in the presence of aluminum is aluminum fluoride polymer deposition due to aluminum on the chip being incorporated into the plasma. A photoresist mask must block the aluminum in the field for all cases, except when processing of small mm-sized chips where the aluminum loading is negligible.

Accelerometers, gyroscopes, infrared sensors, gravimetric sensors, electrothermal actuators, RF tunable capacitors and RF mixer-filters have been made in the front-side CMOS MEMS process. The low-g accelerometer in Fig. 2 is one of the most complex microstructures made to date, with embedded wiring to connect the fully differential capacitive bridge and self-test actuators. A nearly identical design in TSMC 0.35 μm CMOS achieved a measured noise floor of $45 \mu\text{g}/\sqrt{\text{Hz}}$ ($1 \text{ g} = 9.8 \text{ m/s}^2$), which was set by Brownian noise of the proof mass. The motion is sensed with balanced capacitive bridge modulation, with each sense capacitance being around 40 fF. The on-chip CMOS preamplifier is essential to achieving the input-referred sensitivity of 0.3 mV/g. The parasitic capacitance on the high impedance node is between 60 to 80 fF and included contributors from the interconnect and the sense transistor gate input capacitance. To compare with a non-integrated approach, a direct bondwire connection to an external chip with 100 μm pads and the equivalent preamp would have an additional 250 fF of capacitance and reduce the sensitivity by a factor of 3. The improvement in signal to noise performance for this scale of sense capacitance is good, but it is not usually the prime motivator for switching to the CMOS implementation.

Modern CMOS processes require stress matching of the interconnect dielectric and metal layer stack to enable chem-mechanical polishing of 8" and above wafer diameters without delamination of the thin films. This is fortuitous for MEMS design as the out-of-plane curl from stress gradients is smaller when made in CMOS with minimum gate lengths better or equal to $0.35\ \mu\text{m}$ (corresponding to 8" or larger wafers). In any CMOS process, however, the field oxide has particularly high compressive stress. For minimum out-of-plane curl, the field oxide must be removed by placing the CMOS "active" mask in microstructural areas. The accelerometer in Fig. 2 curls around $0.5\ \mu\text{m}$ from the plate center to edges, compared to over $10\ \mu\text{m}$ curl for similar structures made in $0.5\ \mu\text{m}$ CMOS. Although the curl still is large compared to homogeneous microstructural materials, it is compensated through design of a frame around the proof mass that keeps the stator and rotor fingers aligned.

Stress gradients may also arise in the in-plane directions for CMOS-MEMS structures having embedded interconnect. Each metal layer toward the top of the stack can be designed with a smaller width to ensure that the lateral stress gradients from oxide sidewalls are eliminated (The right two beams in Fig. 1(d) illustrate this design.) This stress bimorph effect is exploited in lateral self-assembly and electrothermal actuators, where the embedded metal lines are offset on purpose to accentuate the bending stress, as illustrated by the leftmost beam in Fig. 1(d) [19].

A recent use of the CMOS-MEMS technology is as a platform for gas chemical sensor microsystems. Highly integrated multi-sensor platforms at ETH Zürich exploit their backside etched CMOS-MEMS technology (Fig. 1(c)). An example is an integrated system with microhotplates for calorimetric detection, interdigitated electrodes for capacitive detection and a resonant silicon cantilever for gravimetric detection of the respective chemophysical properties of polymers drop cast onto the sensors [20]. At Carnegie Mellon, work is ongoing on scaling down gravimetric gas chemical sensors to improve sensitivity. The approach incorporates a microgroove on a cantilever, as shown in Fig. 3, so that the beam can be filled with polymer without affecting the air gaps on the sides of the beam that are used for electrostatic stimulus and capacitive detection. A gas sensitive polymer is ink-jet deposited onto a well area located at the base of the cantilever and wicks into the groove under capillary forces. Due to the small size of the cantilever, the sensor had a measured sensitivity of $76\ \text{fg}/\text{Hz}$ under closed-loop oscillation.

Membranes for pressure sensors and microphones and microspeakers can be formed by first releasing a beam mesh structure with minimum sized uniform gaps and then depositing a conformal coating of parylene or CVD polymer to seal the mesh, as shown in Fig. 4. The measured noise for a prototype $0.61\ \text{mm}^2$ membrane was $46\ \text{dB SPL}$, A-weighted and was limited by $1/f$ transistor noise [22]. This technology

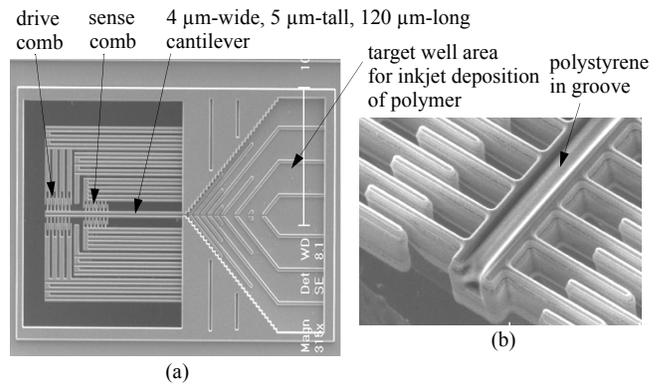


Figure 3. CMOS-MEMS resonant cantilever for gravimetric gas chemical sensing showing (a) the full device and (b) a close-up of the cantilever tip where the $2\ \mu\text{m}$ -wide groove is filled with polystyrene. The combs have $5\ \mu\text{m}$ -tall $0.6\ \mu\text{m}$ -wide fingers and gaps. After [21].

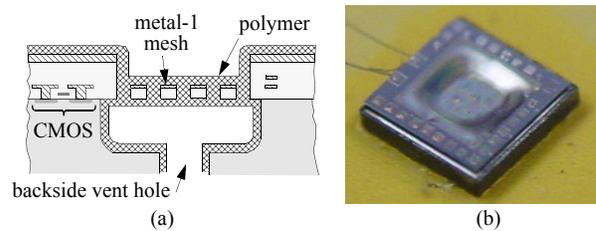


Figure 4. CMOS-MEMS membrane technology showing (a) the process flow and (b) membrane deflection under $80\ \text{V}$ applied. [Chip photo by J. J. Neumann].

is the basis for multi-membrane microphones being developed by Akustica [23].

One of the most promising future applications for CMOS-based sensing is in bioimplantable sensors. The possibility exists to combine one or more sensors along with an on-chip coil antenna and circuitry for wireless power and data transmission in a single chip under $4\ \text{mm} \times 4\ \text{mm}$. Such a small form factor could provide effectively non-invasive sensing capabilities in parts of the body and is a prime example of where miniaturization is the key motivation to integrate. At Carnegie Mellon, a thrust is underway to implement this vision for *in situ* bone stress measurement [24]. The sensor is intended to be placed directly into an open fracture site to provide a direct measure of bone strength while the bone is healing. For this sensor application, the CMOS chip must be textured throughout the surface of the chip to accommodate bone cell growth (osteoconductivity) and integration. Texturing is achieved through silicon DRIE that forms an array of $60\ \mu\text{m}$ square silicon posts. Osteoconductivity has been demonstrated with passive silicon textured chips coated with titanium for biocompatibility. In the prototype 6×6 sensor post array is shown in Fig. 5, piezoresistive bridges are located at the top surface of the posts to provide data for stress tensor extraction. Beams span the posts to interconnect the array to row-column scan circuitry. Sample devices are currently being embedded in plastic for testing.

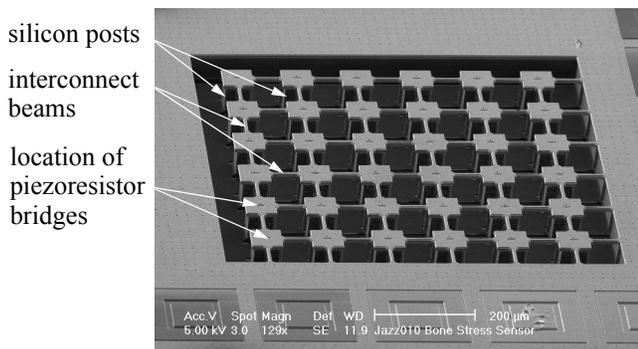


Figure 5. Engineering prototype of a bone implantable stress sensor. The silicon posts, which are spaced on 120 μm pitch, house piezoresistive bridges and are sized for in-growth of bone cells. [SEM by J. F. Alfaro]

IV. CONCLUSION

The multitude of fabrication approaches for CMOS-based sensors are generally motivated by the vision of low-cost, miniature multi-sensor systems. To date, there are a handful of commercial CMOS-MEMS successes tied to captive foundries. The emergence of MEMS capabilities within non-captive foundries has made it possible to pursue a fabless business model with or without a monolithically integrated product. The steady refinement of manufacturing approaches that use foundry CMOS in a modular fashion bodes well for future successes in the fabless business model for on-chip sensors.

The main raw performance enhancement provided by electronics integration is the reduction and repeatability of capacitive parasitics on high-impedance interconnect. The argument for integration becomes much stronger as sensor sizes shrink further. One science application driver for continued downscaling is in detection of single molecules where cantilevers are often below 100 nm in cross sectional dimensions. Capacitive motion sensing to replace the predominant optical sensing alternatives is possible but will require on-chip integration to lower parasitics.

The foundry CMOS integration approach enables the use of system design advances in one sensor application to make rapid progress on related applications. Analog Devices and Freescale have achieved some of this benefit in their respective lines of inertial sensors and pressure sensors. This modular design approach is being taken in CMOS-MEMS gas chemical sensor work at ETH Zürich as well. The bioimplantable sensor area may become a future beneficiary of this approach due to the potential for reuse of on-chip wireless antenna and circuit designs for various medical sensor applications.

V. ACKNOWLEDGMENT

The author thanks his current and former students whose prior work is highlighted.

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