CMOS-MEMS Resonant Mixer-Filters

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Abstract

RF mixer-filters made by micromachining composite metal and dielectric interconnect layers within foundry CMOS are a potential component in on-chip receivers. Through the electrostatic voltage-squared nonlinearity, mixer-filters down-convert to an intermodulation frequency set by the mechanical resonance enabling higher gain than resonant filters having a RF signal output. The research is leading toward resonant mixer-filters integrated with preamplifiers and having 0 dB insertion gain with sub-mW power.

Introduction

The cellular phone market, along with emerging wireless markets in modular USB port plug-ins, RF identification tags and sensor networks continue to motivate research to implement ultra-low power RF transceivers completely on chip. The RF filters remain the primary components to monolithically integrate. Receiver architectures that introduce resonant microelectromechanical filters have been proposed to solve this filter integration challenge. Micromechanical structures in vacuum exhibit a narrow bandpass filtering function with quality factors (Q) above 1000, reaching nearly 100,000 for crystalline materials like silicon. In the RF filter application, mechanical resonance must be set at the band of interest, meaning 800 MHz and higher for cell phones. However, such high-Q MEMS resonators cannot be widely tuned so proposed architectures employ arrays of resonant filters, with each filter tuned to a different channel. Proving out a single-chip technology with arrayed filters that span the entire communication band and meet the required band-reject specifications remains a challenge. Steady progress toward this goal is being made by groups using bulk- and shear-mode microresonators.

An alternate architecture in Fig. 1 incorporates an array of MEMS resonant mixer-filters as a parallel receiver. Electromechanical mixing of RF and LO inputs and narrow-band filtering is performed in each single passive device [1]. In this architecture, the micromechanical resonant frequency sets the intermediate frequency (IF) for each mixer-filter. This IF filtering requirement is much lower than in the direct filter architecture, so that relatively large motions attained through mechanical bending modes can be exploited (when compared to motion from bulk or shear modes). An analog preamplifier is required to detect the motional displacement current of each resonator. The resulting MHz IF signal then can be converted to digital form.

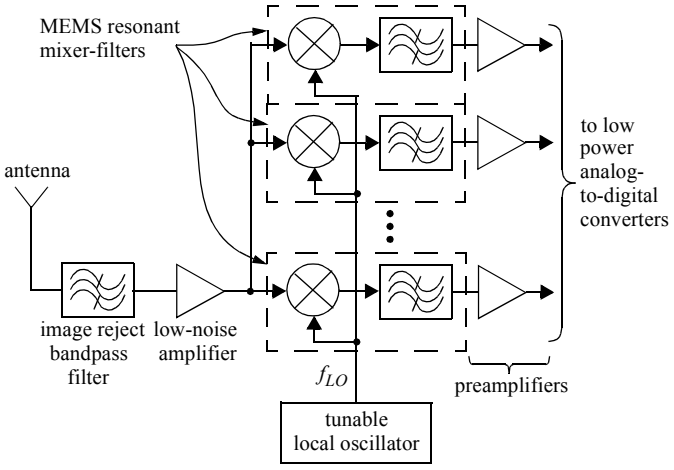

Figure 1. Parallel receiver front-end architecture exploiting MEMS resonant mixer-filters.

The potential advantage of using MEMS mixer-filters over direct RF MEMS filters is their ability to operate with constant conversion gain at arbitrarily high RF, thereby side-stepping the trade-off of resonant frequency vs. output sensitivity. The mixer-filters retain advantages promoted by other MEMS filters of small footprint and low power, enabling channel "tuning" by selecting between device outputs. There is a practical limit to input frequency that is set by parasitic input shunt capacitance and series resistance. Hence, integration of the mixer-filter devices directly with the active RF electronics is essential to any eventual implementation. The CMOS-MEMS approach provides a solution available to device designers now through existing foundries.

Mixer-Filter Operation

The CMOS-MEMS cantilever single-ended mixer-filter shown in Fig. 2(a) and (b) provides a simple example to explain the principle of operation. The cantilever is driven with an approximate parallel-plate electrostatic force,

$$F_e = -\frac{\varepsilon_o A}{2(g+x)^2}(v_{RF}-v_{LO})^2 + \frac{\varepsilon_o A}{2(g-x)^2}(V_P-v_O)^2, \quad (1)$$

where A is the electrode area, g is the electrode gap, ε_o is the permittivity in the gap, V_p is a dc "polarizing" voltage that generates motional current, and v_O is the output voltage comprising the output signal, v_o, and a dc bias $V_{O,bias}$ from inter-

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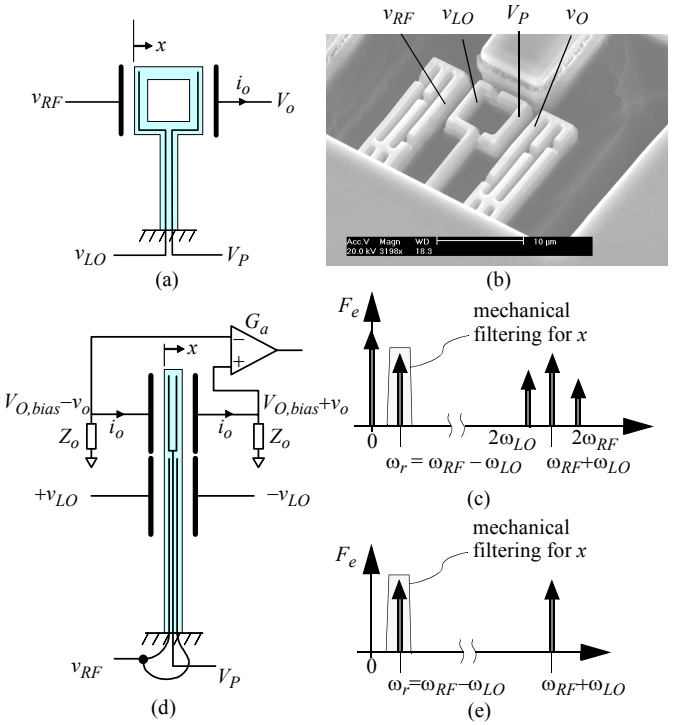

Figure 2. CMOS MEMS cantilever resonator mixer-filter. (a) Schematic of single-ended drive. (b) SEM of single-ended device sized for 1 MHz center frequency. (c) Force spectrum of single-ended drive. (d) Schematic of differential drive. (e) Force spectrum of differential drive.

face electronics. The voltage-squared nonlinearity generates the frequency terms in Fig. 2(c). The force stimulates the motion, x, according to the micromechanical mass-spring-damper transfer function of the cantilever. When operated in vacuum, the air damping is eliminated and narrow bandpass filtering centered at the mechanical resonance, ω_r, is obtained. Therefore, the only significant motional term is the mixing term $v_{RF}v_{LO}$. The square frame at the end of the cantilever is meant to space apart the RF and output nodes in an attempt to reduce feedthrough.

Interference signals located at $2\omega_{RF} \pm \omega_r$ and $2\omega_{LO} \pm \omega_r$ must be eliminated by the front-end image rejection filter. The interferer at $\omega_{LO} - \omega_r$ may be removed either by the image rejection filter or by quadrature mixing, which requires another mixer-filter driven by a quadrature phase LO [2]. The image filter solution avoids the need to match mixers, but then places a lower limit on the mixer IF equal to the width of the communications band.

Interference of RF tones having a beat frequency equalling ω_r must be eliminated by differentially driving the cantilever. A basic differential topology is shown in Fig. 2(d). Feedthrough from the drive to sense electrodes no longer couples across the beam width, so the square frame is eliminated. By driving one gap at $v_{RF} - v_{LO}$ and an opposing gap at $v_{RF} + v_{LO}$, as indicated in Fig. 2(d), the sum of forces is

$$F_e = \frac{2\varepsilon_o A}{g^2}[a v_{LO} v_{RF} - V_P' v_o], \tag{2}$$

where the effective polarizing voltage across the output gaps is $V_p' = V_P - V_{O,bias}$, a is a factor accounting for the locations of the sense and drive electrodes, and $x << g$ is assumed. The force is linear with v_{RF}, unlike in (1). Excluding the x term in the denominator does not affect the first-order mixer analysis, but it is important to include when assessing effects on additional nonlinear terms. The differential drive and sense cancels the RF beat frequencies along with the dc, $2\omega_{RF}$ and $2\omega_{LO}$ force terms (Fig. 2(e)). The on-chip mixer gain can be found through a derivation similar to that in [1] and is

$$G = G_a\left(\frac{v_o}{v_{RF}}\right) = aG_a\left|\frac{Z_o}{2Z_o + R_x}\right|\left(\frac{V_{LO}}{V_P'}\right), \tag{3}$$

where Z_o is the termination impedance, V_{LO} is the LO amplitude and G_a is the preamp gain. The motional resistance is

$$R_x = \frac{Bg^4}{(\varepsilon_o A V_P')^2}, \tag{4}$$

where $B = k / \omega_r Q$ is the mechanical damping coefficient and k is the spring constant. To maximize conversion gain, Z_o should be as large as possible (even for small-gap mixers), taking into account the additional constraint of lowering the effective Q if Z_o is resistive. The maximum Z_o is limited by the input impedance of the interface circuit and the parasitic capacitance. An optimal polarizing voltage for maximum gain exists and is

$$(V_P')_{opt} = \frac{g^2}{\varepsilon_o A}\sqrt{\frac{B}{2}\sqrt{(\omega_r C_o)^2 + 1/R_o^2}}, \tag{5}$$

where R_o and C_o are parallel resistance and capacitance comprising Z_o. As Z_o increases, the optimal polarization voltage decreases and R_x increases to "match" with Z_o. Note that this maximum gain optimization is allowable for the IF mixer design, but is not applicable to direct RF MEMS resonator filters, which must be optimized for power transfer, not voltage gain. Therefore, with mixer design, minimizing C_o is important to performance and provides motivation for an integrated preamp, where parasitic capacitance can be in the fF range. Given a fixed C_o, the maximum achievable gain is

$$G_{max} = aG_a\frac{\varepsilon_o A}{g^2}\frac{V_{LO}}{2\sqrt{B\omega_r C_o}}, \tag{6}$$

so for high gain, it is best to select a low resonance IF with large area electrodes and narrow gaps.

CMOS MEMS Fabrication

Mixer-filters can be made in almost any MEMS technology, however CMOS-MEMS integration boasts three main advantages: i) The output capacitance can be minimized with

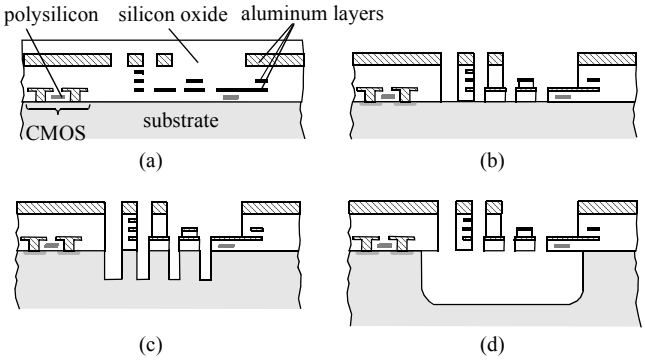

Figure 3. CMOS MEMS process. (a) Foundry 4-metal CMOS. (b) Oxide RIE. (c) Silicon DRIE. (d) Isotropic silicon etch.

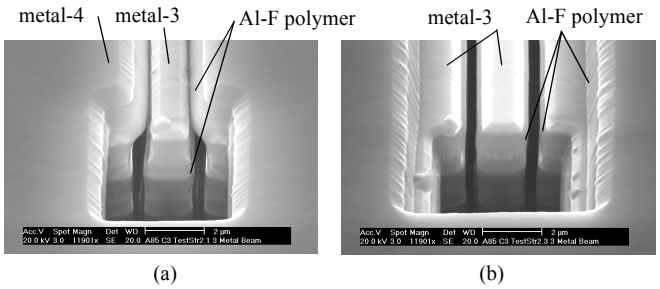

Figure 4. Test structures for assessing the design rules for gap etch. (a) Metal-4 layed out with its sidewall in line with metal 3, demonstrating metal-4 bloat and excessive sidewall polymerization. (b) Metal-4 layed out with 2 μm cut-in from metal-3 edge, with reduced polymerization. The gap widths are 0.25 μm on the left side and 0.35 μm on the right side. After [4].

short interconnect to low-capacitance on-chip interface circuits, which achieves optimally high gain; ii) The embedded aluminum interconnect inside the microstructures enables mixer-filter design with independent isolated electrodes for electrostatic force drive and for motional current output with minimal feedthrough; and iii) The interconnect series resistance can be kept well under 50 Ω, which is needed to keep the input RF signal from attenuating.

The CMOS MEMS process, illustrated in Fig. 3, creates micromechanical structures by etching the composite metal and dielectric interconnect layers after the foundry CMOS is completed [3]. The process starts with a CMOS chip shown in cross-section in Fig. 3(a). The RF MEMS passives and circuit modules shown in this paper are made in 4-metal 0.35 μm CMOS (TSMC) and BiCMOS (Jazz Semiconductor) processes. The structures are micromachined after the foundry process is completed through a sequence of dry etch steps. The first post-CMOS micromachining step (b) is a CHF_3:O_2 reactive-ion etch (RIE) of the inter-metal dielectric stack. The RIE etches any dielectric that is not covered with metal. The etch is masked by the first metal layer encountered and thus acts to define the microstructural sidewalls. The top-most metal layer sets the thickness of the structure. The second post-CMOS micromachining step (c) is a timed directional deep-RIE of the exposed silicon substrate. This step sets the spacing from the microstructures to the substrate. The final step (d) is a timed isotropic silicon etch in an SF_6 plasma to undercut and release the structures.

The minimum allowable gap is constrained by sidewall polymer buildup and by aspect-ratio dependent retardation of the etch. An aluminum fluoride polymer deposition of up to 0.2 μm occurs locally on sidewalls during the plasma oxide etch, due to aluminum on the chip being incorporated into the plasma. Micromechanical sidewalls and gaps formed with the top aluminum layer (metal-4) are particularly affected, as the aluminum is exposed to the plasma for longer periods of time. An excessive amount of polymer is present on these sidewalls, as shown in Fig. 4(a). The metal-4 layer also experiences a bloat of around 0.1 μm with respect to layout. A design solution to enable very narrow gaps is to enforce a cut-in of metal-4 with respect to the lower metal layers as shown in Fig. 4(b).

Mixer-Filter Results

The cantilever resonant mixer-filter shown in Fig. 2(a) was the first CMOS-MEMS topology to demonstrate mixing [4]. Fully differential single-cantilevers remain to be tested. In these initial tests, differential signals were produced by setting polarizing voltages of opposite polarity on two 435 kHz resonators layed out side by side. The mixer-filter response, shown in Fig. 5(b), remains unchanged for input frequencies from 10 MHz to 400 MHz. Q was 1400 for pressure below 1 T. Mixing has been demonstrated up to 3.2 GHz, however significant feedthrough exists from on-chip capacitive coupling from v_{LO} and v_{RF} to the on-chip preamp bias current line and directly to the preamp inputs. These feedthrough sources have been reduced substantially through improved interconnect placement on 1 MHz designs recently tested.

Scaling of interconnect spacing provides a gap of around 0.5 μm for 0.35 μm CMOS, however the current RIE process limits the gap that can be cleared to around 1 μm. The optimized mixer gain scales as $1/g^2$, so there is motivation to reduce the gap even further. In custom MEMS processes, common practice is to deposit a conformal CVD thin film and later release etch to form the gap. A design solution in CMOS-MEMS used self-assembly actuators on the "stator" electrodes to form narrow gaps. The design concept for lateral self-assembly in CMOS-MEMS beams is illustrated in Fig. 6 [5]. The lower metal layers in the beam are offset with respect to the top metal layer of the beam, as shown in (a). The residual stress difference between the silicon oxide and the aluminum, shown in (b), gives rise to a lateral displacement upon microstructural release, as shown in (c). By designing the metal offset to switch sides halfway down the beam length, the displacement mimics that of a guided-end beam. These beams when placed in parallel make stiff actuators to reduce low-order modes arising from the "stator" electrodes.

Self-assembled gaps were used in the square-frame resonator (SFR) in Fig. 7, which also has an inherent differential

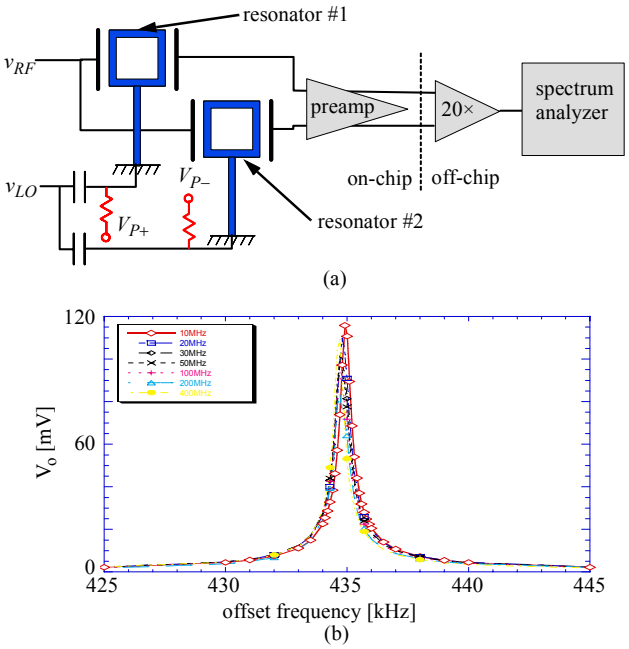

Figure 5. Dual cantilever resonator mixer-filter. (a) Test schematic. (b) Mixer output measurement with pressure of 1 T, $|V_{LO}| = |V_{RF}| = 1$ V. After [4].

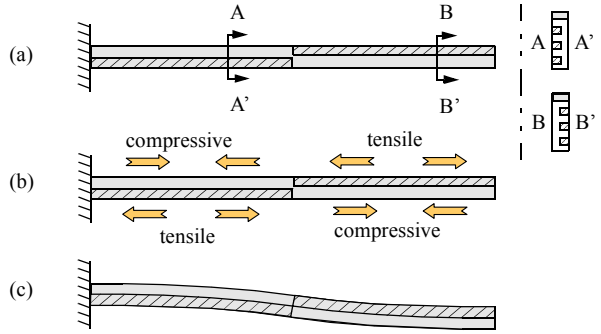

Figure 6. CMOS-MEMS lateral self-assembly actuator. (a) Cantilever in layout, illustrating embedded metal offset inside beam. (b) Residual stress distribution before release. (c) Displacement after release.

input and output [6]. Upon microstructural release, the self-assembly actuators engage with a limit stop intended to set the gap to 0.3 µm. The filter gain of the SFR, operating in the primary bending mode at 6.486 MHz, is –24.95 dB with a Q of 786 (Fig. 7(c)). The measured gain was improved by 10 times over a design with a fixed 0.68 µm gap and fixed V_p'.

Conclusion

Foundry CMOS-MEMS technology is capable of producing resonant mixer-filters with Q's around 1000 and integrated with preamplifiers on chip. The design freedom in CMOS-MEMS can create differential signal paths that reject interferers, shield against feedthrough, and reduce load capacitance. Multiple channel select filters can be made on a single chip, since the frequencies are set by lateral design features. MEMS mixer gain is invariant with input frequency below the input

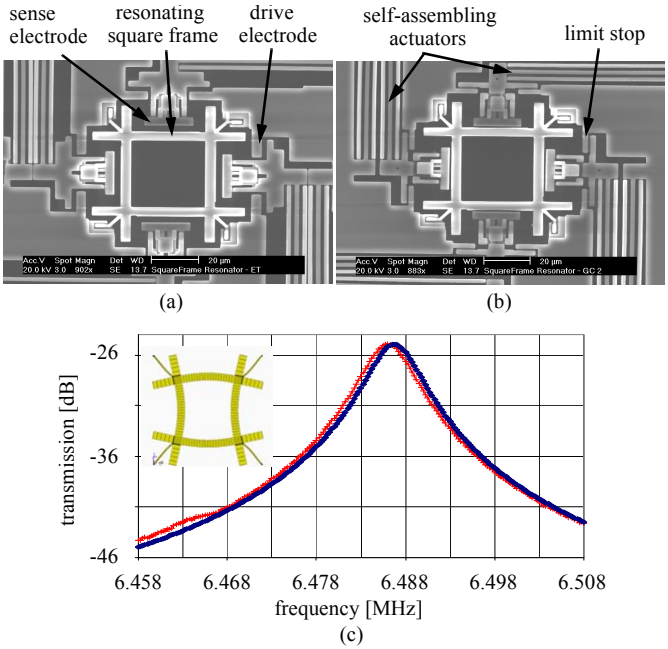

Figure 7. Square frame resonator (a) with self-assembly actuator designed open, (b) with self-assembled gap set by limit stops. (c) Block diagram. (d) Measured and simulated resonance peak after feedthrough subtraction and a 26 dB on-chip preamp gain. $P = 40$ mT, input voltage = 0 dBm, input polarizing voltage = 6 V, V_p' = 18.6 V. After [6].

RC cutoff, making the potential for impact greater at higher frequency bands. A goal of 0 dB insertion loss at IF in the 10's of MHz is expected to be reached with a combination of self-assembled gap reduction to 100 nm, optimally sizing the preamp for maximum system gain, and arraying of coupled resonators to further boost signal.

Acknowledgement

The author thanks the students who have contributed including Jay Brotz, Fang Chen, Altug Oz and Janet Stillman. Special thanks to Tamal Mukherjee, Umut Arslan and Chiung-Cheng Lo for their contributions and proofreading. The work was funded through DARPA DAAB07-02-C-K001.

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