Rapid Yield Estimation as a Computer Aid for Analog Cell Design

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Abstract

A rapid yield estimation methodology that aids the analog circuit designer in making design tradeoffs that improve yield is presented. ARYE (Analog Rapid Yield Estimator), a CAD tool that implements this methodology for op amps has been incorporated into ACACIA, the CMU Analog Design System, in order to allow analog designers to quickly explore the impact of design changes on yield. A design example using ARYE and ACACIA to enhance the yield of a two-stage op amp design will be presented.*

1. Introduction

An ever increasing fraction of new application specific integrated circuit (ASIC) designs incorporate analog circuit blocks. A significant fraction of integrated circuit analog cells may fail to satisfy performance specifications due to global variations in the fabrication process (parametric yield loss); in part, because the performance of analog circuits is highly sensitive to variations in process parameters, compared to that of digital circuits. Although circuits can also fail due to *functional* causes [1], in this paper we consider only parametric yield failures. Since the yield of an ASIC determines the manufacturer's profitability and the yield is dominated by the cells which have the worst yield, estimating and optimizing the parametric yield of analog circuit designs prior to manufacturing is an important problem.

Estimating parametric yield loss is made difficult by the complex dependence of analog circuit performance on process parameters; i.e., it is not sufficient to verify the analog circuit performance at a few process corners (slow-slow, fast-fast, etc.). Yield modeling and optimization for digital circuits has been greatly debated in recent years as overviewed in [1]. Currently, analog circuit yield is typically estimated by simulating the behavior of many instances of the design, each instance representing a possible outcome of the fabrication process. Unfortunately, this approach typically requires hours, days, or even weeks of computer time, severely limiting its use. Typically, at most a final yield estimation of a design would be performed in this manner before fabrication.

The goal of the proposed yield estimation method is to allow the analog circuit designer to rapidly compare the parametric yield loss of many possible circuit alternatives. In this paper, ARYE, an analytical model based tool for rapid yield estimation of two-stage op amps will be described. First yield estimation will be discussed and then the proposed rapid yield estimation method will be presented. Next, incorporation of the rapid yield estimation strategy into the ACACIA [2] synthesis framework is described. Finally, an example of how ARYE can be used to improve the design of a two-stage op amp will be presented.

2. Rapid Yield Prediction

2.1. Parametric Yield Loss

In order to simplify the design task, designers often assume that device parameters, such as an MOS device threshold voltage, are either a single value, or are bounded by an upper and lower value. In reality, however, these device parameters exhibit a continuous range of variations due to fluctuations in the IC fabrication process; and further, the variations of the device model parameters are correlated. Designs which anticipate the worst-case combinations of device model parameters can be vastly conservative. It is important to note that, due to the correlations between the distributions of device parameters, it is not sufficient to obtain the means and variances of device parameters in a given process and generate sample distributions with the aid of a random number generator. Instead, it is necessary to go back one step further and use independent fabrication process variables such as the diffusion times and temperatures as the random variables. The effect of the global process disturbances that lead to parametric failures can be modeled by a process simulator [3, 4] which assumes that the probability distributions of a set of independent fabrication process variables are known. The process simulator takes independent random variables

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for process disturbances as well as for the process controls and the mask geometries and generates any desired number of sets of device model parameters (such as k' and V_{TO} for each device).

In order to accurately estimate the yield of an analog circuit, a number of hypothetical instances of the circuit would typically be generated using a process simulator. For each instance, a set of device model parameters would be generated. Two alternatives are possible: either there is a unique model for each device size for each instance; or, when device mis-matches are important, there is a unique model for each device for each instance. It is important to note that process simulators use a different set of process parameter variances (typically much smaller) for devices within the same circuit as compared with devices on different wafers. Next, circuit simulations would be run with each set of device model parameters, and the circuit's performance extracted from the simulator's outputs. For each hypothetical instance, the simulated performance would be compared to the performance specifications, and the number of designs which satisfy all of the specifications are counted. The estimated parametric yield is simply the fraction of the simulated designs which meet all of the specifications. Accurate estimation of parametric yields often requires that thousands of instances of the circuit be simulated and evaluated.

2.2. Rapid Yield Prediction Method

Unfortunately, the large number of circuit simulations required to accurately estimate parametric yield limit its usability for complex analog circuits. A frequently employed, though by no means rigorous, alternative is to simulate for a small set (e.g., 10) of instances whose device model parameters were chosen to represent the typical variations of a given process. Obviously, this method is most successful for an older process where designers have acquired significant experience. Given this state of yield estimation, it is difficult to use yield estimations to guide tradeoffs during the design process.

The time consuming aspect of analog circuit yield estimation, as presented above, is the circuit simulations and extraction of performance from the simulations. An alternative to using simulation that is applicable to a wide range of analog circuits is to use approximate models to analytically predict circuit performance in terms of device parameters [5, 6, 7, 8]. In general, analytical predictions of performance require very little computational time, making rapid parametric yield estimation possible. However, the accuracy of these yield estimates will be no better than the accuracy of the analytical model. It is therefore important to verify the accuracy of the analytical model over the expected range of device parameter variations. Note, as will be seen in section 3.1 analytical performance predictions are already a part of the circuit synthesis strategy; therefore, their use does not impose any additional overhead in this case. On the other hand, to use this technique for a new type of circuit requires the creation of an analytical model that can accurately predict the circuit performance. In some cases, formation of an accurate analytical model can be quite difficult, which is a potential drawback to this method. Note, because this method for rapid yield prediction is based on analytical models, a final yield estimation using full SPICE-type simulations, as presented above, is still desirable for verification of the yield prediction.

A block diagram for the yield estimation process is shown in Fig. 1. To further increase the speed of rapid yield estimation, the process simulations needed to generate device model parameters are performed once for a given process, and a library of device model parameters, with appropriate statistics for the given fabrication process, are stored and used during the rapid yield estimation process. The yield prediction loop uses analytical models to estimate the yield of the original circuit. The analytical prediction of the performance for each instance of process is compared with the performance specifications to determine which instances met the specifications (passed) and which did not (failed). The number of chips that passed (i.e., the number of device parameter sets for which the nominal design meets the performance specifications) divided by the total number of chips (i.e., the total number of device parameter sets) is the yield prediction.

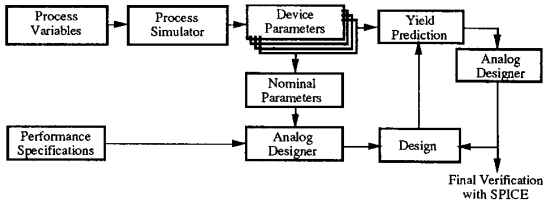

Figure 1: Block Diagram of the Yield Estimation Method

3. Yield Prediction within ACACIA

3.1. ACACIA System

ACACIA is an experimental design framework developed at Carnegie Mellon University with the aim of facilitating the analog circuit design process [2]. ACACIA can generate layouts of frequently used analog modules, starting from performance specifications. As can be seen in the ACACIA block diagram (see Fig. 2), there are four major components, OASYS - including the analytical circuit models, which generates sized transistor schematics; KOAN-ANAGRAM, which transforms sized schematics to mask geometries, ARYE, a rapid yield estimation method that also uses the analytical circuit models, and a graphical interface that enables the analog circuit designer to explore various design tradeoffs.

Automated synthesis in ACACIA is performed by OASYS [6, 9] which takes specifications (e.g., for an op amp these would be gain, unity gain frequency, etc.), for selected analog circuit blocks (currently, OASYS

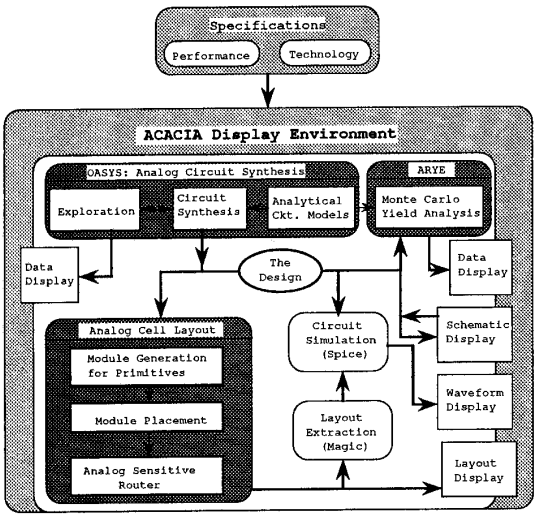

Figure 2: Block Diagram of ACACIA Analog Design System

implements op amps and comparators) using nominal device model parameters for the process in which the circuit will be implemented. In OASYS, as in several other recent analog synthesis methodologies (e.g., [10, 11]), synthesis is based on approximate analytical circuit models that predict the performance of a fixed topology in terms of the design parameters (e.g., transistor sizes and operating points) and device model parameters. Although errors on the order of 5-10% may occur in the process of generating a mathematically tractable set of equations, the power of this formulation is great. One possible drawback of this approach is that these equations must be developed for each separate topology. However, one unique feature of OASYS is its use of fine-grained hierarchy, which allows it to have an analytical model for current mirrors and differential pairs which can be reused and can itself contain multiple styles (e.g., Widlar mirror and cascoded mirror). Although OASYS only has design equations for two block-level op amp topologies, because of the available combinations of sub-block topologies, approximately 72 useful op amp topologies are represented by these equations (for example, see Fig. 3). ARYE currently operates on all two-stage op amp topologies currently available in OASYS, which is > 40 device-level topologies.

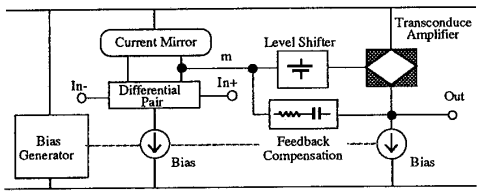

Figure 3: Block Diagram of Hierarchical Two-Stage Op Amp Model

3.2. User Interface for Yield Prediction

Since it relies on the analytical models that are already part of the ACACIA/OASYS framework, ARYE fits synergistically into the framework giving the designer improved capabilities. As new synthesis targets are added, predicting their yield will be straightforward. In order to make maximize the usefulness of this tool, an interactive interface to yield prediction is provided. Graphic displays showing the yield statistics give the designer the necessary information to adjust the design to improve yield. A screen dump showing the interactive interface between ACACIA and the analog designer performing yield enhancement is shown in figure 4.

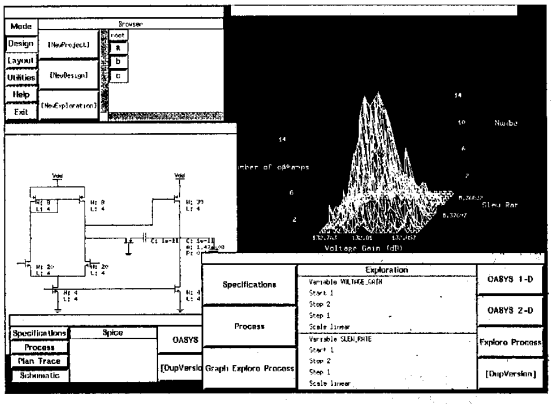

Figure 4: ACACIA Designer Interface for Yield Exploration

4. Example of Rapid Yield Prediction

In this section, a brief example of how ARYE can aid the designer of a two-stage op amp will be presented. In this case the analog designer first uses OASYS to automatically select the specific two-stage op amp topology and device sizes to meet a set of desired performance specifications. Prior to any yield predictions, the FABRICS II process simulator [1] was used to generate a library of device parameters, assuming the process flow for a hypothetical CMOS process. ARYE was then invoked to rapidly estimate the yield of the selected op amp circuit. In this case, the estimated parametric yield was only 48.6%, based on 1000 design instances. The computation time required for yield estimation was 41.5 seconds on an approximately 13 MIP workstation. Fig. 5 shows the yield surface for the phase margin and the unity gain frequency (UGF) of the initial design. The heavy lines on the base grid of Figures 5 and 6 indicate the required performance specifications, phase margin > 45 degrees and UGF > 1 MHz. Designs in front of and to the right of these solid lines fail to meet specifications. Note, the specification that was violated most often was the desired phase margin of 45 degrees.

Yield enhancement can proceed in two possible ways. Either the analog designer can directly suggest changes in individual devices sizes, or he can make

changes in the requested performance specifications to OASYS and rerun the synthesis. In this case, looking at Fig. 5, it is clear that while the phase margin is being frequently violated, the UGF values are far from their lower limit specification, 1 MHz. Since decreasing the UGF (which, for example, can be achieved by increasing the compensation capacitor) also increases the phase margin, a balance between yield loss due to phase margin and due to UGF can be struck. Fig. 6 illustrates the effect of a 5% increase in the compensation capacitor and a 16% increase in the output stage bias current (all that was allowed given the power constraint). The yield in this case increased to an estimated 89%.

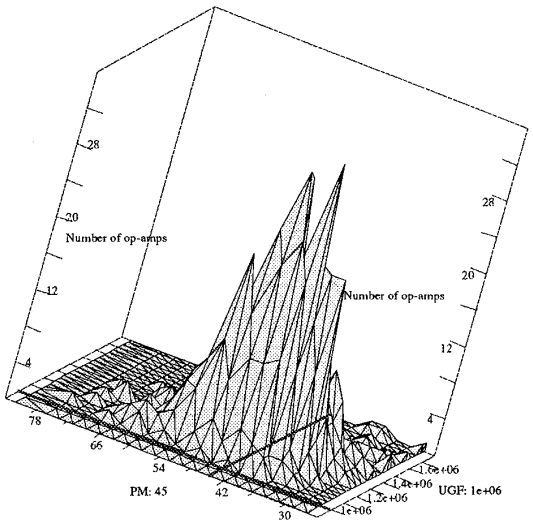

Figure 5: Yield Surface for an Op Amp Design A.

5. Conclusions

In this paper a new rapid yield estimation strategy that uses analytical models was presented. This rapid yield estimation strategy is particularly well suited for used with synthesis systems that use analytical models (e.g., OASYS). An example of the use of ARYE to improve the yield of an op amp demonstrates the potential benefits of this approach for improving circuit designs.

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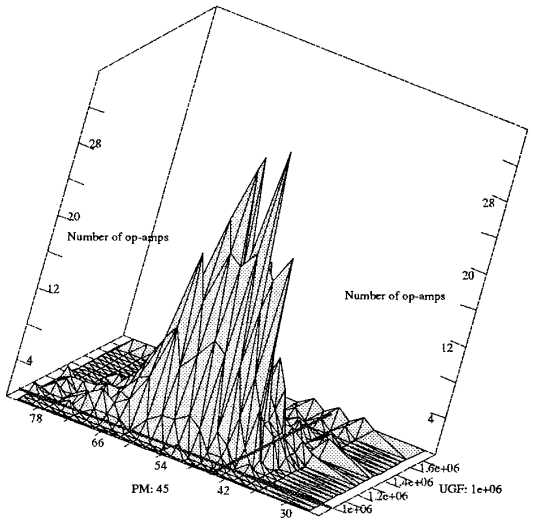

Figure 6: Yield Surface for an Op Amp Design B.