Micromachined High-Q Inductors in 0.18μm Cu Interconnect Low-K CMOS

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ABSTRACT

Spiral inductors fabricated in a 0.18μm 6-level copper interconnect low-K dielectric process are described. A post-CMOS maskless micromachining process compatible to copper interconnect and low-k dielectric CMOS has been developed to create inductors suspended 100μm above the substrate with sidewall oxide removed. Such inductors have higher quality factors as substrate losses are eliminated by silicon removal and have higher self-resonant frequency due to removal of inter-turn dielectrics. Micromachined inductors have the potential to extend the useful operational frequency range of CMOS RF circuits. Quality factors of greater than 7 were obtained at 5.5 GHz for inductors with silicon undercut and inter-turn oxide removed, compared to a Q of 4 for inductors having only their inter-turn oxide removed but without silicon undercut.

I. Introduction

Advances in silicon technology, with decreasing feature sizes and application of novel materials, are pushing circuit performance to higher frequencies. However, the performance of passive components have remained the same with substrate losses limiting performance at higher frequencies. To expand CMOS applications into the 5 GHz range, work has focussed on improving the Q factor of RF inductors by using custom process modules. These include fabrication of inductors with thick copper layers on sapphire substrates[1], and removal of the underlying silicon by wet etchants[2][3].

The micromachining process described here does not require additional masks. The fine line geometry structures can be defined by post-CMOS reactive ion dry etching, which is 100% compatible with CMOS design rules[4][5]. Combining the advantages of Cu interconnect technology with the CMOS micromachining process, it is possible to design high performance RF passive components that can leverage copper interconnect technology. Suspended inductors in a state-of-art six level copper interconnect and low-K dielectric CMOS processes for RF circuit applications have been fabricated. A combination of lower resistivity and lower skin depth of the copper over aluminum is advantageous at higher frequencies. The lower resistivity reduces ohmic losses in the copper inductor and the lower skin depth implies thinner copper layers at higher frequencies. Removal of sidewall oxide increases the self resonant frequency. Undercutting of the lossy silicon below the inductor improves the quality factor.

II. CMOS Micromachining Process

A 0.18μm 6-metal-level Cu interconnect low-K dielectric process offered by United Microelectronics Corporation (UMC)[6] was used to fabricate CMOS circuits and the inductors. The process flow, shown in Fig. 1, enables fabrication of micromachined structures in CMOS. The conventional CMOS processing (Fig. 1(a)) is followed by an anisotropic RIE with CHF_3 and O_2 to etch away oxide not covered by any of the metal layers, resulting in high-aspect-ratio vertical sidewalls (Fig. 1(b)). The following anisotropic (Fig. 1(c)) and isotropic silicon etch (Fig. 1(d)) removes the underlying silicon to release the microstructure[9][10]. The anisotropic etch is used to obtain the desired spacing between the inductor and the substrate. The isotropic etch undercuts the silicon beneath the inductor. The proposed process allows placement of circuits less than 30μm away from the inductor, while being suspended as far away from the substrate as desired.

The top metal layer used as an etch resist mask for the micromechanical structures is milled by 0.5μm in the Al interconnect process, resulting in an increased sheet resistance of about 30~40%. The etch rate of the copper mask is 70~80% lower than that of aluminum leading to very little reduction in the top metal thickness. This property of copper is advantageous for inductor applications where top metal resistivity determines the DC resistance.

The micromachined structural elements are formed by a sandwich of metal and dielectric layers. Due to the differences in residual stress of the two materials, the structures exhibit out-of-plane curl. The Cu interconnect structures have lower curl compared to Al interconnect structures as the out-of-plane bending moment of inertia of Cu-CMOS beam is 2.3 times that of 5μm-thick beams in a three-metal Al process[9].

III. Inductor Design

The inductor topology is shown in Fig. 2. To minimize the coil resistance and maximize the Q, within the specified area, an octagonal shape is chosen and all metal layers are utilized. The top two metal layers (metals 6-5) are combined as a single wire of about 0.7μm in thickness, to compose the inductor plus an output port. The other layers (metals 4-3-2-1) define the other output port wire having a total thickness of 1.5μm. The thickness of the top-most metal layer was reduced by

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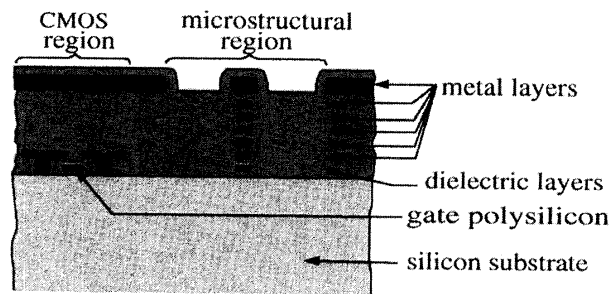
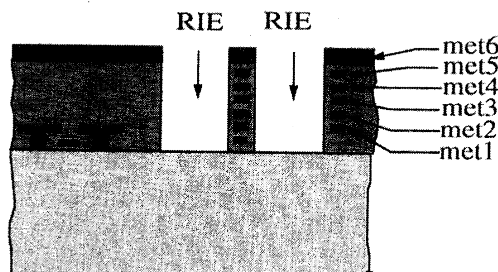


(a)



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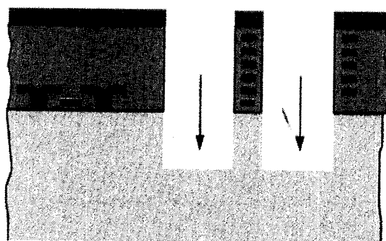

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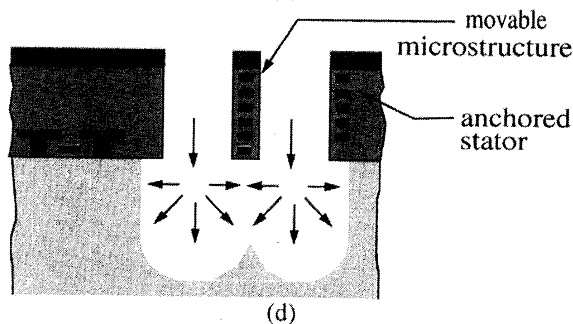

(d)

Fig. 1. Cross sections of device in each stage of the process flow.
(a) Device from CMOS processing.
(b) After anisotropic dielectric layers etch.
(c) After anisotropic Si etch.
(d) After isotropic Si etch to release the mechanical structure.

0.2μm due to ion milling during the anisotropic oxide etching. The width of all wires is 20μm. The metal layers are connected through stacked vias as seen in a FIB cross-section in Fig. 3. The lower resistance of the copper stack plug vias also helps reduce the DC resistance of the inductor. The lower dielectric constant of the oxide layers reduces the parasitic capacitance, leading to a higher inductor self-resonant frequency. An SEM of the released inductor after silicon undercut is shown in Fig. 4.

Fig. 2. Schematic of the inductor design. The 4-turn spiral is wired with Metal 6 and 5 in parallel. The cross wire has Metal 4, Metal 3, Metal 2 and Metal 1 in parallel. The dot represents contact vias between Metal 6, Metal5, Metal 4, Metal 3, Metal 2 and Metal 1.

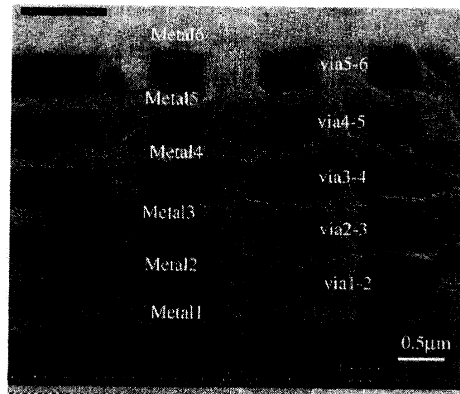

Fig. 3. The copper stack vias connect inductor wires as shown in Fig. 2.

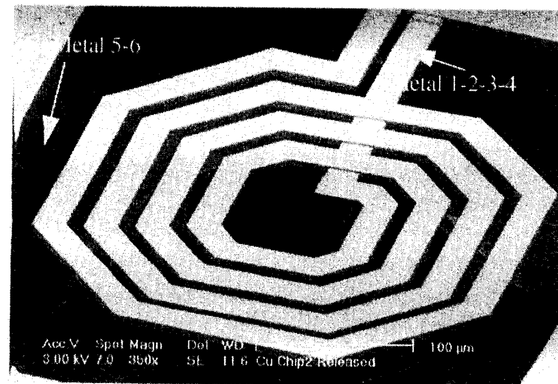

Fig. 4. SEM of an inductor after Si undercut suspended in the air.

IV. INDUCTOR CHARACTERIZATION

The inductance and Q factor of the devices were derived from 2-port S-parameter measurements. Measurements were made using ground-signal-ground (GSG) microwave probes connected to a HP8510 network analyzer from 50MHz to 20GHz. Probe calibration was done by a CS-5 calibration substrate, and the probe pads were de-embedded by making

measurements on dummy pad structures (open and short).

Measurements were made on four sizes of octagonal inductors with inductances ranging from 3.1nH to 4.4nH on two chips processed with different recipes. The first chip was processed until step (b) of the process flow in Fig. 1, with oxide removed and contained inductors N1-4. The second chip was processed completely with the oxide removed and the silicon undercut and contained inductors B1-4. Comparison of the S_{11} parameters for inductor B1 and N1 are shown in Fig. 5. The DC resistance of the two inductors is almost the same, however, the B1 inductor exhibits lower losses at higher frequencies. A comparison of the quality factor of the inductors before and after Si undercut is shown in Fig. 6. The B1 inductor has a higher quality factor above 1.5 GHz. At low frequencies, losses due to the DC resistance dominate, and the quality factor is about the same for both the inductors. The substrate losses that dominate at higher frequencies are reduced by the silicon removal.

The B1-4 inductors are modeled by the lumped parameter circuit shown in Fig. 7. C_p is the parasitic capacitance due to the return port crossover. R_{dc} is the DC resistance of the inductor. The skin effect is modeled by expressing the series resistance, R_d, of the inductor as

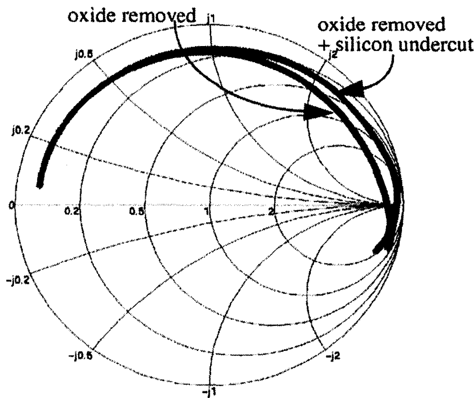

Fig. 5. Comparison of S_{11} characteristics of inductors with one oxide removed (N1) and one with oxide removed and silicon undercut (B1).

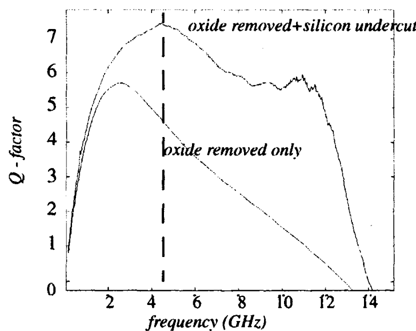

Fig. 6. Comparison of Q of inductors with the oxide removed(N1) and oxide removed and silicon undercut inductor (B1).

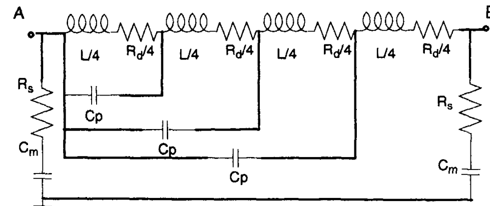

Fig. 7. Lumped parameter circuit model of the silicon and oxide released inductor.

TABLE I Summary of experimental model parameters for inductors with oxide removed and silicon undercut (B1-4).

Model Parameter	B1	B2	B3	B4
L(nH) (Calculation[11])	3.0	3.5	4.0	4.5
L (nH)	2.82	3.60	3.87	4.41
C_p (fF)	36.5	37.5	41.0	47.0
$R_{dc}(\Omega)$	2.53	3.33	3.53	4.23
R_s (Ω)	1500	2100	2300	2900
f_{crit} (GHz)	4.1	4.1	4.1	4.1
C_m (fF))	3.0	3.3	3.3	3.6
Q_{max}	7.5	7.25	7.3	7.0
f @ Q_{max} (GHz)	4.4	5.0	5.4	5.2
f_{res}(GHz)	13.9	12.0	11.3	10.9

TABLE II Comparison of inductors with oxide removed(N1-4) and with oxide removed plus silicon undercut(B1-4)

	Oxide + Silicon removal				Oxide removal only			
Parameter	B1	B2	B3	B4	N1	N2	N3	N4
L_m (nH)	2.82	3.60	3.87	4.41	3.05	3.97	4.27	4.9
Q_{max}	7.5	7.25	7.3	7.0	5.5	5.7	5.4	5.1
f@Q_{max} (GHz)	4.4	5.0	5.4	5.2	2.6	2.5	2.5	2.4
f_{res}(GHz)	13.9	12.0	11.3	10.9	13.5	12.3	12.0	10.5
Area ($x10^{-8} m^2$)	9.6	10.5	10.5	11.6	9.6	10.5	10.5	11.6

$$R_d = R_{dc} e^{\sqrt{\frac{f}{f_{crit}}}} \quad (1)$$

R_d and C_m model the frequency dependent losses. This simplified model holds up to 10GHz, the intended range of operation relevant to circuit designers. The value of f_{crit}, the frequency beyond which skin effect begins to dominates is the same for all inductors and is dependent on the thickness of the inductor metal.

Table I summarizes the measured performance of the four undercut inductors with circuit model parameters fit to experimental data. The inductance of the structure was calculated using FastHenry[11]. A comparison of the circuit model to measurement results is shown in Fig. 8. Comparison of inductors N1-4 and B1-4 to highlight the effect of silicon removal is shown in Table II. There are no significant differences in the self resonance frequencies of the two types of inductors. The inductance values after removal of the silicon are lowered by about 10%.

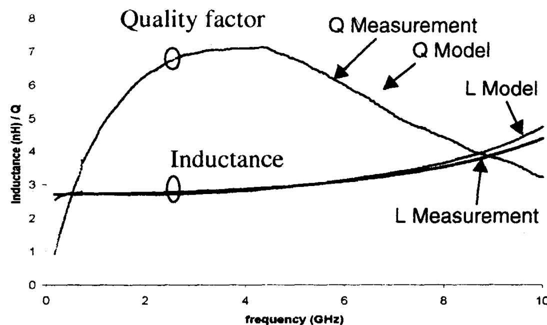

Fig. 8. Comparison of Q factor and inductance from model to measurement for inductor B1.

V. Reliability of Suspended Structures

For application of this technology in commercial devices the reliability of the suspended inductors after release was verified. The entire die was covered by metal-6 (the top-most metal layer) to protect the circuit from the post-CMOS process. The removal of the cover glass exposed the top metal to the environment. This is a concern for long term reliability due to possible environmental corrosion. Without any passivation layer after post-CMOS micromachining, the released chip was placed in an environmental chamber at 70°C, with 90% humidity for 24 hours. No significant metal corrosion was observed. The chips were wire bonded using the same equipment and settings as chips with aluminum metalization.

VI. Discussion

Thicker top metal layers have limited usefulness at higher frequencies due to skin depth limitations. Use of thinner parallel conductors available in modern CMOS process might be more advantageous and can be fully exploited if substrate losses are eliminated. Electromagnetic field simulations show that closed loops around inductors reduce the Q of inductors by a factor of 40~50% at higher frequencies. The use of a metal-6 cover as an etch mask to protect circuits induces losses that severely reduce the Q factor at higher frequencies. Slotting of the metal 6 cover is an easy solution to this problem and has been implemented in the next design iteration. Self-resonant frequency of the inductor is limited by the crossover parasitic capacitance of the return port. Trends towards low-K inter-metal dielectric will increase self-resonant frequency.

VII. Conclusion

A maskless post-CMOS micromachining technique for fabrication of higher frequency RF applications has been developed. This technology can also be applied to minimize RF crosstalk through the conductive silicon substrate[2]. Monolithically integrated IC inductors in aluminum interconnect CMOS devices have been reported with maximum Q factors of about 10 after using thick top metal layers. The quality factor degradation due to substrate losses at higher frequency make it difficult to extend the operating frequency to beyond 4 GHz. A combination of a multilevel copper interconnect for lower DC resistance and the maskless micromachining technology can deliver higher Q factors at higher frequencies. Simulations indicate that Q factors can be increased to about 20 at 10GHz with optimized layout in the CMOS process used in the present work.

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References

[1] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins and Y. K. Kwark, "Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low loss substrates," *IEEE Transaction on Microwave theory and techniques*, Vol. 45, No. 10, October 1997, pp.1961-1968.

[2] K Ng, N. Pham, L. Sarro, B. Rejaei, J. Burghartz "Characterization of a Bulk-Micromachined Post-Process Module for Silicon RF Technology" 2000 Topical Meetings on Silicon Monolithic Integrated Circuits in RF Systems. pp 99-102 April 2000

[3] J. Y. C. Chang, A. A. Abidi, and M.Gaitan, "Large suspended inductors on silicon and their use in a 2 μm CMOS RF amplifier," *IEEE Electron Device Letters*, Vol. 14, No. 5, May 1993, pp.246-248.

[4] G. K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F.Gulliou, M.S.-C. Lu, L.R.Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process," *Sensors and Actuators*, A57, pp.103-110 (1996).

[5] US Patent 5717631, "Microelectromechanical structure and process of making same".

[6] United Microelectronics Corporation. http://www.umcgroup.com

[7] H. Lakdawala and G.K. Fedder, "Analysis of Temperature-Dependent Residual Stress Gradients in CMOS Micromachined Structures", Transducers 99, Sendai Japan

[8] CRC Handbook of Chemistry and Physics, 77th Edition 1996-1999

[9] X. Zhu, D. W. Greve, R. Lawton, N. Presser, G.K. Fedder, "Factorial experiment on CMOS-MEMS RIE post processing", in Proc. of the 194th Electrochemical Society Meeting, Symposium on Microstructure and microfabricated system, Boston, MA, Nov. 1-6th, 1998, pp.41-44.

[10] X. Zhu, D. W. Greve, G.K. Fedder, "Characterization of silicon isotropic etch by inductively coupled plasma etch in post-CMOS processing", in Proc. of MEMS200, Miyazaki, Japan, 2000.

[11] FastHenry User Manual, software available for download at ftp://rle vlsi.mit.edu/pub/fasthenry/