Laminated, Sacrificial-Poly MEMS Technology in Standard CMOS

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SUMMARY

We present a micro-machining technology which enables MEMS fabrication on standard CMOS with very dense electrical / mechanical integration. Micro-mechanical structures are fabricated alongside circuits on standard 0.5μm and 0.8μm 3-metal CMOS dice using three maskless dry-etch steps. The resulting laminated beams are made of CMOS metal and dielectric layers. Such multi-conductor mechanical structures can carry multiple signals for actuation and sensing. Small gaps facilitate XYZ electrostatic actuation and fine capacitive position sensing. Experiments show that mechanical structures can be integrated 5μm away from circuits, resulting in very low parasitics and better system performance, as well as small die size.

Keywords: *MEMS; Surface micromachining; Polysilicon; CMOS compatibility; Stability.*

MICROMACHINING TECHNOLOGY

The MEMS fabrication technology consists of 3 reactive ion etch (RIE) steps performed after standard CMOS fabrication. This technology has evolved from [1] by substituting the original silicon etch with a sacrificial polysilicon etch for release. The recipe developed for a Plasma-Therm 790 reactor is given in Table 1 for dice fabricated in the HP 3-metal 1-poly 0.5μm N-well CMOS process through MOSIS. The process flow is shown in Fig. 1.

The first two CHF_3/O_2 RIE steps etch anisotropically through the exposed dielectric (SiO and SiN). The top metal layer acts as etch-resistant mask to define mechanical structures. Dielectric-to-metal etch selectivity is 8:1. The first etch step removes passivation and reaches the top metal. For the second etch step, pressure is lowered to etch through high aspect ratio trenches (i.e. narrow lateral gaps). Because of CMOS manufacturing tolerances, the duration of step #2 is adjusted to stop the etch in the 0.3μm-thick polysilicon layer or just below it. Finally, an SF_6/O_2 isotropic RIE step etches the exposed polysilicon to release suspended structures. No lithography operation is needed.

Table 1: MEMS post-process reactive ion etch steps.

	Oxide etch 1	Oxide etch 2	Poly etch
Gas flow [sccm]	13.5 CHF_3 4.5 O_2	13.5 CHF_3 4.5 O_2	50 SF_6 2.5 O_2
Pressure [mT]	60	40	100
Power [W]	55	50	60
Etch rate [Å/min]	145	112	
Time [min]	120	150	45

The CMOS metal and dielectric layers form a laminated mechanical material, as shown on Figs. 2 and 3. Seven different laminates can be fabricated in a 3-metal process. Each conducting layer is approximately 0.4μm thick (note that the SEM of Fig. 2 was taken at an angle, so its vertical

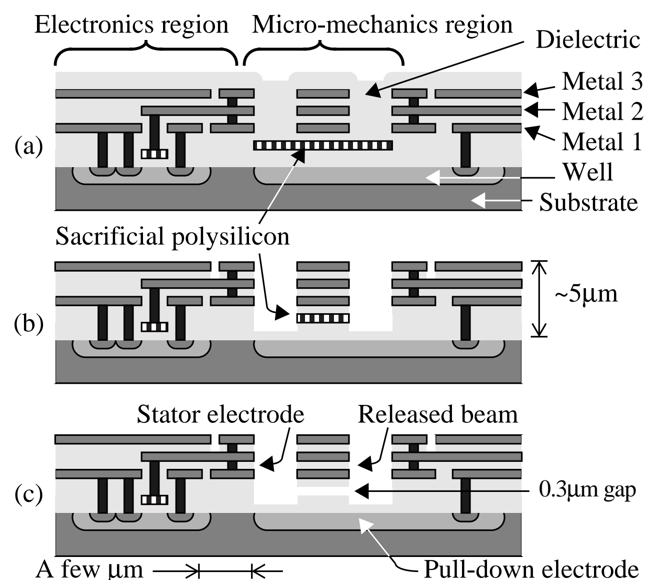


Fig. 1: Cross section of MEMS die during process flow. (a) After CMOS fabrication. (b) After oxide etch 1 & 2. (c) After polysilicon etch.

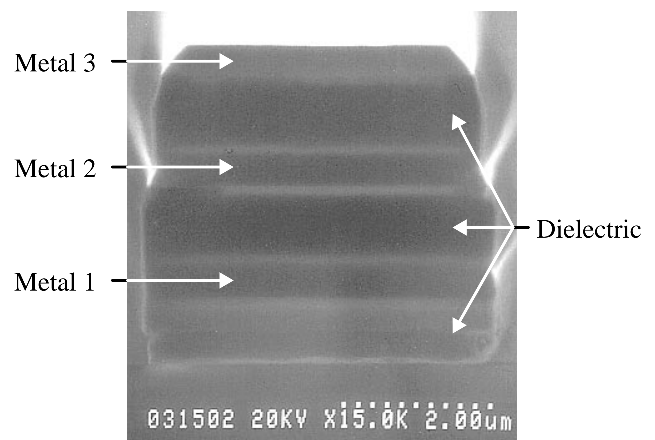


Fig. 2: SEM cross section of a released 3-metal beam.

and horizontal scales are slightly different). About half of the top metal layer is milled off during the RIE steps. The metal and dielectric deposition, etching and alignment tolerances which occur during CMOS fabrication affect the cross section of mechanical structures and induce both inter-die and intra-die performance variations.

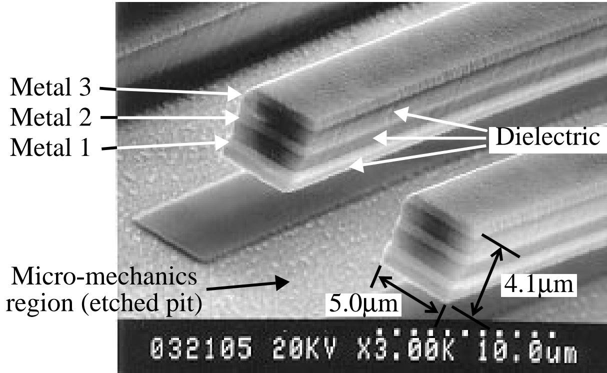


Fig. 3: SEM of two released 3-metal laminated beams.

A 1.2µm lateral gap is required between structures to release 1.2µm- to 5µm-wide beams. Beams up to 15µm wide can be released given a wider gap. Electrostatic actuation and position sensing are widely used with this technology. Narrow lateral gaps result in high force and high sensitivity for in-plane motion. Likewise, an N-well located under a mechanical structure provides a narrow-gap electrode for off-plane motion.

MECHANICAL CHARACTERISTICS

The main mechanical characteristics have been computed for equivalent homogeneous beam cross sections. Table 2 gives the effective density and elasticity for 3-metal beams. Other laminates have comparable characteristics. The laminate density is derived from the beam cross section shown on Fig. 2 and the bulk densities of Al and SiO_2. Young's modulus is derived from the measured resonant frequency of cantilever beams. Density and elasticity match very well within a die and from die to die, as indicated in Table 2 by the very low mismatch of resonant frequency measured among identically-designed cantilever beams.

Table 2: Mechanical characteristics of 3-metal beams.

	Nominal value	Standard deviation	
		Intra-die	Inter-die
Estimated density	2760 kg/m^3	*see data below for combined variance*	
Young's modulus	67.7 GPa		
Resonant frequency	n/a	0.4%	1.4%

The CMOS metal and dielectric films which make laminated structures have different coefficients of thermal expansion. The resulting vertical stress gradients cause cantilever beams to curl up after release [2]. Each laminates has a different stress and radius of curvature. Table 3 gives the radius of curvature measured on 9µm-wide beams for each laminate. The 3-metal laminate and the metal-1/metal-2 laminate have the highest radius of curvature (i.e. they are the flatest). They also have the largest relative mismatch. In general, matching is poor from die to die, but it is fair within a die.

Table 3: Radius of curvature of 9µm-wide beams for all laminates.

Laminate type	Nominal value	Standard deviation	
		Intra-die	Inter-die
Metal 1	0.27 mm	0.9%	4.5%
Metal 2	1.3 mm	10%	16%
Metal 3	2.1 mm	1.3%	6.7%
Metal 1 + Metal 2	5.8 mm	20%	68%
Metal 1 + Metal 3	3.4 mm	4.8%	21%
Metal 2 + Metal 3	2.3 mm	2.9%	18%
M1 + M2 + M3	7.7 mm	21%	57%

Table 4 gives the radius of curvature measured on 3-metal beams of various widths. Results indicate a significant edge effect to the vertical stress gradient of 3-metal beams.

Table 4: Radius of curvature of 3-metal laminated beams for various widths.

Beam width	Nominal value	Standard deviation	
		Intra-die	Inter-die
2.1 µm	3.8 mm	1.8%	18%
3.0 µm	4.2 mm	4.3%	23%
4.5 µm	4.5 mm	7.3%	26%
6.0 µm	5.2 mm	9%	34%
9.0 µm	7.7 mm	21%	57%
12.0 µm	8.6 mm	12%	39%

Each radius of curvature result presented above is derived from the measured curl of a set of 5 similar beams replicated on 5 dices. All beams are 250µm long, and curl was measured with an optical microscope. Measurement uncertainty is not included in Tables 3 and 4. For most laminate/width combination, it is less than half of the intra-die standard deviation. It is not significant compared to inter-die standard deviation results.

Table 5: Integrity of 3-metal laminated beams.

	After CMOS process	After MEMS process	After MEMS process and...		
			70°C, 90%RH 150 hrs	200°C 150 hrs	1 billion cycles
I_{lk} @ 50V	< 5pA	10 to 200pA	200pA	15pA	< 5pA change
f_0	n/a	nominal	-1.3%	-0.1%	-1.3%

To check the long-term integrity of mechanical structures, we have monitored over time the dielectric leakage current (I_{lk}) at 50 volts between the conductors of 3-metal cantilever beams, and the resonant frequency f_0 of various beams (see Table 5). Current leakage appears to be induced by humidity, but remains very low after accelerated aging. Resonant frequencies do not vary significantly. Both metrics are unchanged after 10^9 mechanical cycles (the applied stress was 10% of the yield strength of Al). Overall, we saw no evidence of delamination or breakdown.

ELECTRICAL CHARACTERISTICS

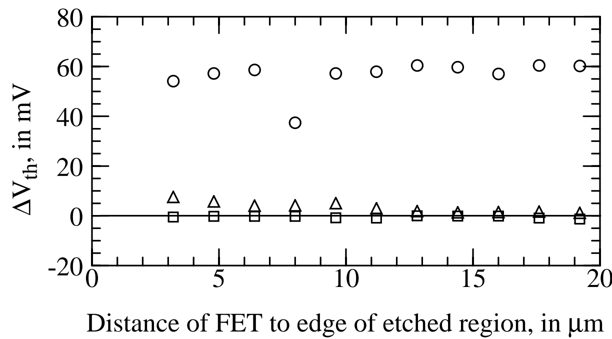
Mechanical structures can be fabricated in close proximity to MOSFETs without degrading them. Table 6 gives the main static characteristics of N-channel FETs (W=4μm and L=1.1μm) arrayed between 4μm and 20μm from a micro-mechanical region: $\beta=\mu_n \cdot C_{ox} \cdot W/L$ is the transconductance factor, S is the subthreshold slope, V_{th} is the threshold voltage, V_{off} is the offset voltage of a differential amplifier. In addition, table 6 gives the propagation delay t_d of a minimum-size inverter, measured from a 101-stage ring oscillator laid out 5μm from an etched region.

Table 6: Static and dynamic MOSFET characteristics.

	Nominal CMOS value	After MEMS fabrication	After MEMS fab and 200°C 250 hrs	After MEMS fab and 70°/ 90%RH 250 hrs
β	160 $\mu A/V^2$	+1 %	< 0.5 %	-2% to +2%
S	96 mV/dec	< 1 %	< 1 %	0 to 15%
V_{th}	670 mV	-1 mV	+4 mV	0 to -60mV
V_{off}	σ=5.7 mV	σ=5.8 mV	σ=6.5 mV	σ=9.3 mV
t_d	180 ps	+1.7%	+1.6%	+0.2%

The results of Table 6 show that FETs are not degraded by MEMS processing. For example, Fig. 4 shows the typical threshold voltage change for an array of MOSFETs located near a micro-mechanics region: ΔV_{th} is typically within ±2mV after MEMS fabrication.

Likewise, Table 6 shows that FETs are not significantly affected by 250 hours of temperature-accelerated aging at 200°C after MEMS fabrication. Fig. 6 shows that, on a typical die, ΔV_{th} increases more towards the edge the etched region. The same trend is seen for changes in transconductance factor and subthreshold slope.



Distance of FET to edge of etched region, in μm

Fig. 4: Change of MOSFET threshold voltage as a function of FET distance from micro-mechanics region:
□ after MEMS fabrication (typical die);
△ after 250 hours at 200°C (typical die; same die as □);
○ after 250 hours at 70°C / 90% RH (worst case die).

Table 6 shows that humidity exposure (250 hours at 70°C and 90% relative humidity) after MEMS fabrication causes a significant shift of threshold voltage and subthreshold slope. The threshold voltage of FETs from the worst-case die tested during our experiments is shown on Fig. 4. Except for one device, the V_{th} shift is similar for all FETs in the array. Therefore, V_{th} matching is better than absolute V_{th} variations, and the offset voltage V_{off} of a differential circuit (a more important metric than V_{th} for circuit design) degrades by only 2.5mV. Overall, circuits operate reliably under all tested conditions, as close as 3μm to 5μm from an etched micro-mechanics region.

APPLICATIONS

The fabrication technology presented above is used to implement an array of actuators for a data storage application because it allows efficient X and Z actuation, on-chip signal processing, low-noise position sensing, and good mechanical / electrical integration.

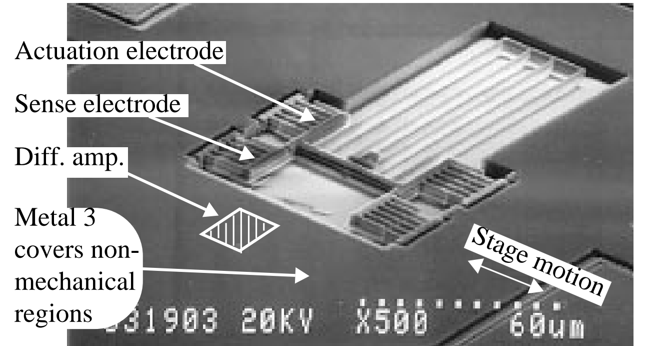


Fig. 5: SEM of 1D test stage with on-chip amplifier.

A 1D test stage is shown in Fig. 5. The readout amplifier is laid out 15μm from the etched region to minimize parasitics. By comparison, some CMOS MEMS processes require over 150μm clearance [3-4]. Extra clearance increases the die size and lengthens wiring, which adds parasitics that can strongly limit system performance, such as the signal-to-noise ratio in capacitive position sensors.

In addition, the stage shown above uses multi-conductor beams to carry three different signals for actuation and position sensing. Two out-of-phase signals drive differentially two capacitive position sensors connected as a half-bridge with the high-impedance node on the stator side. In this con-

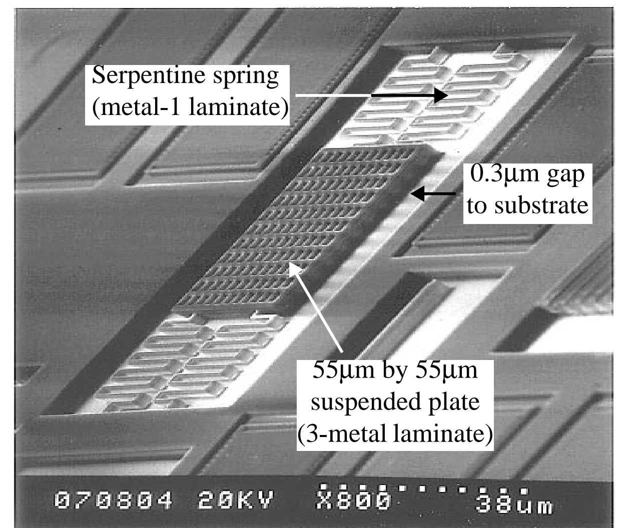


Fig. 6: SEM of a suspended plate with narrow Z gap.

figuration, the sensitive node is directly on the substrate, and parasitics are lower than if the high-impedance signal was returned through the mechanical structure. The same wiring scheme can be used to implement a low-parasitics fully-differential position sensor. Multi-conductor beams can also be used to carry multiple signals to or from a payload (such as a read/write head for data storage systems) or to design nested actuator structures.

The sacrificial-poly process also provides electrodes with a narrow gap to the substrate, and therefore lends itself to the design of sensitive Z accelerometers. The physical gap between a movable structure and the underlying substrate (or N-well electrode) is equal to the thickness of the sacrificial polysilicon etched during release, *i.e.* about 0.3µm. Including the oxide present above and below the mechanical gap, the electrical distance between the metal-1 layer of a movable electrode and the substrate (or N-well) is equivalent to an air gap of approximately 0.45µm, or a capacitance of $20aF/\mu m^2$.
For example, the 55µm x 55µm suspended plate shown in Fig. 6 has a 50fF capacitance to the underlying substrate at rest. As a motion sensor, it has a sensitivity of 0.1fF/nm. Coupled with on-chip electronics and low-parasitics wiring, such a device can achieve a competitive resolution with a small die size.

CONCLUSIONS

We have presented a new MEMS technology which achieves very dense electrical / mechanical integration in standard CMOS. We have presented the main mechanical and electrical characteristics of structures fabricated in this technology. This process is used to develop high-performance, low-cost MEMS for data storage applications. It can also be employed to implement sensitive off-plane accelerometers.

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