FACTORIAL EXPERIMENT ON CMOS-MEMS RIE POST PROCESSING

[†]X. Zhu, [†]D. W. Greve, ^{*}R. Lawton, ^{*}N. Presser, [†]G.K. Fedder [†]Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA 15213-3890
^{*}Jet Propulsion Laboratory,4800 Oak Grove Drive, Pasadena CA 91109-8099 ^{*}Aerospace Corp. POB 92957, Los Angeles CA. 90009

ABSTRACT

CMOS-MEMS is a promising approach to achieve integration of microelectromechanical structures with circuits by using foundry CMOS services coupled with post-CMOS processing. The most significant benefit is the low cost of manufacturing the mechanical structures with CMOS. We report suitable conditions for post-CMOS processing by reactive ion etching (RIE) to define the mechanical structures. Values of power, pressure and gas flows are determined which achieve acceptable mechanical integrity, electrical continuity, etch rate and selectivities of the metal etch mask over the CMOS dielectric materials. Results are presented from a Box-Behnken factorial experiment to achieve these goals.

INTRODUCTION

Our approach to the goal of low-cost monolithic integration of circuits with microelectromechanical systems (MEMS) is to fabricate microstructures directly out of the interconnect layers in a conventional CMOS process. Such a process utilizes only maskless post-CMOS fabrication steps. The top metal layer in the CMOS process is used as an etch mask during RIE to release microstructures[1] as illustrated in Fig. 1 (a). As shown in Fig. 1 (b) and (c), the etch is divided into 2 steps: CHF_3/O_2 anisotropic etch of dielectric layers to define the structures; SF_6/O_2 isotropic etch of silicon to release the structures. Composite mechanical structures can include one polysilicon layer, three metal layers and the inter-metal dielectric layers. The dry etch release steps avoid sticking problems usually associated with the wet etch processing. About 5:1 high-aspect-ratio of beams can be achieved in this process.

In this paper, our concentration is on the isotropic etching of interconnect dielectric layers. There are some dramatic differences in using RIE of dielectrics in CMOS micromachining when compared with integrated-circuit (IC) processing[2][3]. First, for definition of microstructures, it is preferred to have no selectivity in the vertical etch direction between silicon dioxide, silicon nitride and Si, since the structure etch must go through a stack of various dielectric layers. However, the selectivity between these materials and the metal mask layer, specifically aluminum, should be kept high. Second, ion milling during RIE is significant because of the extremely long etch of the dielectric layers. This milling of the metal layer can cause loss of device dimension and electrical connection failure. As in IC processing, the directivity of etching is achieved in part by control of passivation on the sidewall[4]. Too much polymerization on the surface will slow down the etching and limit the smallest spacing that can be achieved; too little polymerization will not provide protection on the sidewall, causing the loss of critical dimension. Third, electrical connection failures can result from the etch, mostly at vias connecting different metal layers. Failures are caused by two mechanisms as shown in Fig. 2: one is the removal of metal layer inside the vias which results in an open circuit at the sidewall of the vias; the second is lateral etching of refractory metal layers which exist above and below each aluminum layer in the submicron CMOS process.

THEORY

Complexity of RIE system

It is well known that plasma systems have a lot of processing variables, such as gas mixture, gas flow rate, pressure, RF power, electrode spacing, electrode temperature, electrode material, total wafer area(loading) and previous processing steps. All these variables affect the requirements mentioned above and their influence is non-linear and correlated. Up to now there is no suitable model to completely describe the process for the post-CMOS micromachining. The construction of a mathematical model which quantitatively represents the process responses as functions of the process variables is highly desirable, and permits the identification of the optimized settings to satisfy all the different requirements.

The problem of RIE etch of microstructures is illustrated in Fig. 3. Multiple effects of RIE need to be optimized at the same time. Important effects include etch rate, loss of critical dimension, survival of electrical connection and generation of polymers (on the side-wall and in the field). Sometimes the requirements conflict with each other. For example, to increase etch rate, we need to reduce the generation of passivation, but this will cause loss of mechanical structure dimension and electrical connection failure. To ease our task, we chose three processing variables (pressure, power and mixture of gases) as experimental factors in a Box-Behnken factorial experiment[2][5] to generate different response surfaces. After a series of screening experiments, we chose a CHF₃/O₂ mixture instead of the CF₄/O₂ mixture used previously[1] as it can generate sufficient passivation with a reasonable etch rate and less failure of electrical connection. The etching profile can be evaluated by measuring the top metal layer thickness and line width after dioxide etching as shown in Fig. 4.

The starting point for the three processing factors was obtained from the manufacturer's recommended recipe and our former work[1]. The space for conducting factorial experiments was determined by another set of screening experiments

Response Surface Methodology

The benefit of Response Surface Methodology, a statistical technique, is that the experimental strategy and data analysis are combined efficiently to generate a parametric model that represents the process response. After the response has been quantitatively

modeled, graphical representation of the response surface can be generated in the parametric space. The trends in individual responses from changes in the processing factors can be predicted, and from multiple response surfaces of each processing factor, an acceptable range can be obtained.

The only constraint in this method is that the response must be represented as a continuous variable, that is either the original data is a continuous variable or can be converted to a continuous variable. Etch rate and beam width are obvious continuous data. However, polymerization and electrical continuity are non-continuous variables which are hard to set criteria for the response surface analysis. For polymerization, we have to use a rough quantitative measurement, where values are fit into 3 categories: 1 for heavily polymerized, $0.5 \sim 0.75$ for the medium case and 0 for no polymerization. The electrical connection, determined by the resistance of vias connecting different layers are either conducting with a contact resistance of about 7-16 Ω by 2-wire measurement, or open, indicated by infinite resistance. In order to convert this to a continuous variable, an open-circuit is approximated as a 1M Ω value of resistance. This value is large enough to establish the parametric model.

The effect of experimental error on the validity of a parametric model can be assessed using statistical analysis. First, the experimental error can be estimated by repeating experimental runs and calculating the standard deviation of the replicate differences. Also, the lack-of-model-fit can be estimated by performing extra trials to calculating the deviation between the model and the experimental data.

Response Surface Design

In general, a response surface design should be chosen that will support at least a full quadratic model. Three levels of the various factors are needed for a quadratic model. The general form of the full quadratic model, which includes a constant term, *n* linear term, n(n-1)/2 two-factor interaction terms, and n(n-1)/2 quadratic terms for curvature, is:

$$Y = b_0 + \sum_{i=1}^n b_i X_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^n b_{ij} X_i X_j + \sum_{i=1}^n b_{ii} X_i^2$$
(1)

where Y is the process response and the X_i are the process variables. The three levels of X_i should be equally spaced on same scale (e.g., linear, log, or square root). Thus for 3 factors, 10 coefficients must be determined, since Eq. (1) can be simplified to:

$$Y = b_0 + b_1 X_1 + b_2 X_2 + b_3 X_3 + b_{12} X_1 X_2 + b_{13} X_1 X_3 + b_{23} X_2 X_3 + b_{11} X_1^2 + b_{22} X_2^2 + b_{33} X_3^2$$
(2)

Following common practice, we add 5 extra trials to estimate residual error. A large number of data points gives better error estimation and model fitting; however, this will lead more consumption of time and effort.

In our research, we chose a Box-Behnken design[2][5] as shown in Fig. 5 with

15 trials for 3-factor 3-level experiments with 12 points on the each edge of the experimental space cube and 2 replicates at the center. The 3 levels of factors (power, pressure and O_2 flow rate) are shown in Table 1. Comparing to full-factorial design, 12 runs are saved out of 27 runs.

Factor	low-level (-)	mid-level (0)	high-level(+)
X1=Pressure (mTorr)	40	110	180
X2=Power (Watt)	50	100	150
$X3 = O_2$ flow (sccm)	2.5	12.5	22.5

Table 1: 3 Levels of 3 Factors

EXPERIMENTAL RESULTS

The measured data from the factorial experiment is given in Table 2, where +/- and O correspond to the 3-level settings of pressure, power and O_2 flow rate in Table 1. Fig. 5 illustrates how the etch rate, electrical connection and polymerization varies with power, gas mixture and pressure. Etch rate is increased with increasing RF power and chamber pressure; it is not significantly affected by O_2 concentration. Increasing RF power and decreasing pressure will cause a decrease in passivation. At high power levels, ion milling causes the top metal layer to thin resulting in loss of critical dimension in the final microstructures. The ion milling can be compensated by increasing chamber pressure. The vias fail at high power and lower pressure as shown in Fig. 2.

The data generated by a response surface design is analyzed using Least Square Regression(LSR) analysis software from Minitab[®] which determines the model coefficients by minimizing the residual variances. The coefficients of Eq. (2) with each factor normalized to ± 1 and 0 levels are listed in Table 3. The significance of each factor, their interactions and their quadratic effect can be extracted from the table. For example, increasing RF power increases the etch rate, reduces the generation of polymer, especially on the sidewall, but thins the top mask layer, reduces the beam width and is prone to cause the vias failure; whereas, increase pressure will cause opposite effects. However, the interaction and quadratic coefficients also have a significant effect on the responses. The interpretation of each factor's contribution to the final responses is quite difficult without assistance of graphic plots.

Run No.	Pressure	Power	O2 flow rate	Cal Etch Rate (Å/min)	Via contact (Ω)	Top Metal layer Width (W) (µm)	Top Metal Layer Thick (T) (µm)	Polymer on Sidewall	Polymer in the field
1	+	+	0	663	16	1.800	0.582	0.00	0.5
2	+	-	0	127	16	1.680	0.625	1.00	1
3	+	0	+	373	7	1.868	0.636	0.50	1
4	-	-	0	120	12.0	1.585	0.381	0.00	0
5	0	-	+	145	7.8	1.843	0.598	0.50	0
6	-	+	0	311	100000	0.459	0.091	0.50	0
7	0	-	-	149	7.8	1.851	0.611	0.50	0
8	0	+	-	438	100000	1.171	0.372	0.50	0.5
9	+	0	-	336	8.6	1.852	0.587	0.75	1
10	0	0	0	353	11.5	1.748	0.508	0.00	0
11	-	0	+	214	12.6	1.331	0.191	0.00	0
12	0	+	+	462	100000	1.216	0.357	0.00	0
13	-	0	-	268	100000	1.150	0.309	0.00	0
14	0	0	0	375	9	1.822	0.500	0.00	0
15	0	0	0	377	9.5	1.822	0.512	0.00	0

Table 2: Box-Behnken Design for Isolation Layer Etching

Table 3: Normalized Coefficient Values for the Full Quadratic Model

	etch_rate	top metal layer	to metal layer	via contact	polymer on	polymer in the
	(A/min)	width (µm)	thekness(µm)	(32)	the side wall	neia
b ₀	367.8	1.797	0.507	1070	0.000	0.000
b ₁	70.3	0.319	0.178	-234000	0.223	0.438
b ₂	161.6	-0.295	-0.101	371000	-0.127	0.000
b ₃	-1.8	0.053	-0.008	-141000	-0.098	0.063
b ₁₂	-39.0	-0.170	-0.066	-17000	0.152	0.375
b ₁₃	-33.7	-0.246	-0.021	265000	0.222	0.000
b ₂₃	-35.6	-0.046	-0.002	233000	0.152	0.125
b ₁₁	76.0	0.308	0.062	-242000	0.371	-0.125
b ₂₂	26.9	-0.072	0.033	283000	-0.055	0.000
b ₃₃	7.5	0.033	-0.000	-8000	-0.129	-0.125

Fig. 6 shows an example of an etch rate contour plot with the change of power and pressure and constant 16 sccm O_2 flow. The etch rate increases with power and pressure; and the etch rate is more insensitive to pressure at higher pressure level. By overlapping

the contour plots generated with the upper and lower bounds of the desired responses as functions of pressure, power and O_2 concentration, a set of acceptable processing parameters are derived, as shown in Fig. 7. The central blank portion of the graph delimits the operating regime in which all criteria are met. The current processing point is at 125 mTorr chamber pressure, 0.55 W/cm², CHF₃ flow at 22.5 sccm and O_2 flow at 16 sccm. At the etch rate of 425 Å/min, it takes about 2 hrs to etch through all the dielectric layers. Previous recipes operated at a lower power level (about 0.27 W/cm²), and took around 9 hrs to complete etching.

The quality of the model can be determined by examining by the adjusted- R^2 number[5]. A perfect fit would have an adjusted- R^2 value of 100%. The adjusted- R^2 for the responses of etch rate, top metal layer width, top metal layer thickness, via contact, polymer on side-wall and polymer in the field are 97.8%, 95.3%, 97.9%, 72.5%, 85.6% and 78.4%, respectively. These values indicate that the parametric model represents this processing reasonably accurately.

CONCLUSION

The application of a Box-Behnken factorial experiment to select appropriate conditions for the RIE etching of the dielectric layer in CMOS-micromachined devices has been demonstrated. A quantitative parametric model to represent this process has been obtained. The processing region for achieving minimal lateral etch, minimal polymerization and electrical continuity of vias has been determined. The factorial experiment design and the use of overlay contour plot dramatically reduced the time and effort to optimize this very complicated processing. These results show that a systematic experimental approach is effective in process optimization.

ACKNOWLEDGMENTS

The research effort was sponsored by JPL and by DARPA under the AFOSR, Air Force Materiel Command, USAF, under cooperative agreement F30602-96-2-0304.

REFERENCES

1. G. K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F.Gulliou, M.S.-C. Lu, L.R.Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process," *Sensors and Actuators*, A57, pp.103-110. (1996).

2. S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era (1990).

3. K. Williams and R. Muller, "Etch Rates for Micromachining Processing," *Journal of Microelectrome-chanical Systems*, pp. 256, Dec (1996).

4. S. Rossnagel, J. Cuomo and W. Westwood, *Handbook of Plasma Processing Technology*, Noyes Publications (1990).

5. M.W. Jenkins, M.T. Mocella, K.D. Allen and H.H. Sawin, "The Modeling of Plasma Etching Processes Using Response Surface Methodology," *Solid State Technology*, pp.175-182, Apr. (1986).



Figure 1. Cross sections of device in each stage of process flow. (a) Device from CMOS processing. (b) After isotropic isolation layer etch. (c) After isotropic Si etch to release mechanical structure.



Figure 2. Via failure mechanism: (a)Loss of critical dimension by ion milling, (b) Lateral etch of refractory layer illustrated by FIB cross-cut of structure.



Figure 3. Multiple responses of the RIE system as a function of multiple processing variables.



Figure 4. SEM of the cross section of a CMOS-micromachined beam's profile.



High power, low pressure results in loss of critical dimension in the beam width.

The center point condition results in an adequate beam width and no polymerization with design line width =2.1 μ m.

Figure 5. The Box-Behnken 3-factor design of experiment. The etch rate, polymerization and electrical connection vary with the processing parameters.



Figure 6. The etch rate (\mathring{A}/min) contour plot as a function of power and pressure with 16 sccm of O_2 flow.



Figure 7. Overlay contour plots of etch rate, critical dimensions, electrical connectivity and polymerization with O_2 flow is held at constant 16 sccm, where \star indicates our current processing point.