Temperature Control of CMOS Micromachined Sensors

By

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Temperature Control of CMOS Micromachined Sensors

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Ph.D. Dissertation

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Abstract

An understanding of residual stress, in the various layers of the CMOS process is important for design of sensors. A simulation methodology based on experimentally extracted material properties was developed in the course of this work. The differences in stress gradient with temperature are exploited to design a novel IR imager pixel. The IR imager can achieve a NEDT of 6mK.

A methodology for the design of a temperature stabilization scheme for CMOS micromachined sensors is presented in this work. Temperature stabilization of a z-axis accelerometer, fabricated in a 0.5 μm Agilent CMOS process is demonstrated. The accelerometer motion is sensed by a vertical comb drive designed by controlling the rotor and stator curvature. The polysilicon layer of the CMOS process has been utilized for heating the device structure to a constant temperature, that is higher than the maximum ambient operating temperature. The capacitance detection circuits have temperature independent gain. The D.C. bias stability of the accelerometer improved from 1.7 G/^{o}C, to 42 mG/^{o}C, and the sensitivity stability improved from 60% to 18% over a temperature range of 70 ^{o}C after temperature control.

To my father,
Late Mohammadi N. Lakdawala

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Chapter 1. Introduction

MicroElectroMechanicalSystems (MEMS) have contributed to advances in inertial instruments and significant progress has been made over the past decades. The advantages of low-cost, low-power, small size, batch fabrication allows MEMS-based inertial sensors to have a wide range of applications in automotive, consumer, computer and navigation markets. Being a mature MEMS-based sensor application, current low-cost MEMS accelerometers have a high degree of integration, with sensing elements and electronic interface circuitry on a single chip. The ADXL series of accelerometers from Analog Devices includes a polysilicon micro-structure integrated with on-chip capacitance sense circuits and digital output [1][2]. Accelerometers and gyroscopes using the Complementary Metal Oxide Semiconductor (CMOS) micromachining technology have also been developed at Carnegie Mellon University [3][4][5][6][7]. CMOS micromachining technology has many advantages over polysilicon surface micromachining processes [8][9]. Compatibility with conventional CMOS technology enables fast, repeatable, reliable, and economical fabrication of MEMS devices integrated with conventional CMOS [10][11].

One of the concerns in designing CMOS microstructures is structural curling [12]. The multilayer structural material, composed of metal layers with interleaved dielectric layers, exhibits residual stress gradients that induce structural curling. Stress in each layer is a function of temperature due to the differences in the Temperature Coefficient of Expansion (TCE) of the layers. This variation of structural curling leads to variation of sensitivity and offset of inertial capacitive sensors, as the coupling area between adjacent electrodes changes.

1.1 Motivation

This thesis proposes a technique to reduce the temperature dependence of CMOS microsensors by integrating a micro-oven within the device structure. The polysilicon of the CMOS process is used for resistive heating of the device structure. The device is held at a constant temperature irrespective of the ambient temperature. The constant temperature is chosen

as the highest specified operating temperature of the device. This approach is preferred to electronic compensation of device performance for several reasons:

- The sensitivity variation with temperature is a function of manufacturing effects (metal oxide thickness, inter-metal misalignment). Simple correction factors are not sufficient and an expensive post-fabrication calibration cycle is required.
- Heating of devices reduces the structural curl and can improve device performance.
- No additional fabrication steps are required as the CMOS polysilicon is used both as a heater and temperature sensor. This design enhancement can be applied to any capacitive CMOS sensor as many do not utilize polysilicon for sensing.
- Device performance can be tuned by temperature control.

1.2 Previous Research

Temperature stabilization schemes are based on the premise that effects of temperature on device performance can be eliminated if the device is held at a constant temperature. One way of maintaining a constant temperature is to heat the device to a temperature greater than its maximum operating temperature. This approach is relatively low-cost as it can be implemented using resistive heaters. Heaters have been used to improve the frequency stability with temperature of devices have been used in commercial high quality quartz resonators and voltage references. In some cases the device cannot be operated at an elevated temperature and must be controlled to the nominal operating temperature using a combination of heating and cooling. Thermo-electric coolers and heaters are used for temperature control of laser diodes used for communication applications.

Temperature stabilization schemes have also been applied to micro-devices. Integrated micro-heaters to stabilize temperature of surface acoustic wave (SAW) resonators were first proposed by White et al. [13] Micro-heaters have been incorporated into film bulk acoustic resonators (FBAR) to improve the temperature performance [14]. Micro-heaters have also been integrated with silicon microprobes for thermal marking applications [15]. Researchers were able to raise the temperature of pig cortex by 50^{o}C using 6mW of power for 2 minutes. Micro-oven temperature control has also been used by researchers to stabilize resonant frequency of CMOS compatible surface micromachined resonators placed in a vacuum using less than 2mW of power [16]. Thermal applications of polysilicon microbridges have been investigated by Mastrangelo [17], to design flow sensors, pressure sensors and as incandescent light sources.

The work in this thesis demonstrates for the first time a integrated temperature control scheme that has been implemented to improve its temperature performance of an inertial sensor.

1.3 Summary

Chapter 2 covers the analysis of the residual stress gradients in CMOS micromachined devices with temperature. A simulation methodology based on the parameter extraction is presented as a tool to simulate device curl. An automatic meshing technique to simplify the meshing of CMOS micromachined devices is described. The theoretical analysis introduced in this chapter serves as a basis for the mechanical design of the infrared imager pixel, and the z-axis temperature compensated accelerometer. The lateral curl in CMOS microstructures due to temperature is exploited in the design of the IR imager pixel. The differences in residual stress gradients that cause CMOS micromachined beams to curl depending on their composition, are exploited in the design of the vertical comb drive that is based on a controlled z-offset between the rotor and the stator combs.

Chapter 3 describes a CMOS micromachined infrared (IR) sensitive pixel that senses temperature by measuring capacitance change due to lateral motion induced by differences in thermal coefficient of expansion (TCE) of two materials. The temperature-induced capacitance change is measured by an on-chip circuit with input d.c. bias feedback and double-correlated sampling. The area of the pixel sense element is 800 μm^2. Measured pixel sensitivity is 0.57 mV K with equivalent temperature noise of 6 mK/$\sqrt{Hz}$, corresponding to 0.2 aF/$\sqrt{Hz}$ of equivalent capacitance noise. An imager architecture consisting of 16 x 16 pixels has been designed and is expandable to larger arrays.

Chapter 4 describes the design and characterization of a CMOS micromachined Z-axis accelerometer based on an out-of-plane comb drive. The design procedure for the comb drive, the mechanical design and temperature independent interface circuits is explained. The accelerometer has a noise floor of less than 1 mG/$\sqrt{Hz}$. The linearity of the device is better than 3% over 20G input range. The cross axis sensitivity is 32 dB. The device performance was measured to be dependent on temperature. The device D.C offset and sensitivity were measured to be dependent on temperature. A compensation scheme that improves the temperature stability of device performance is necessary.

Chapter 5 presents a temperature compensation technique that aims to keep the temperature of the device constant using integrated polysilicon resistors of the CMOS process embedded in the

device structure. Holding only the device at a constant temperature rather than the entire chip leads to lower power consumption and reduces packaging difficulties. A Z-axis accelerometer sensitive to out-of-plane acceleration, described in Chapter 4 has been used as a test-bed for demonstration of the temperature control scheme. The D.C. offset stability of the accelerometer improved from 1.7 G/^{o}C, to 42 mG/^{o}C, and the sensitivity stability improved from 60% to 18% over a temperature ranges of 70^{o}C after temperature control.

Chapter 6 provides an approach to improve the performance of inductors fabricated in a digital logic process with copper interconnect and low-k dielectric, using the CMOS micromachining process. Removal of the underlying silicon and the inter-turn sidewall oxide helps reduce the substrate losses that dominate at higher frequencies, increase the self resonant frequency and also reduce substrate noise coupling into the inductor.

Chapter 7 provides some conclusions based on this research work for temperature stabilization of CMOS micromachined sensors. An outline of future research that aims to understand and exploit temperature effects in CMOS micromachined device is also presented.

Appendix I, summarizes technique that can dynamically measure device shape, for large displacements. The measurement set-up is implemented by modification of the MIT microvision system. The Appendix II described the details of the circuit cells that were designed to implement the capacitance interface circuits, and the design of the test board that was used to test the accelerometer.

Chapter 2. Characterization of Temperature Effects in CMOS Micromachined Structures

CMOS surface-micromachining technology through conventional CMOS processing integrates circuits with mechanical structures at low cost. It provides an ability to place multiple isolated conductors in microstructures for novel capacitive sensing. The multilayer structure material, composed of metal layers with interleaved dielectric layers, exhibits residual stress gradients that induce structural curling. Stress in each layer is a function of temperature due to the differences in the temperature coefficient of expansion (TCE) of the layers. This variation of structural curling leads to variation of sensitivity of lateral capacitive sensors, as the coupling area between adjacent electrodes changes. Curl-matching techniques have been used to minimize the effect of these variations. In order to design and verify matched curl in structures it is imperative to predict structural curl variation due to temperature using finite element analysis. Simulation of structural curl by finite element techniques requires knowledge of the material properties and residual stress in all layers of the CMOS stack. Test structures proposed in this chapter allow extraction of the TCE, and residual stresses that are need for accurate characterization of curl in CMOS micromachined structures.

The first step in the finite element analysis of CMOS micromachined structures is the creation of a multilayer mechanical mesh of the structure. The process of generating this mesh for a complicated structure can be time consuming and often a hindrance to simulations. An automatic mesh generation algorithm that can optimally mesh micromachined structure by recognizing the functionality of its constituents modules, like springs, masses, etc., was designed. The meshing rules for the various components are governed by the meshing rules described in a rules file.

This chapter describes the CMOS micromachining process used for fabrication of most of the devices described in the thesis. An analytical understanding of the stress and stress gradients in

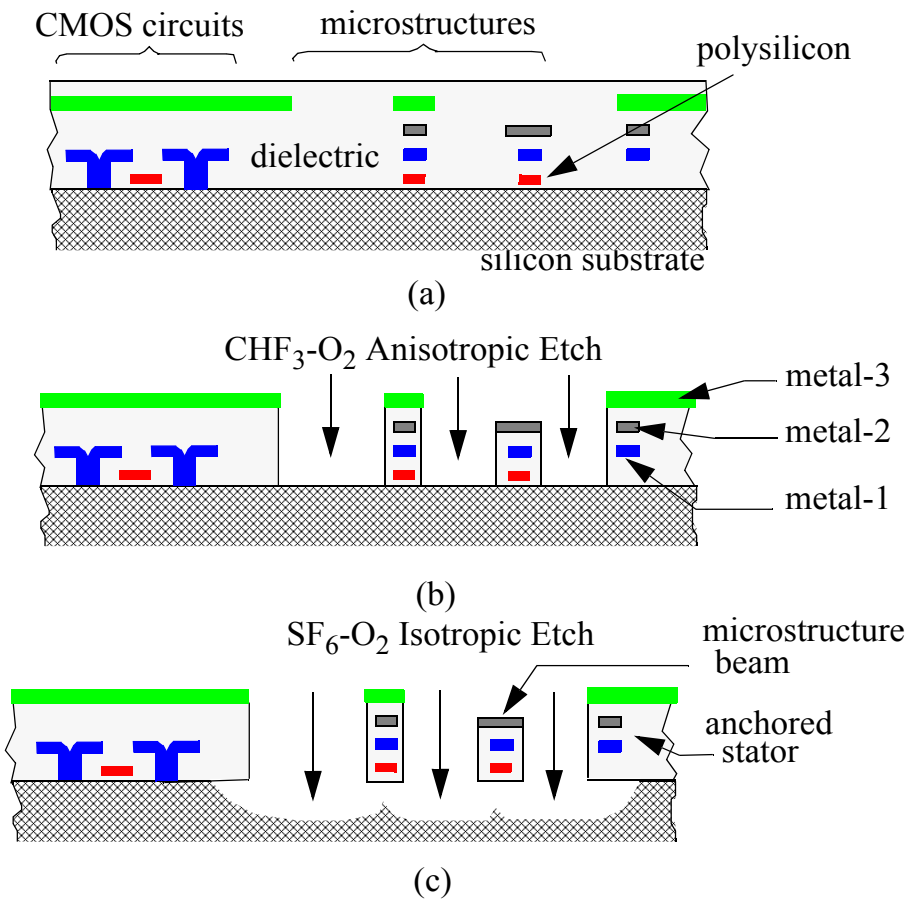


Figure 2.1 Schematic of the process for micromachined structures in standard CMOS.

CMOS micromachined devices is developed. A parameter extraction technique has been used to derive TCE values of the metal, oxide and the polysilicon layers. The expressions derived for beam bending with temperature have been used in NODAS [18] to model the mechanical effects of temperature in CMOS micromachined structures [19]. Finally, the automatic meshing technique for multilayer CMOS micromachined structures is described.

2.1 CMOS Micromachining Process

The devices described in this thesis have been fabricated in the high-aspect-ratio CMOS micromachining process developed at CMU [8]. The process flow, shown in Figure 2.1, enables fabrication of micromachined structures in a standard 0.5 μm 3-metal CMOS process. The conventional CMOS process is followed by an anisotropic reactive-ion etch (RIE) with CHF_3 and O_2 to etch away oxide not covered by any of the metal layers, resulting in high aspect ratio vertical sidewalls. An isotropic RIE (using SF_6 and O_2) then removes the underlying silicon, thus releasing the microstructure. The details of the process are described in [9][10] and [11].

2.2 Thermal Multimorph Analysis

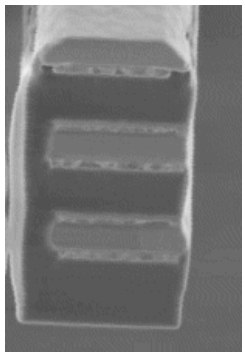
The analysis of temperature-dependent curl for CMOS micromachined beams extends Timoshenko's treatment [20][21] of thermal bimorphs for lateral and vertical directions and results in equations describing the beam tip deflection with temperature. Consider an elemental length *dx* of a multilayer beam shown in Figure 2.2. Axial forces acting at the centroid of each material causes vertical and lateral bending moments to be generated within the element. Each material, denoted by subscript *i*, has a thickness t_i, width w_i, area $A_i = w_i t_i$, coefficient of thermal expansion α_i, and an effective biaxial modulus E_i. The biaxial modulus can is expressed as

$$E_i = \frac{\bar{E}_i}{1 - \nu_i} \tag{2.1}$$

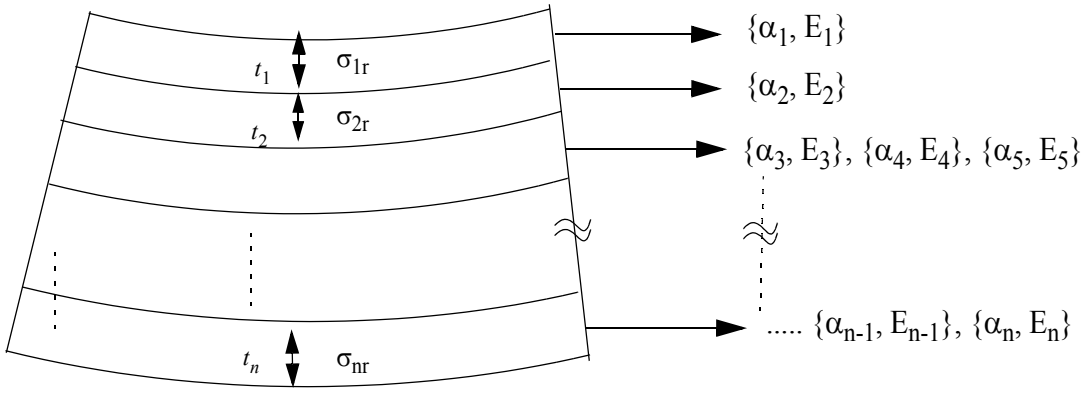
where $\bar{E}_i$ is the Young's modulus and ν_i is the Poisson ratio of the *i*-th layer. The material properties for each layer are assumed to be uniform throughout the layer and independent of temperature. Effects of anticlastic curvature along the width of the beam have been neglected. The temperature across the element is T(x). The stress gradients across the height of each material are assumed to be linear. Let σ_i and σ_{ir} be stress at the center of each layer or the average stress in each layer if a uniform stress gradient is assumed, before and after the film has been released respectively. This stress is produced in CMOS metal layers due to the fabrication process. The deposition conditions and methods for the various metal and oxide layers are different. The field oxide is grown by thermal oxidation, the inter-metal dielectric (oxide) is deposited by low temperature methods. The metal (aluminum for Agilent 0.5 μm process) is deposited by sputtering. Since the access to these layers during the fabrication is only available at the CMOS foundry, the extraction of the material properties poses a challenge for the foundry users.

The bending moment in the beam can be expressed in terms of the layer stresses. Let z_{ci} represent the moment arm of the axial force measured from the neutral axis of the element. Let M_{yi} represent the moment about the y-axis in the *i*-th layer produced by the interfacial forces. Since the element is in equilibrium and no external bending moment acts on the beam,

$$\sum_{i=1}^{n} A_i \sigma_{ir} = 0 \tag{2.2}$$



(a)



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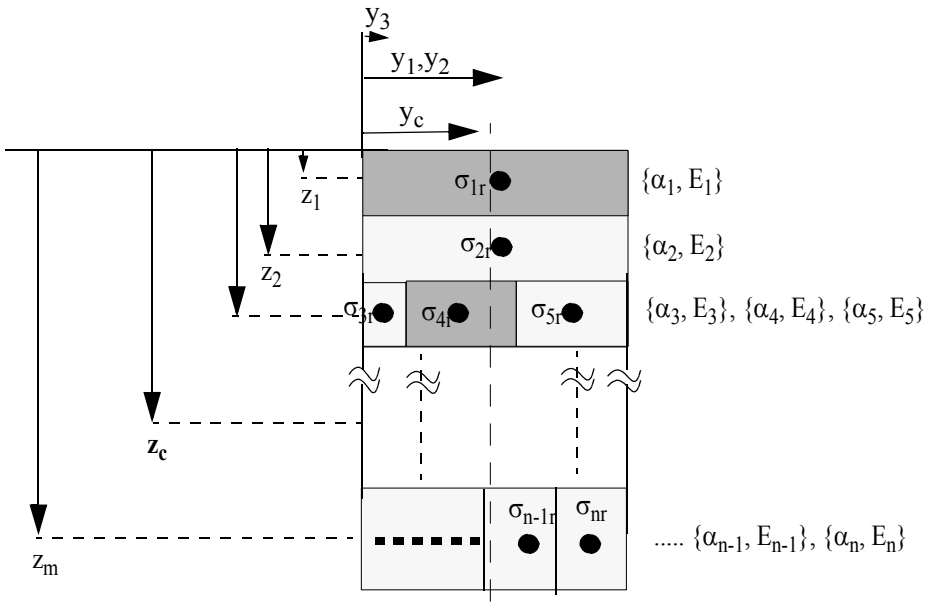


(c)

Figure 2.2 (a) Cross section of a typical CMOS micromachined beam (b) Model of a CMOS cantilever beam composed of metal, dielectric and polysilicon layers. (c) Cross-section of an asymmetric multi-layer beam with dots representing the axial forces acting out of plane. Since the forces are asymmetrically located, there is a resultant lateral bending moment in addition to the vertical bending moment.

$$\sum_{i=1}^{n} M_{yi} - \sum_{i=1}^{n} A_i z_{ci} \sigma_{ir} = 0 \tag{2.3}$$

For this case, the distance of the centroid of each layer to the neutral axis, z_{ci} can be computed as

$$z_{ic} = z_i - z_c \tag{2.4}$$

$$z_c = \frac{\sum_{i=1}^{n} z_i E_i A_i}{\sum_{i=1}^{n} E_i A_i} \tag{2.5}$$

where z_c is the location of the centroid of the element relative to the top of the beam. For small deflections assuming Bernoulli beam theory, the bending moment generated within each material can be written as

$$M_{yi} = E_i I_{yi} \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} \tag{2.6}$$

where $I_{yi} = \frac{1}{12} w_i t_i^3$ is the moment of inertia of the i-th material, assuming a rectangular cross-section taken about the principal axis of the layer parallel to the y-axis. The moment of inertia for the i-th material about the neutral axis of the element can be calculated using the parallel axis theorem as

$$I_{yic} = I_{yi} + z_{ic}^2 A_i \tag{2.7}$$

The bending moment of the entire beam is computed by summing the bending moments of each material, and from (2.3)

$$M_y = \sum_{i=1}^{n} E_i I_{yic} \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} = \sum_{i=1}^{n} M_{yi} + \sum_{i=1}^{n} z_{ic}^2 E_i A_i \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} \tag{2.8}$$

$$M_y = \sum_{i=1}^{n} z_{ci} A_i \sigma_{ir} + \sum_{i=1}^{n} z_{ic}^2 E_i A_i \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} \tag{2.9}$$

Cantilever beams fabricated in the CMOS micromachined process possess an out-of-plane deflection at room temperature. The radius of curvature of each type of beam at room temperature

is different. To describe the initial curl at room temperature, we introduce the concept of a characteristic temperature. Let T_0 be a characteristic temperature defined such that at this temperature, all the materials have no relative extension and the beam is flat. This temperature can be experimentally observed and provides a intuitive way of characterizing curl. When the beam is flat there is no internal bending moment, and the stresses in the various layers produce only axial strain. As the beam is heated or cooled from this temperature the thermal stresses in the layers produce a non-zero bending moment that causes the beam to curl. For an unreleased beam, the bending moment produced due to residual stress of the layers is cancelled by the support structure. During the release process the substrate is removed and the stress in the beam is released resulting in common strain in all the layers, a strain gradient that cancels the internal-bending moment. The released residual stress of the i-th layer at temperature, T, for small deflections can be expressed as

$$\sigma_{ir} = \sigma_{iro} + \alpha_i E_i (T - T_0) - E_i z_{ic} \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} \tag{2.10}$$

where σ_{iro} is the released stress in the layer at temperature T_o. The second term in the R.H.S of (2.10) is the stress produced due to thermal expansion in the layer, and the last term corresponds to the stress gradient due to the curl in the element. Multiplying throughout by $z_{ic}A_i$,

$$z_{ic}A_i\sigma_{ir} - z_{ic}A_i\sigma_{iro} = \alpha_i A_i z_{ic} E_i (T - T_0) - E_i A_i z_{ic}^2 \frac{\mathrm{d}^2 z}{\mathrm{d}x^2} \tag{2.11}$$

$$\sum_{i=1}^{n} z_{ic}A_i\sigma_{ir} - \sum_{i=1}^{n} z_{ic}A_i\sigma_{iro} = \sum_{i=1}^{n} \alpha_i A_i z_{ic} E_i (T - T_0) - \frac{\mathrm{d}^2 z}{\mathrm{d}x^2}\left(\sum_{i=1}^{n} E_i A_i z_{ic}^2\right) \tag{2.12}$$

The second term in the L.H.S. of (2.11) is the total bending moment produced, which is reduced to zero, when the element has no curl at the characteristic temperature. The total internal bending moment can then be written from (2.9) as,

$$M_y = \sum_{i=1}^{n} \alpha_i A_i z_{ic} E_i (T - T_0) \tag{2.13}$$

From (2.8),

$$\frac{1}{\rho_z} = \frac{d^2 z}{dx^2} = \frac{\sum_{i=1}^{n} \alpha_i A_i z_{ic} E_i}{\sum_{i=1}^{n} E_i I_{yic}} (T - T_0) = K_{\rho z}(T - T_0) \tag{2.14}$$

where, ρ_z, is the radius of curvature of the beam. Qualitatively, the numerator of the expression represents the sum of the bending moments produced due to temperature change about the neutral axis. The denominator is the total flexural rigidity of the beam, with the moment of inertia measured about the neutral axis.

The radius of curvature can be calculated for the lateral bending case in a similar manner.

$$\frac{d^2 y}{dx^2} = \frac{1}{\rho_{yT_o}} + \frac{-\sum_{i=1}^{n} \alpha_i A_i y_{ic} E_i}{\sum_{i=1}^{n} E_i I_{xic}} (T - T_{0l}) = \frac{1}{\rho_{yT_o}} + K_{\rho_y}(T - T_0) = \frac{1}{\rho_y} \tag{2.15}$$

where ρ_{yTo} is the radius of curvature at T_{ol}. This radius of curvature accounts for the manufacturing-induced lateral stress differences.

2.3 Parameter Extraction for TCE

To accurately predict the effect of temperature on stress, material properties and thickness of each layer has to be obtained. Mechanical material properties of individual layers is difficult to obtain as the CMOS process occurs in a standard foundry process. Also since microstructures can only be designed with a top metal layer, mechanical properties of individual layers using techniques proposed in [22] cannot be readily applied. Effective Young's modulus measurement of the various beam types was obtained in [23] using resonating beam test structures. The beam types measured included all possible combinations of metal 1,2,3 and polysilicon of the CMOS process that can be practically fabricated using the micromachining process. Published values of Young's moduli were used for the individual layers.

The variation of stress gradients is a strong function of temperature coefficients of expansions of the various metal and oxide layers. The TCE of each of the layers is a function of the deposition parameters and may be different for each layer, even if they are composed of the same material. However, we propose in this thesis to extract TCE values for aluminum, oxide and polysilicon to best-fit the measured data. The use of this technique is appropriate as material properties of each

layer cannot be measured independently as we do not have access to partially processed wafers from the CMOS foundry. The final use of TCE values is to predict the curvature change the best-fit values result suffice that purpose. These best-fit values are used to model the stress effects in CMOS micromachined devices. A test structure to measure the radii of curvature of the various combinations of beams at various temperatures was designed and fabricated.

The scanning electron micrograph (SEM) of the test structure is shown in Figure 2.3. It consists of a plate with beams embedded in the center. The plate is heated by an integrated polysilicon resistor. The plate is thermally isolated from the substrate using long and thin springs which ensures a uniform temperature across the device. The use of this test structure for measurement of curl was found yield more accurate and repeatable results compared to the earlier measurements made on heated cantilever beams reported in [12]. The main advantages are

- The temperature of the beams can be accurately determined from polysilicon resistance measurements.
- Measurements are made on packaged die, and therefore the measurements accurately reflect the effects of packaging that are seen by actual devices.
- The setup does not require specialized temperature controlled wafer holders as with earlier measurements. All the curvatures are measured directly by the white light interferometer.

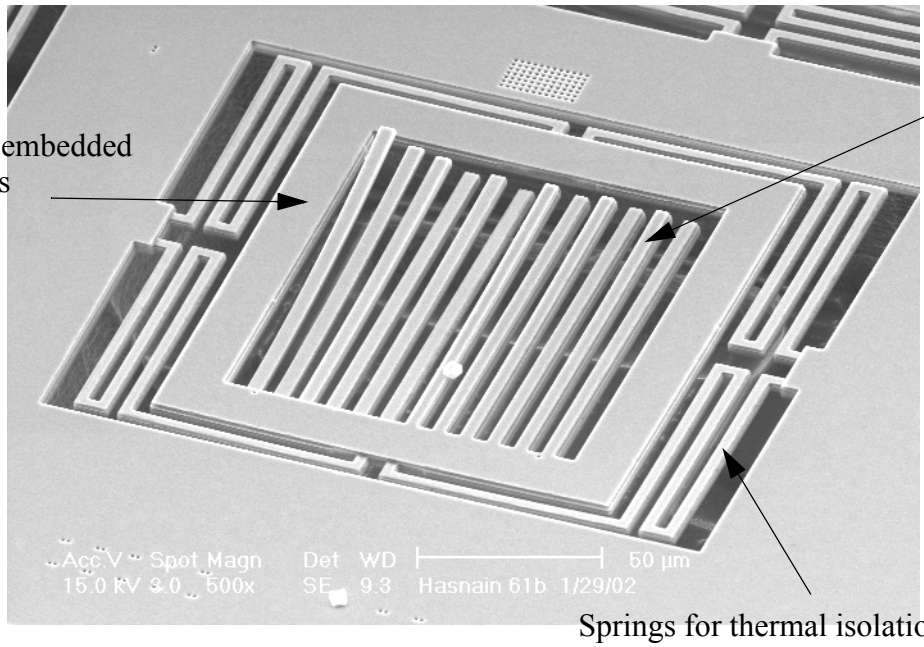


Figure 2.3 SEM of the test structure used for calculation of device curl with temperature. The structure is heated by joule heating of the embedded polysilicon resistors. The temperature of the structure is obtained by monitoring the resistance of the polysilicon resistance.

The temperature distribution in the device due to current flow in the polysilicon resistor was simulated using FEM modeling, and is shown in Figure 2.4. The temperature within the entire structure is uniform, as heat conduction through air is negligible. The uniform temperature distribution in air implies that this test structure can used with ambient air, without the need for vacuum, greatly simplifying the measurement setup. As current is passed through the polysilicon heater embedded in the plate, the temperature increases, due to Joule heating. The resistance of the polysilicon is a function of temperature and is characterized by a temperature coefficient of resistance. The temperature of the structure is set by controlling the resistance of the polysilicon resistor to a constant value, determined by the set temperatures. The details of this technique are detailed in Chapter 5. The radius of curvature for each of the beam types was measured using a white light interferometer. Best-fit values of TCE were obtained for metal, oxide, and the polysilicon layers using (2.14). The thickness of each metal, oxide and polysilicon layer is obtained by measurement of beam cross-section made using a focussed ion beam (FIB), by a scanning electron microscope. The characteristic temperature, T_0, is calculated from the radius of curvature measured at 292K (room temperature). Table 2.1 compares the change in deflection with temperature of a 100 μm long cantilever calculated using measured and analytically-

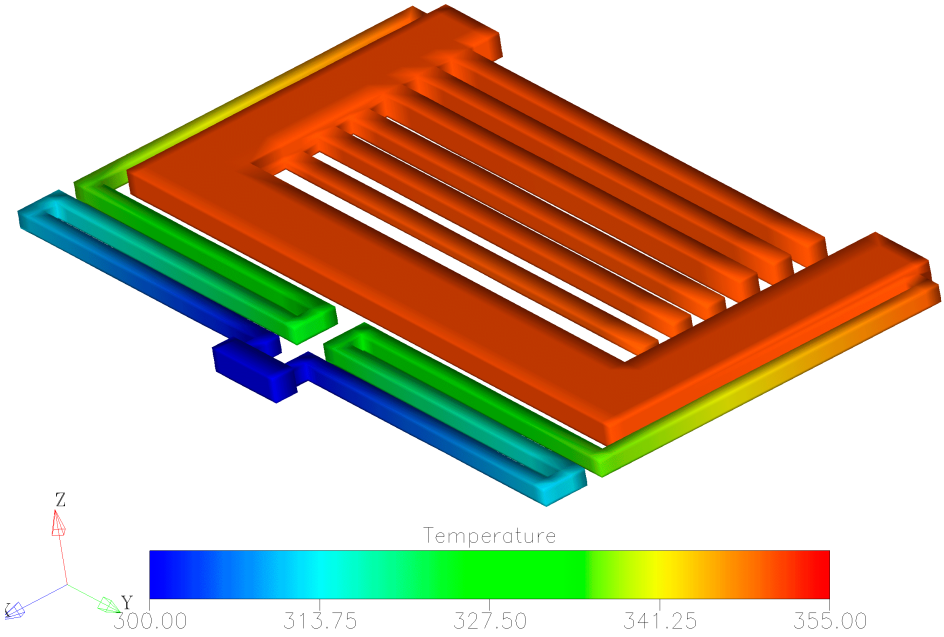


Figure 2.4 FEM simulation of the test structure for a heater temperature of 350K. The symmetry of the device has been exploited to reduce the problem size. The temperature of the beam is very close to that of the heater plate.

Table 2.1: Summary of Test structure measurement results. Comparison of the change in deflection with temperature of a 100 μm long cantilever calculated using measured and analytic values of radius of curvature

Beam Type	Measured (nm/K)	Analytical eqn. (2.14) (nm/K)	Error % analytical/ measured	FEM (nm/K)	ρ_z at 292K (mm)	T_o (K)
M123P	-11.21	-11.48	2.34	-11.53	12.4	328.46
M3P	-11.52	-11.96	3.67	-11.81	5.5	370.83
M23P	-16.45	-16.75	1.77	-16.63	7.3	334.13
M12P	-17.61	-18.72	5.91	-18.59	81.0	296.01
M2P	-17.94	-18.72	4.15	-18.61	2.9	387.94
M1P	-76.35	-71.78	-6.37	-70.59	0.6	403.49
M123	-12.60	-12.06	-4.48	-12.27	2.6	444.60
M3	-14.64	-15.05	2.67	-15.19	1.6	509.97
M23	-19.31	-19.43	0.63	-19.37	1.8	433.24
M12	-19.81	-20.93	5.36	-20.49	1.6	446.42
M2	-25.76	-24.20	-6.43	-24.13	0.9	499.03
M1	-75.12	-77.77	3.40	-76.56	0.4	477.38
M13P	-6.90	-6.69	-3.14	-6.62	113.6	298.88
M13	-7.71	-7.63	-1.07	-7.59	15.7	333.75

Table 2.2: Layer thickness measured from FIB cross section of a M123P beam

Material	layer thickness (nm)
Bottom oxide (bo)	450
Polysilicon (poly)	250
Oxide between poly and metal 1 (oxp1)	550
Metal 1 (m1)	700
Oxide between metal 1 and metal 2 (ox12)	860
Metal 2 (m2)	700
Oxide between metal 2 and metal 3 (ox12)	860
Metal 3 (m3)	660

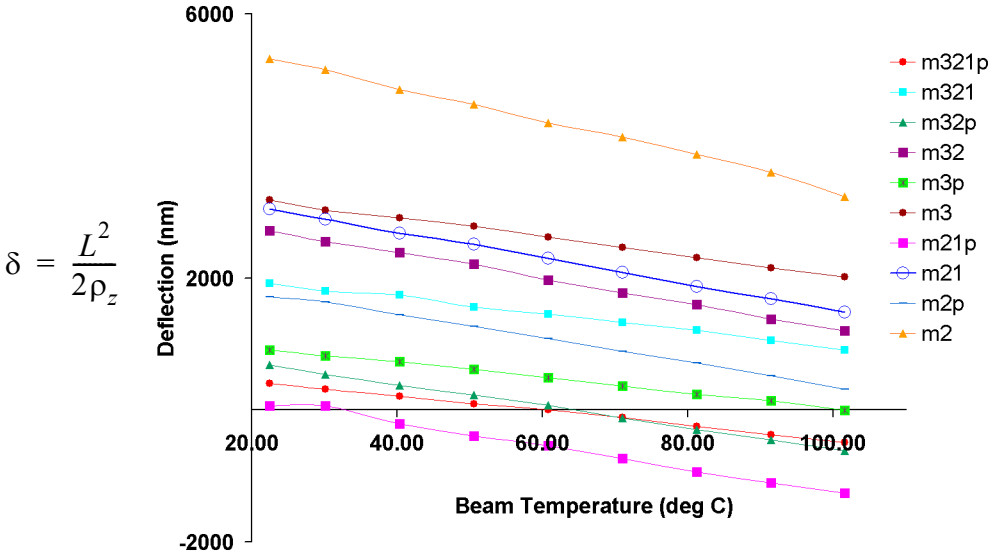


Figure 2.5 Out-of-plane deflection of a 100 μm long beam calculated from the measured radius of curvature for some CMOS micromachined beam types.

calculated values of radius of curvature, using (2.14). The layer thickness of the CMOS process used for the analysis were measured using a focussed ion beam (FIB) image of a beam containing metal 1, 2, 3 and polysilicon and are shown in Table 2.2. The error between finite element analysis is seen to be less than 2% for all cases.

The change of deflection with temperature for a beam of length L can be calculated using

$$\frac{d\delta}{dT} = \frac{d}{dT}\left(\frac{L^2}{2\rho_z}\right) = \frac{L^2}{2}\left(\frac{-\sum_{i=1}^{n}\alpha_i A_i z_{ic} E_i}{\sum_{i=1}^{n} E_i I_{yic}}\right) \tag{2.16}$$

where δ is the out-of-plane deflection of the beam. The out-of-plane deflection of a 100 μm long beam calculated from the measured radius of curvature is shown in Figure 2.5. The best fit values of the TCE for metal, oxide and polysilicon are calculated such that the root mean square error given by

$$\vartheta = \sqrt{\frac{1}{k}\sum\left(\frac{d}{dT}\frac{1}{\rho_{measured}} - \frac{-\sum_{i=1}^{n}\alpha_i A_i z_{ic} E_i}{\sum_{i=1}^{n} E_i I_{yic}}\right)^2} \tag{2.17}$$

Table 2.3: Summary of the mechanical parameters used in the simulation

Layer	Young's Modulus [46][47]	TCE (best fit)	TCE [46]
Metal	70 GPa	21μ/K	28.3μ/K
Oxide	75 GPa	0.23μ/K	0.4μ/K
Polysilicon	160 GPa	4.3μ/K	2.3μ/K
Field Oxide	57 GPa	0.53μ/K	0.4μ/K

is minimized for measurements made over *k* combinations of CMOS micromachined beam types (Figure 2.6). Table 2.3 summarizes the TCE values, that yields the minimum root mean square error of about 4%, along with values obtained from literature. The Young's modulus used in the calculation is also listed in Table 2.3. The analytical expressions derived for curling have been successfully applied to calculate displacements in CMOS micromachined thermal actuators for scanning tunneling microscope (STM) applications with device temperature. The details of the analysis are presented in [24]. Thermal actuators have also been used to fabricate micro-mirrors in [25].

2.3.1 Curl Prediction Using Characteristic Temperature.

The characteristic temperature obtained for each beam provides a conceptually easy method to predict the curl of complicated CMOS microstructures. This method assumes that the stress in all the layers of the CMOS micromachined structures is zero. This assumption is not truly valid for large fixed-fixed structures. However, good results can be obtained for small structures. The curl of structure can be simulated by setting the temperature of all the layers of the simulator to be

$$T_{set} = -T_0 + T_{sim} + T_d \tag{2.18}$$

where T_o is the characteristic temperature obtained from Table 2.1, determined by the type of beams used in the device design. Sometimes more than a single type of beam may be used in a structure; in this case the T_o for the most common type of beam may be used. T_{sim} is the simulator initial temperature, usually 273 K, and T_d is the device temperature.

A finite element model with all layers taking into account the various beam combinations of the device is automatically generated by techniques described in Section 2.7. An example of the predictive capability of the FEA is given by the analysis of the CMOS micromachined

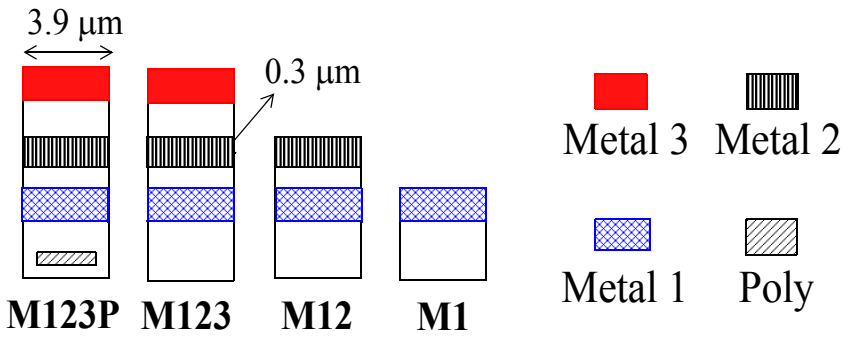


Figure 2.6 Example of beam combinations.

accelerometer [26][7] shown in Figure 2.7. The simulation temperature is determined by the type of beam element that dominates the accelerometer design. For example, in the CMOS micromachined accelerometer case, the characteristic temperature is calculated to be 496 K using an area-weighted average of the beam materials. Note that this temperature was extracted from using data measured from the same run as the accelerometer, as described in [12]. Characterization of curl for these measurements was done on simple cantilever beam structures that were heated externally. The die were not packaged and were glued to a silicon wafer. Temperature of the chip was obtained by placing thermocouples very close to the chip. The simulation temperature is computed using (2.18). The maximum stator deflection of the accelerometer is compared to FEA in Figure 2.7(a). The predicted curl variation, shown in Figure 2.7b matches within experimental error to the curl of the actual device, as seen in Figure 2.7c. The close up of the curl matching between the stator and the rotor comb fingers shown in the inset.

2.3.2 Characterization of Lateral Curl with Temperature

SEM of the test structure designed for lateral curl measurement is shown in Figure 2.8. The cantilever beams are suspended on thermally isolated heated base. The base is heated by Joule heating due to an integrated polysilicon resistor. The thermal isolation is obtained using long thin beams that are connected to the substrate connected metal using metal to metal vias. This thermal isolation technique is detailed in Chapter 3

The lateral curl is measured between the alternating aligned and misaligned beams. The manufacturing misalignments are eliminated to the first order. The dynamic measurement technique leverages the capability of a MIT microvision [27] to measure lateral deflections very accurately.

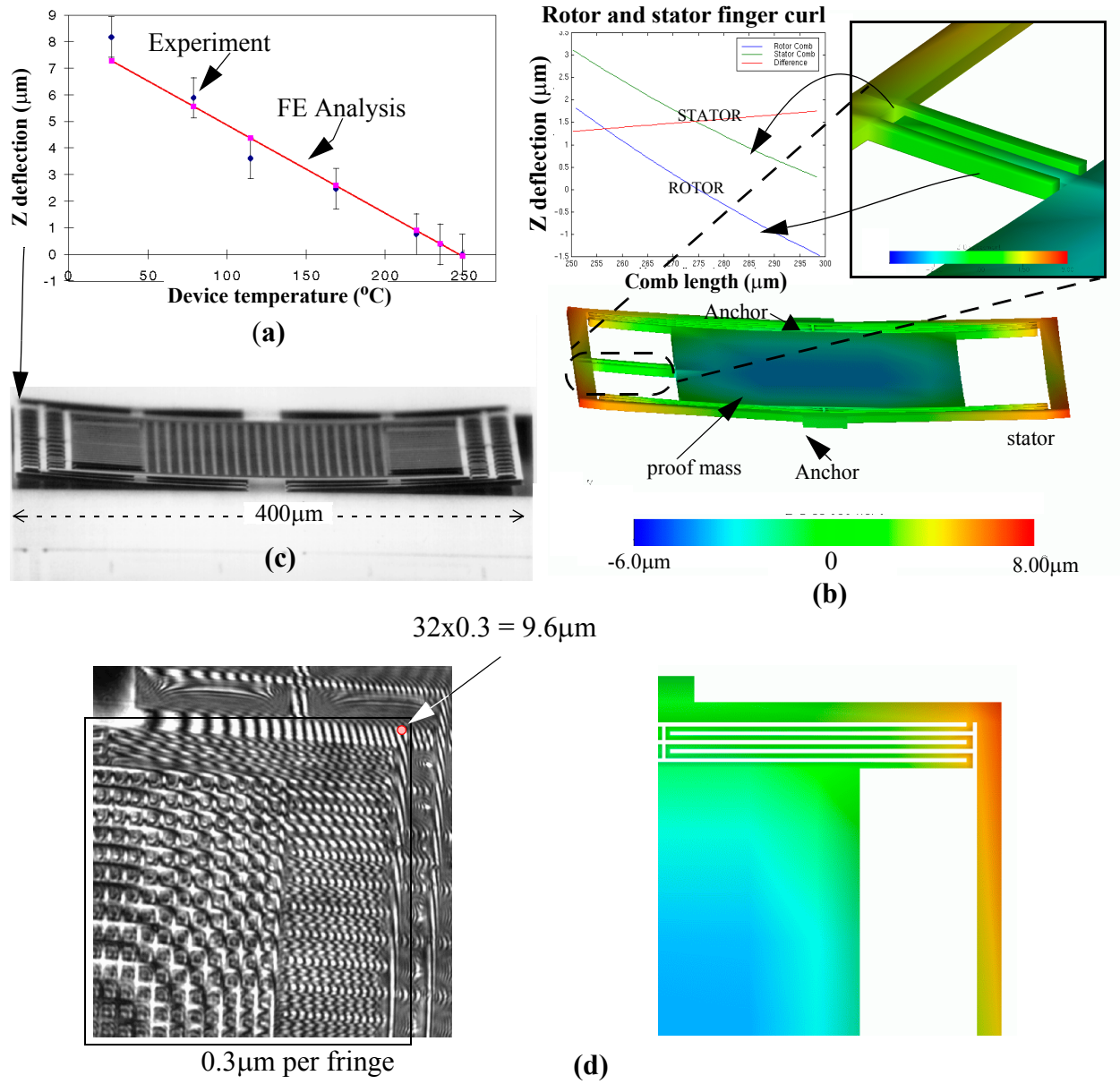


Figure 2.7 (a) Maximum stator deflection with temperature compared with thermomechanical FEA simulation. (b) The simulated curling in a CMOS accelerometer, (c) compared to a scanning electron micrograph of an actual device. (d) Comparison of interferometry measurements to FEA

Ohmic heating is used to increase the temperature of the base of the beams. The temperature of the entire beam is the same as that of the base. This is true as thermal losses to the substrate are small, due to the small device area. Convention and radiation losses are also negligible. The temperature of the base is same as that of the beams. This was verified by FEM simulation of the structure simulating the temperature distribution of the device in air. The temperature distribution

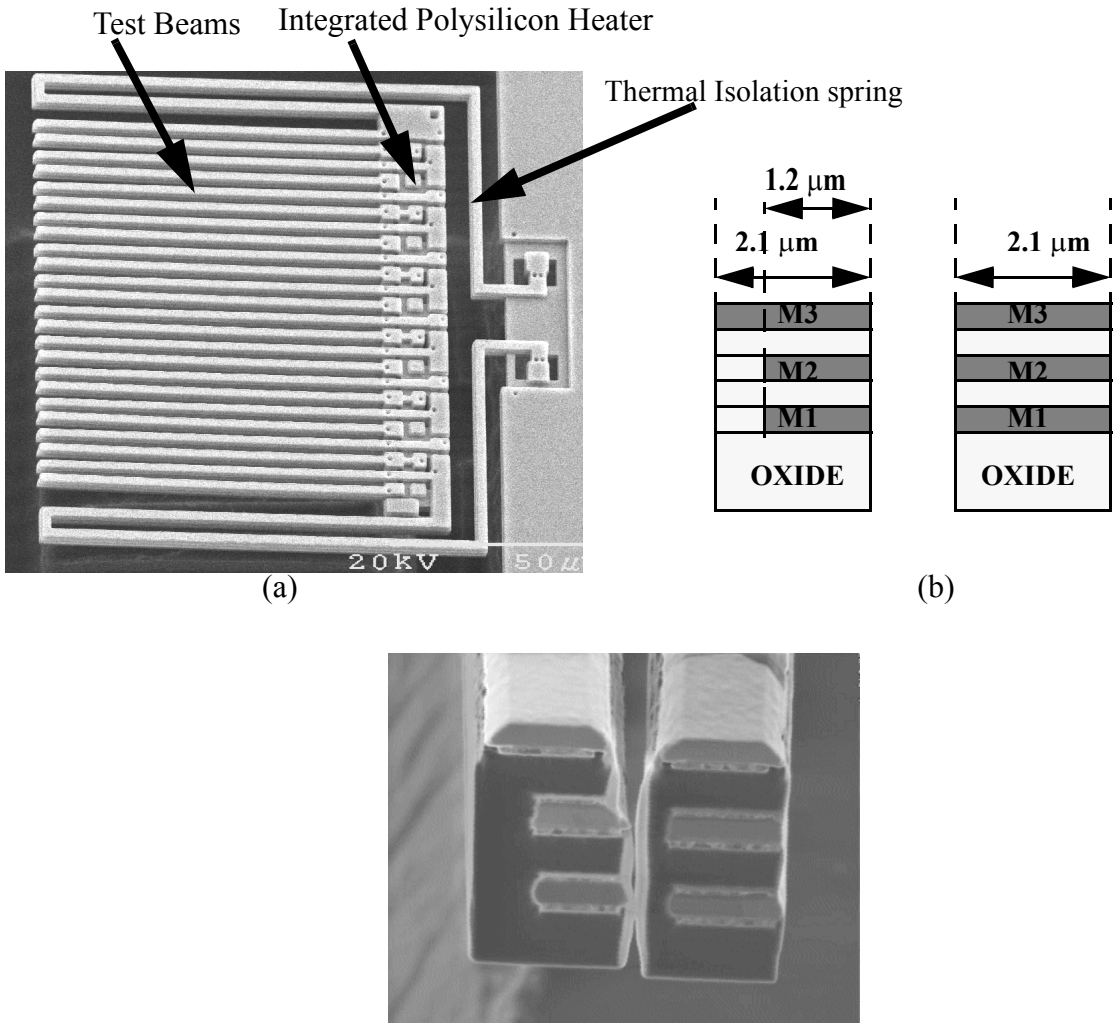


Figure 2.8 (a) SEM of the test structure used to characterize beam curling with temperature. It consists of alternating misaligned and symmetric beams (b) Cross-section of the measured beams (misaligned), along with the reference (aligned) beam. (c) FIB cross-section of the beams.

within the structure for 10 mA of current flowing through the resistor is shown in Figure 2.9. The device temperature was extracted from the resistance change in the polysilicon heater. The temperature characteristic of the polysilicon heater was obtained separately by measuring the resistance of the polysilicon heater while the device was placed in a temperature-controlled oven. The device temperature was measured using the temperature characteristic of threshold voltage of the N-well-substrate diode. Measurements with an infrared microscope were made to confirm the uniform temperature distribution.

A 10 Hz triangular heating pulse was applied to the heater. Beam deflections in the lateral direction and the beam curvature were measured using the MIT microvision system [27]. The

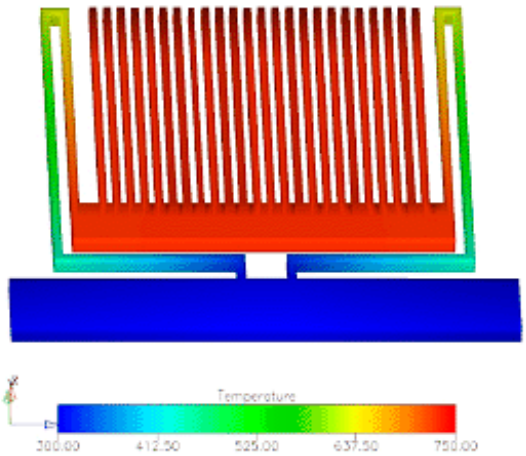


Figure 2.9 The temperature distribution within the device, for a heater current of 10 mA.

temperature distribution is expected to reach its equilibrium value at every measurement as the thermal time constant of the structure is 6 ms. Comparison of the measured lateral deflection vs. temperature with the analytical calculation is shown in Figure 2.10. A measured 0.15 μm overetch was incorporated in the deflection computation. The measured and the modeled deflections match to within 15% for large deflections. Possible sources of error include temperature calibration and microvision resolution.

2.4 Temperature Effects of Residual Stress

Temperature change in a beam, causes an axial strain, in addition to a strain gradient. The axial strain occurs as all the layers of the beam expand. This produces a change in the effective residual stress of the beam. In this section, we derive effective values of TCE, and biaxial

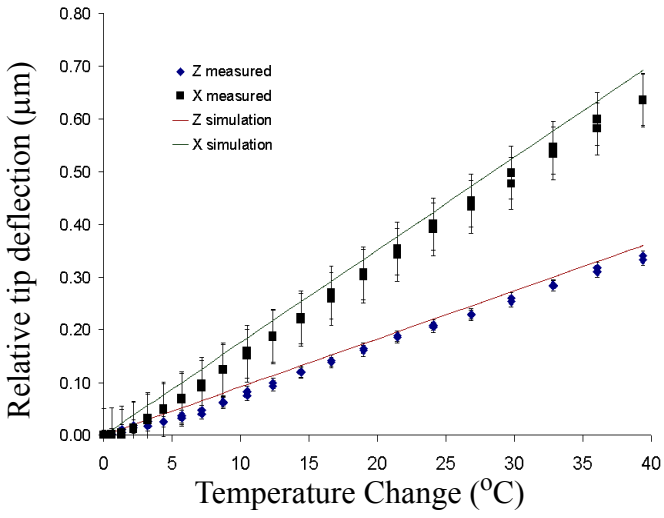


Figure 2.10 Comparison of relative lateral and out-of-plane tip deflection from measurements and analytical calculations showing a match to within 15%.

modulus that can characterize the change in effective residual stress and strain when the beam is heated. The effective value of TCE is useful in considering the effects of temperature when the CMOS beam is approximated by a single layer.

The residual stress in each layer before release is

$$\sigma_i = \sigma_{io} - E_i \alpha_i (T - T_o) \tag{2.19}$$

where σ_i is the unreleased residual stress of the layer at temperature T, and σ_{io} is the unreleased residual stress of the layer at temperature T_o. The substrate is assumed to be infinitely thick, with zero TCE. The total axial force developed at temperature T is given by

$$\sum_{i=1}^{n} A_i \sigma_i = \sum_{i=1}^{n} A_i \sigma_{io} - \sum_{i=1}^{n} A_i E_i \alpha_i (T - T_o) \tag{2.20}$$

If σ_T is the effective residual stress at temperature T, and σ_o is the effective residual stress at the characteristic temperature, then

$$\sigma_T = \frac{\sum_{i=1}^{n} A_i \sigma_{io}}{\sum_{i=1}^{n} A_i} + \frac{\sum_{i=1}^{n} A_i E_i \alpha_i (T - T_o)}{\sum_{i=1}^{n} A_i} = \sigma_o + E_{eff} \alpha_{eff} (T - T_o) \tag{2.21}$$

where, σ_o is the effective residual stress at temperature T_o. The temperature variation of effective residual stress can be expressed in terms of the effective beam constants. E_{eff}, is the effective biaxial modulus of the beam, given by the ratio of

$$E_{eff} = \frac{\sum_{i=1}^{n} A_i E_i}{\sum_{i=1}^{n} A_i} \tag{2.22}$$

This is an area-weighted average of the biaxial modulus of the beam. α_{eff}, is the effect thermal expansion coefficient producing an extension of the neutral axis, given by

$$\alpha_{eff} = \frac{\sum_{i=1}^{n} \alpha_i A_i E_i}{\sum_{i=1}^{n} A_i E_i} \tag{2.23}$$

When the beam is released the effective axial stress is translated to a stress gradient in the beam that produces the curl and strain along the neutral axis. The strain after release along the neutral axis is due to the common extension of all the layers of the multi-layer beam. This strain, ε_T, is relative to the unreleased state, and can be expressed as

$$\varepsilon_T = \frac{\sigma_T}{E_{eff}} = -\left(\frac{\sigma_o}{E_{eff}} + \alpha_{eff}(T - T_o)\right) = \alpha_{eff}(T - T_o) + \varepsilon_o \tag{2.24}$$

where, ε_T, is the common strain in the beam at temperature T, and ε_o is the common strain in the beam at temperature T_o respectively.

Effective residual stress in each type of beam can be measured using residual stress measurement test structures proposed in [28]. Measurements of residual stress on the various beam types have been made in [23], using that technique. If σ_{Tr} is the measured effective residual stress in the beam at room temperature, T_r, then from (2.21),

$$\sigma_{T_r} = \sigma_o - E_{eff}\alpha_{eff}(T_r - T_o) \tag{2.25}$$

Eliminating σ_o from (2.21) and (2.25), we can write the effective residual stress in the beam at any temperature, T as

$$\sigma_T = \sigma_{T_r} - E_{eff}\alpha_{eff}(T - T_r) \tag{2.26}$$

It is observed that the effective residual stress in CMOS micromachined beam is a function of temperature. The values of α_{eff} from CMOS micromachined beams ranges from 8.77 x 10^{-6} /K for beam containing metal 1,2,3 and polysilicon layers to 2.95 x 10^{-6} /K for a M3 beam. The temperature coefficient of residual stress for the various combinations of CMOS micromachined beam $E_{eff}\alpha_{eff}$, has been calculated from experimentally extracted TCE values in Table 2.4, for the Agilent 0.5 μm process. The values in Table 2.4 are computed using data in Table 2.1 and Table 2.3.

Table 2.4: Temperature coefficient of residual stress for various combinations of CMOS micromachined beams

Beam Type	α_{eff} x 10^{-6}/K	E_{eff} GPa	$\alpha_{eff}E_{eff}$ x MPa/K
M123P	8.72	75.6	0.659
M3P	3.22	77.0	0.248
M23P	5.95	76.3	0.453
M12P	7.72	77.2	0.597
M2P	3.58	78.3	0.280
M1P	7.22	80.6	0.582
M123	8.77	71.3	0.626
M3	2.95	72.7	0.215
M23	5.83	72.0	0.420
M12	7.71	70.7	0.546
M2	3.19	71.8	0.229
M1	7.12	69.0	0.491

2.4.1 Macromodel of Effective Stress And Stress Gradient

A macromodel for CMOS micromachined beams has been developed in NODAS [29][30][31], based on effective beam properties. To account for the effect of axial strains in beams due to residual stress and the change in beam/structural curl due to temperature, a model of the residual stress based on experimental measurements can be derived. The stress in the beam can be expressed in terms of the effective beam properties, the effective TCE of the beam and the effective residual stress in the beam at room temperature. This model of the stress and gradient in the beam can easily be incorporated into a macro-modelling environment like NODAS.

The stress gradient in the beam causes the beam to curl. The strain in a cantilever beam, along the neutral-axis when it is released can be expressed as

$$\varepsilon(z, T) = (z - z_{ec})\frac{\mathrm{d}^2 z}{\mathrm{d}x^2} = \frac{z - z_{ec}}{\rho(T)} \tag{2.27}$$

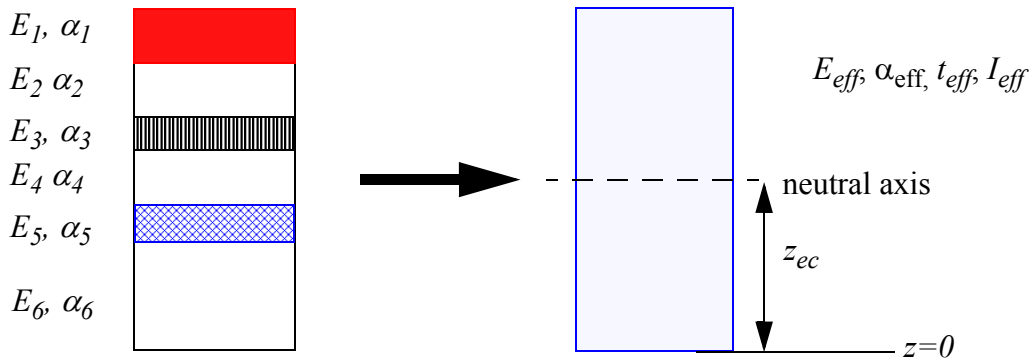


Figure 2.11 Multi-layered CMOS beam modeled as a single layer beam with effective mechanical properties.

where, ρ is the radius of curvature of the beam, derived for each beam type in (2.14), and z_{ec} is the location of the neutral axis of the beam with effective material properties. Effective material properties are used to represent the beam as illustrated in Figure 2.11. The location of the neutral axis is at half the thickness of the beam. It should be noted that the strain due to the curl, as described by the above equation, produces no average strain at the neutral axis, which means that the curl is modeled due to pure stress gradient. The equivalent stress gradient, $\sigma_{eff\Delta}$, in the effective beam is given by

$$\sigma_{eff\Delta} = E_{eff}\left(\frac{z - z_{ec}}{\rho(T)}\right) \tag{2.28}$$

The total stress in the effective beam can be written using (2.26), as

$$\sigma_{eff} = \sigma_T - E_{eff}\left(\frac{z - z_{ec}}{\rho(T)}\right) = \sigma_{T_r} - E_{eff}\alpha_{eff}(T - T_r) - E_{eff}K_{\rho z}(z - z_{ec})(T - T_o) \tag{2.29}$$

The last term in the above expression is based on measurements that can be made using the test structure proposed in Section 2.3. Many finite element simulators allow for a stress and stress gradients to be defined for materials. Using this value of stress can accurately model the effects of stress and temperatures in CMOS micromachined structures and speed up the simulations. This expression is convenient for modeling stress in circuit based mechanical simulators like NODAS.

2.5 Extraction of Residual Stress from Curl Measurements

The discussion in the preceding chapters assumed that the stress in the layers at the characteristic temperature is zero. To accurately account for the effects of residual stress, the axial strains induced due to temperature change must be accounted for in the FEM simulations. We propose to obtain the residual stress in each layer of the beam that would produce the same axial

strains measured from the beam. The exact pre-release stress in each layer of the beam is difficult to measure, as access to the individual thin films of the process is limited. However, for the purposes of computing curl in CMOS structures a set of best fit values of residual stress in each layer can be obtained from experimental observations of curl from all possible layer-combinations of the CMOS beams. A technique similar to that used to obtain best-fit values of TCE in Section 2.5.

The simulation of curl in CMOS micromachined structures using the characteristic temperature of the type of beam is not convenient if the CMOS micromachined device contains more that one type of beam. For example, consider the case in which beams containing metal 1 and 2 are used in the springs and the rest of the structure contains beams that have all the metal layers (1, 2, and 3). This is true for the z-axis accelerometer presented in Chapter 4. The use of a single characteristic temperature will not yield the correct results. For correct simulation, the stress in every layer must be used. The stress in each CMOS layer (metal or oxide) is dependent highly on the manufacturing process. The presence of cladding layers above and below the metal layers affects the stress of the metal layer. The situation is also complicated by etching of the cladding layer of the top-most metal due to ion-milling during the CMOS micromachining process. If it is assumed that the stress in every layer of the CMOS stack (metals, dielectrics, and polysilicon) is the same, independent of the composition of the beam, then a "best fit" set of stress values can be obtained that satisfies the experimentally measured curl in the beam at room temperature. The residual stress calculation using such a technique based on bucking stress of fixed-fixed beams has been proposed in [32].

The CMOS beam can be considered to be composed of the following distinct materials, bottom field oxide (bo), polysilicon (poly), oxide between polysilicon and metal 1 (oxp1), metal 1 (m1), oxide between metal 1 and metal 2 (ox12), metal 2 (m2), oxide between metal 2 and metal 3 (oxm23) and metal 3 (m3). All these layers are present in a beam composed of metal 1,2,3, and polysilicon layers. If the metal is not present in the beam, its void space is assumed to be occupied by the oxide layer on its top. This is due to the chemical mechanical polishing (CMP) used by most CMOS foundries. Figure 2.12 illustrates the various layers in beams composed of metal 1,2,3 and polysilicon (M123P), and a beam composed M3 layers only.

The total internal bending moment of the beam at temperature T_r, is expressed using (2.8), as

$$M_{yu} = \sum_{i=1}^{n} \left(E_i I_{yic} \frac{\mathrm{d}^2 z}{\mathrm{d}x} \right) = \frac{1}{\rho(T_r)} \sum_{i=1}^{n} E_i I_{yic} \tag{2.30}$$

where, M_{yu} is the total internal bending moment produced when the beam is released. The total bending moment due to release of the beam is produced due to the residual stresses in each layer of the beam, and can be expressed in terms of the residual stress as

$$M_{yu} = -\sum_{i=1}^{n} \sigma_i A_i z_{ic} \tag{2.31}$$

σ_i is the unreleased stress in the i-th layer of the beam. Combining (2.30), and (2.31),

$$-\sum_{i=1}^{n} \sigma_i A_i z_{ic} = \frac{1}{\rho(T_r)} \sum_{i=1}^{n} E_i I_{yic} \tag{2.32}$$

This equation has multiple solutions for the stress of each layer. However, due to our assumption that the stress of material is independent of the composition of the beam, we can write (2.32) in terms of the stress of the material content of that layer. The stress in the individual materials is denoted by

- σ_{bo} for the bottom-most field oxide layer,
- σ_{poly} for the polysilicon layer,
- σ_{oxp1} for the oxide between the polysilicon layer and metal 1 layer,
- σ_{m1} for the metal 1 layer,

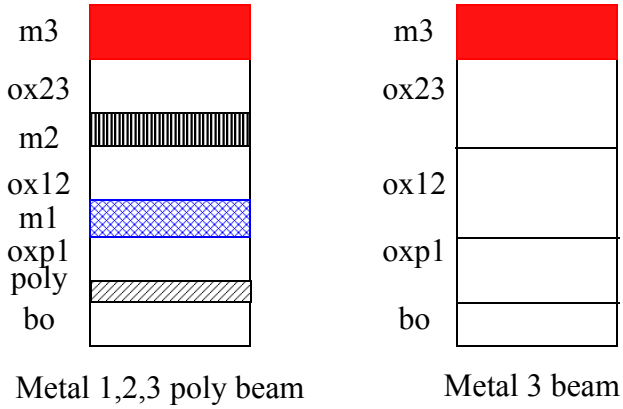


Figure 2.12 Modeling of the various layers of the CMOS beam to represent all beam combinations to be composed of 8 constituent materials. The metal 1,2,3 poly beam contains all the 8 materials, while the m3 beam contains only five layers. The CMP process is assumed to be ideal, so that m3 is at the same level.

- σ_{ox12} for the oxide between the metal 1 layer and metal 2 layer,
- σ_{m2} for the bottom-most field oxide,
- σ_{ox23} for the oxide between the metal 2 layer and metal 3 layer,
- and σ_{m3} for the metal 3 layer.

This leads to 8 values of stress that need to be solved. The R.H.S. of (2.32), is computed for each beam type by making measurements of radius of curvature at room temperature (T_r=292.5K). These measurements have been made using the test structure proposed in Section 2.3. Measurements were made on 12 different types of beams, out which 10 were used for the best fit analysis to avoid simulator convergence problems. This linear optimization problem was solved in MATLAB [33]. The stresses calculated in each layer have been summarized in Table 2.5. The total root mean square error between the measured radius of curvature and that calculated from the values of stress from Table 2.5 is 20.73%.

The stress in sputter-deposited metal is generally tensile, however the stress obtained by the best-fit for metal 3 is compressive. Also the field oxide is highly compressive due to the thermal oxidation process. Further the oxide between metal 1 and polysilicon is seen to be highly compressive, eventhough the same dielectric material is used by the foundry for the insulation between the other metals. There are several reasons for the differences in the calculated stress values and those expected from common wisdom.

- Errors in calculation of metal residual stresses could be due to the variation of the stresses due

Table 2.5: Stress in the various material of the Agilent 0.5μm process calculated from data in Table 2.3, along with the layer thickness.

Material	layer thickness (nm)	Stress (MPa)
Bottom oxide (bo)	450	-85.16
Polysilicon (poly)	250	73.08
Oxide between poly and metal 1 (oxp1)	550	-224.24
Metal 1 (m1)	700	135.74
Oxide between metal 1 and metal 2 (ox12)	860	-175.30
Metal 2 (m2)	700	116.79
Oxide between metal 2 and metal 3 (ox12)	860	22.98
Metal 3 (m3)	660	-117.24

to presence of cladding layers. The cladding layers are normally present above and below a metal layer. These layers can be seen clearly in the SEM of the FIB cross-section in Figure 2.8. However, due to ion-milling during the CMOS micromachining post process, the top cladding layer is removed.

- The other factor contributing to the error is the inaccurate measurement of the layer thickness. The layer thickness in CMP can be a function of the metal density. If a die does not have uniform metal density in all the layers then variations in thickness are possible. The last reason for the larger error is the possible difference in layer thickness between the die on which the thickness measurements and curvature measurements were made. This error was minimized using die from the same wafer.

The effective residual stress of the beam stress can be calculated if the stress of each layer is known using

Table 2.6: Comparison of the measured radius of curvature, to that calculated from extracted stress values in Table 2.5. The effective stress in each beam compared to measurement made in [23]

Beam Type	**ρ(Tr) measured (mm)**	**ρ(Tr) calculated eqn. (2.32) (mm)**	**Error %**	**σ_{eff}(Tr) (calculated) MPa**	**σ_{eff}(Tr) (measured) MPa [23]**
M123P	-12.40	-10.92	13.5	-34.79	-29.2
M3P	-5.54	-3.89	42.09	-91.13	not measured
M2P	-2.92	-3.49	-16.45	-111.05	not measured
M1P	-0.59	-0.58	0.36	-35.33	not measured
M123	-2.61	-3.04	-14.32	-49.56	-42.8
M3	-1.57	-1.81	-13.65	-105.91	-102.7
M23	-1.84	-1.66	10.79	-92.85	-70.8
M12	-1.64	-1.21	35.17	-67.19	-59.7
M2	-0.94	-1.11	-15.45	-133.78	-93.1
M1	-0.36	-0.36	-0.16	-75.95	-53.3

$$\sigma_{eff}(T_r) = \frac{\sum_{i=1}^{n} \sigma_i(T_r) A_i}{\sum_{i=1}^{n} A_i} \tag{2.33}$$

The values of residual stress obtained using the above equation have been compared to that reported in [23]. There is reasonable agreement between the calculated and measured values. It should be noted that the effective residual stress values reported in [23] were made on an entirely different foundry run, about three years than the one in Table 2.5.

A comparison of the measured radius of curvature, and that calculated from values in Table 2.5 using (2.32), is shown in Table 2.6. The residual stress values calculated from the best fit values is in reasonable agreement with effective residual stress measurements made using a bent beam test structure in [23]. Measurements of radius of curvature on various dies fabricated in the Agilent 0.5μm [34] process followed by the CMOS micromachining process have shown a variation of about 30% from run to run [23].

The curvature calculated using individual stress values using (2.32), was verified using Coventorware [35]. The values agree to within 3%. The calculated stress values were converted to an isotropic stress value using

$$\sigma_{iso} = \frac{\sigma_{cal}}{(1-2\nu)} \tag{2.34}$$

In conclusion, one can argue that the stress values derived in Table 2.5, serve the purpose of predicting effects of curl and residual stress in CMOS micromachined structures as the measured curl in CMOS micromachined structure varies by as much as 30% from run to run.

2.6 Characterization of Polysilicon Heaters

The resistivity of polysilicon is a function of temperature, and is higher than that of the metal of the CMOS process. Further the melting temperature of the polysilicon is higher than that of the metal (aluminum) of the CMOS process. These properties make the polysilicon layer, an ideal material for design of on-chip heaters and temperature sensors. An ideal heater must provide heat energy to the surrounding without destroying itself. Heater resistors are implemented using materials that have a high melting point and high resistivity. For design of integrated heaters embedded in CMOS micromachined devices, the heater resistance is constrained by the voltage

supply of the CMOS chip. The maximum supply voltage (V_{ddmax}) for the Agilent 0.5 μm [34] process is 5V. The heater resistance, R_{heater}, is determined by

$$R_{heater} = \frac{V_{ddmax}^2}{P_{max}} \tag{2.35}$$

Where, P_{max} is the maximum power dissipation desired in the device. For a 10 mW power dissipation and V_{ddmax}=5 V, the heater resistor is 2.5 KΩ. These values indicate the suitability of the polysilicon for heating CMOS micromachined device. The resistivity of the polysilicon layer in the Agilent 0.5 μm process [34] is 2.3 Ω/square. The resistivity of the polysilicon layer without the silicided is 110 Ω/square. This value was measured using a four probe measurement test structure.

2.6.1 Characterization of Temperature Coefficient of Resistance (TCR) of Polysilicon

The change in resistance of polysilicon is characterized by the temperature coefficient of resistance (TCR), α_p, that is defined as

$$\alpha_p = \frac{R_T - R_{T_o}}{R_{T_o}(T - T_o)} \tag{2.36}$$

where, R_T is the resistance at temperature T and R_{To} is the resistance at temperature T_o. The resistance of the polysilicon is also a function of stress in the material. The variation of the resistance with stress is characterized by the piezoresistive coefficient that is defined as

$$\pi_p = \frac{R_\sigma - R_{\sigma o}}{R_{\sigma o}(\sigma - \sigma_o)} \tag{2.37}$$

where, $R_{\sigma o}$ is the resistance when the stress in the polysilicon is σ_o, and R_σ is the resistance when the stress in the polysilicon is σ. The dependence of resistance on polysilicon stress means that the temperature coefficient of resistance measured for polysilicon embedded in a released beam is different from that of an unreleased beam. The increase in temperature increases the stress in the polysilicon layer causing the resistance change that is the combination of the temperature effect and the piezoresistive effect. The measured piezoresistive coefficient of polysilicon has been reported in literature and was observed to be -4.47x10^{-5} /MPa [36] for a CMOS process used by the authors. The resistance change due to strain change is determined by the change in axial stress

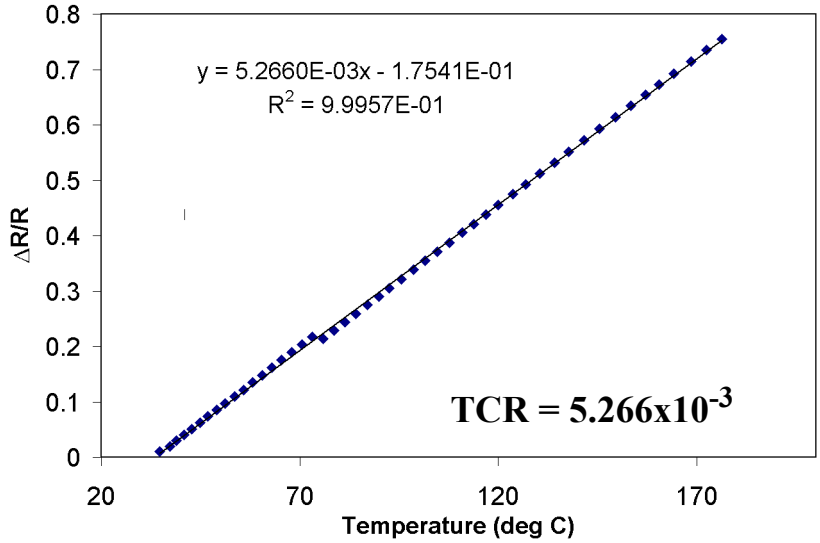


Figure 2.13 Variation of polysilicon resistance with temperature. The temperature coefficient was obtained by a linear fit to be $5.27 \times 10^{-3} K^{-1}$.

per unit increase in temperature, $\Delta\varepsilon = E_{poly}\alpha_{eff}$. For a polysilicon layer embedded in a beam containing metals 1, 2, and 3 (M123P), that has an effective TCE of 8.7 x 10^{-3} /K, the resistance of the polysilicon in a cantilever would decrease as $E_{poly}\alpha_{eff}\pi_p = 6.09 \times 10^{-5}$ per degree of temperature. This is small compared to change in resistance due to the temperature change (5.23 x 10^{-3} /K). The contribution to the piezoresistive coefficient to resistance increase for a CMOS metal 1, 2, and 3 beam is less than 1% of that due to the TCR. The piezoresistive effect has therefore been neglected in the measurement of TCR of polysilicon.

The TCR of the polysilicon was measured for every run that was fabricated to account for the differences in manufacturing. The resistance of an on-chip polysilicon resistor was measured by a four probe test structure with very small current input. This was done to minimize the error introduced due to self-heating. The chip was placed in a temperature-controlled oven. The temperature of the oven was assumed to be the temperature of the chip. The variation of resistance of a polysilicon heater with temperature is linear within the temperatures of interest. The variation of the resistance with temperature change is shown in Figure 2.13. The TCR value ranges from 4.8×10^{3} K^{-1} to 5.5×10^{-3} K^{-1}, for the Agilent 0.5 μm CMOS process. Maximum temperature that CMOS micromachined structures are practically heated is 170^{o}C. Beyond this temperature the aluminum is found to become grainy and the stress values change.

2.7 Automatic Meshing for Finite Element Analysis (FEA) of CMOS Micromachined Structures

FEA is an important tool for the design of MEMS devices. Low-cost, high performance MEMS devices require integrated electronics/MEMS processes, which have led to the development of CMOS micromachining technologies having the additional capability of including multilayer surface micromachined devices. Exploiting such processes for design of electrostatic and thermal actuators and sensors have made FE modeling of such devices very tedious. Device structural optimization is difficult as a new FE model must be constructed for each design iteration. FE modeling experts tend to use heuristics derived from past experience and knowledge of structural features to obtain good FE models. The interdisciplinary nature of MEMS results in limited past meshing experience for most designers. A tool was developed to enable novice designers to make good quality FE models of MEMS devices by replicating the traditional meshing approach [37].

Recent work in FEA of MEMS has used a mixed rigid/elastic formulation [38] in which proof masses are modeled as rigid elements for improved computational efficiency. The automeshing tool detects various MEMS features (such as combs, springs and plate masses) from the layout and meshes them using a rules file. The rules file contains user-defined meshing rules that determine how fine the MEMS feature is meshed. The algorithm is general and can be easily modified for any process and may be applied to improve the initial mesh generation of commercial MEMS FE analysis tools.

The meshing algorithm described has been developed for the high-aspect-ratio CMOS micromachining process developed at CMU [8]. In this process, the microstructural layers can be designed with any of the metal layers as the etch mask, with their thickness being a function of the masking metal layer. The microstructural elements of the system are designed using the same design rules as the CMOS process. The automesher converts this layout directly into a FE model consisting of 20-node brick elements in the universal (UNV) file format compatible with many FE analysis tools.

2.7.1 3D Canonization Algorithm

The multilayer CMOS microstructure is described by a series of masks namely, polysilicon, metal 1, metal 2 and metal 3. The released structure can be represented as the logical OR of the physical metal layers that delineates the overall geometry of the device. This logical layer is

called the *structural* layer. The 3D canonical mesh representation of the structure is a brick mesh with one neighbor at each of its faces. The following algorithm can be used to create the 3D canonical mesh representation [41]:

1. Read layer information from input file in the Caltech Interchange Format (CIF) (Figure 2.14a).
2. The *structural* layer is created by merging the metal layers, to obtain the geometry of the structure that is defined after etching. Feature detection of beams, masses, springs (meander, crab-leg, folded flexure) and comb fingers is accomplished from rectangles in this layer using algorithms in [39][40]. Every rectangle contained within the component is annotated as being one of the above.
3. Each CIF layer is represented by its 2D canonical form, which is made up of rectangles such that each rectangle has only one neighbor per edge. This can be easily achieved by extending the boundary edges into the interior of the layout area until it meets another boundary edge. Figure 2.14b is the canonical representation of the input layers [40].
4. The MEM or the mechanical layer is created by first copying the structural layer. Every rectangle in the MEM layer is further partitioned by each of the 2D canonized rectangles from each of the layers in Step 3. The MEM layer is illustrated in Figure 2.14c. It represents a surface mesh, that when extruded through all the layers present, would yield a minimal mesh or the 3D canonical mesh representation of the structure, as shown Figure 2.14d. At this point we have the minimal 3D brick mesh required to model the device. This mesh is refined by rules described in a user-supplied rules file as described in the next section.
5. Once the mesh refinement process is completed, the finite element model is constructed from the MEM layer by extruding every rectangle through the structure thickness depending on the mask layer information. The dielectric layers of the CMOS micromachined beam are also extruded during this operation.

2.7.2 Mesh Refinement

The 3D canonical structural mesh is refined by rules supplied by the user, who defines the meshing rules for each type of component that can be detected by the detection algorithm. We define beams and plate masses as the basic elements for surface micromachined MEMS structures. Beams are released structures that are connected either at one or two ends to the rest of the structure or the anchor. Components such as crab-leg springs, folded-flexure springs and

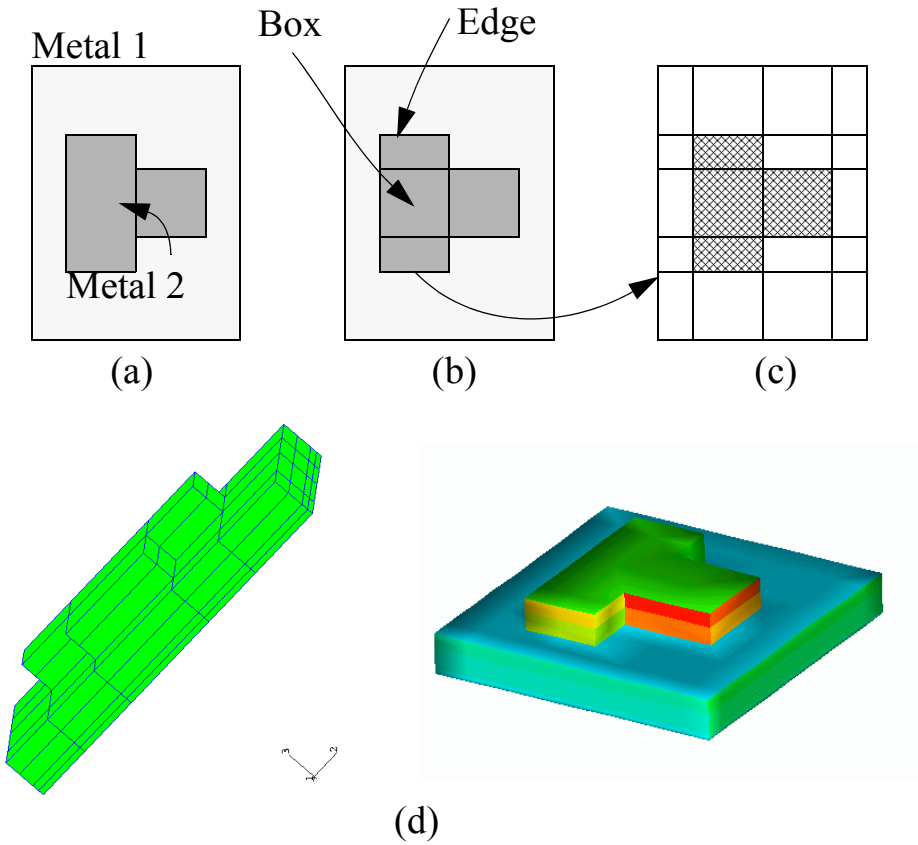


Figure 2.14 An illustration of the 3D canonization algorithm (a) CIF layout of metal 1 and metal 2 microstructure. (b) 2D canonical representation of the metal layers. (c) MEM layer created by splitting every rectangle in one layer with edges of the metal 1 and metal 2 layers. (d) The extruded mesh from the MEM layer.

comb drives can be decomposed into beam elements [39]. For each component the meshing rules are determined by the beam aspect ratio, which is the ratio of the beam length to width. For example, a rules file may be defined as follows:

```
general
    beam aspect < 10 LW=100 Split=1
    beam aspect < 20 LW=4 Split=2
mass X=3 Y=3
comb
    beam aspect < 100 LW=50 Split=1
spring crab
    beam aspect < 5 LW=1 Split=1
    beam aspect < 10 LW=2 Split=1
spring foldedflexure
    beam aspect < 10 LW=10 Split=1
    beam aspect < 20 LW=20 Split=2
spring meander
    beam aspect < 4 LW=3 Split=2
    beam aspect < 7 LW=5 Split=2
```

The rules file describes the meshing rules for unrecognized structures (general), plate masses, crab-leg, folded-flexure and meander springs. For example, crab-leg springs that have beams with

aspect ratio greater than 5 but less than 10 would be meshed such that the aspect ratio of each finite element (LW) would be 2. “Split=1” defines the number of elements that mesh the beam uniformly across its width. Unrecognized components are treated as simple beams and their meshing rules are separately defined in component class *general*.

Mesh refinement is done by first partitioning the rectangles of the *structural* layer based on the beam mesh refinement rules for that component. The MEM layer is then partitioned with the edge of each rectangle in the modified *structural* layer. The final MEM layer is the surface mesh that is extruded to obtain the final mesh. The extrusion process can be modified to account for non-vertical sidewalls. In the final model, each finite element is a 20-node brick.

2.7.3 Illustrative Examples

The automatic mesh generator is used with different rules files depending on the analysis. For mechanical analysis, the comb fingers can be minimally meshed while spring elements are finely meshed and vice versa for electrostatic analysis. To verify the goodness of the mesh, the solver can be run with a denser mesh by changing the rules file. This process can be continued until the desired accuracy is obtained.

The time to convert from a CIF layout to a UNV file is less than 2 minutes for structures with less than 2000 elements. This compares to several hours, if not days, for manual meshing of similarly complex multilayered structures.

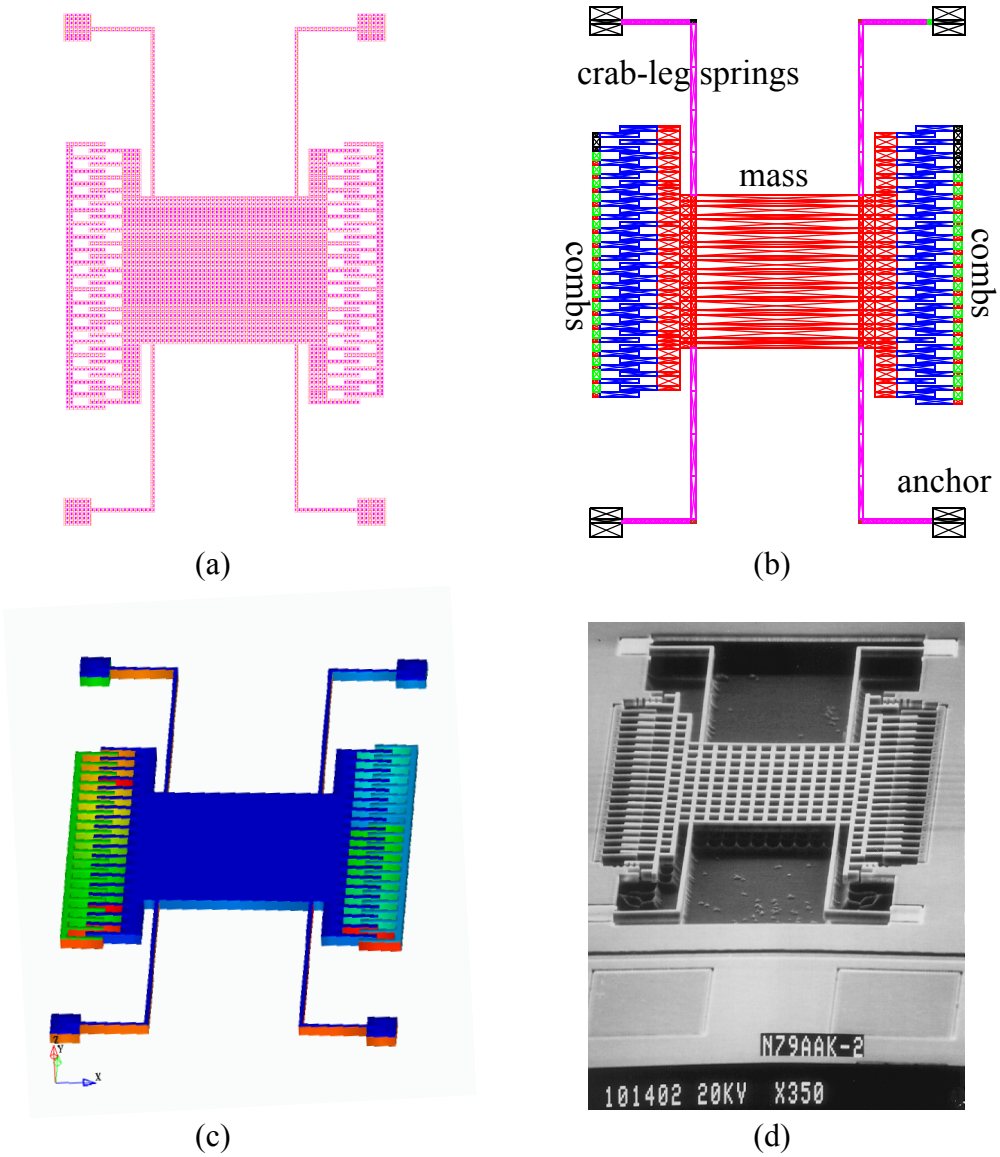
Crab-leg Resonator

The meshing of a crab-leg resonator is illustrated in Figure 2.15. The figure shows the layout of the resonator in standard CMOS using metal and polysilicon layers and intermediate steps of the automeshing process. The component detection algorithm recognizes the crab-leg springs, mass, and comb fingers. Each component is meshed according to rules file defined earlier to generate the FE mesh. Modal analysis using MEMCAD [35] of this structure (3890 elements) yields the first resonant frequency at 49.96 kHz. When the LW of the crab leg was doubled (4120 elements) the resonant frequency was 49.83 kHz. The measured resonant frequency for this structure was 41.53 kHz.

Electrothermal Actuator

Simulation of curling due to residual stress is an important consideration in the design of devices in the CMOS micromachining process. The simulation process is demonstrated for an

electrothermal actuator. The layout of the device with an integrated polysilicon heater is shown in Figure 2.16. The automatic mesher performance for various LW values of the beam element was evaluated by simulation. The meshed structure was evaluated using commercial MEMS FE analysis tools [35]. The results are summarized in Table 2.7 and Figure 2.16. It is observed that the computation time is reduced by a factor of 40 compared to the uniform meshing case with an elemental area of 1 μm by 1 μm. This improvement in computation time arises because the feature recognition identifies the comb fingers and plate masses which are minimally meshed for



(a) (b)

(c) (d)

Figure 2.15 Illustrates the operations performed by the automatic meshing program. (a) Layout of a crab-leg resonator with microstructures defined in Metal 1, 2 and 3. (b) The final MEM layer after feature detection and mesh refinement. Mass, crab-legs, combs and beams components of the comb are detected. (c) The solid model of the resonator in MEMCAD[35]. (d) Scanning electron micrograph of the fabricated crab-leg resonator.

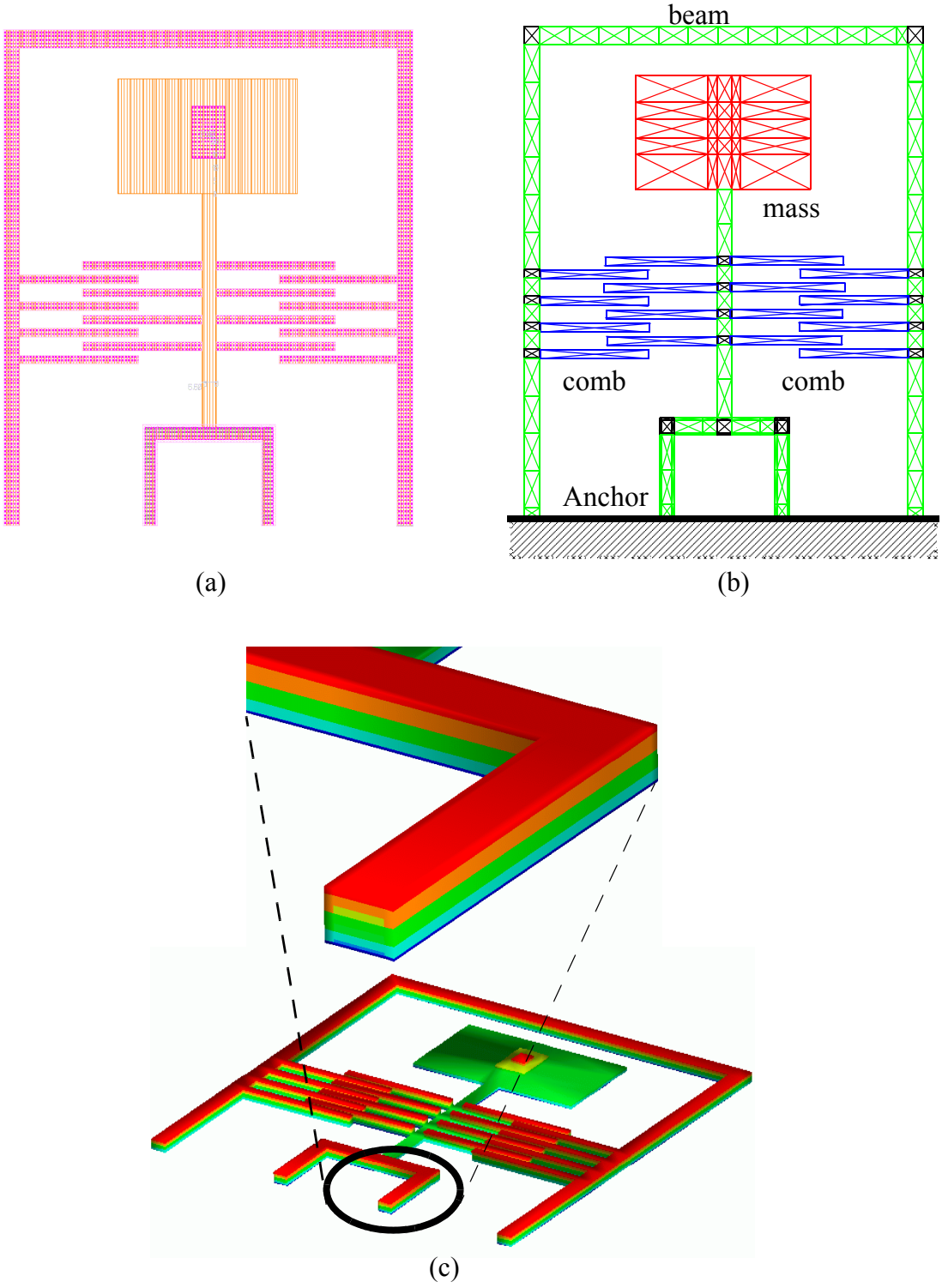


Figure 2.16 Illustrates the simulation of a electro-thermal simulation. (a) Layout of the actuator using the metal and the poly layers of the CMOS process (b) MEM layer with feature detection based mesh refinement. Combs, mass, and the beams are detected separately. The combs are meshed with an L/W ratio of 100 and the beams with a L/W ratio of 2. (c) The solid model of the actuator. Note the metal layers are not of the same width.

Table 2.7: Comparison of thermal FEA of the tip actuator displacements z_{max} with different mesh densities. Comb and plate mass meshing is kept constant.

Element L/W ratio	no. of Elements	Simulation Time (s)	z_{max} (μm)	% Relative Error
UNIFORM	6678	12856.6	32.66	0.00
2	2004	3817.4	32.39	0.83
3	1556	2202.4	32.24	1.28
4	1236	1963.2	31.40	3.85
5	1180	1160.2	31.72	2.87
10	860	869.4	31.54	3.43
20	724	306.06	31.27	4.26

the thermal analysis. This meshing tool was used to determine the optimal curl-matching layout for the comb fingers.

2.8 Conclusion

A methodology for simulation of CMOS micromachined structures using finite element and macromodeling simulators, like NODAS [42][43][44][45] was presented in this chapter. Material properties and their temperature required for accurate thermo-mechanical simulation were measured using test structures, whose temperature can be set using integrated polysilicon resistors. The theoretical analysis introduced in this chapter serves as a basis for the mechanical design of the IR pixel in Chapter 3, and the z-axis temperature compensated accelerometer in Chapter 4 and 5. The lateral curl in CMOS microstructures due to temperature is exploited in the design of the IR imager pixel. The differences in residual stress gradients that cause CMOS micromachined beams to curl depending on their composition, is exploited in the design of the vertical comb drive that is based on a controlled z-offset between the rotor and the stator combs.

Chapter 3. Applications of Thermal Lateral Stress Gradients in CMOS for Infrared Sensing Applications

3.1 Introduction

The human eye can only gather information from the visible light region, with wavelengths in the range of 400 nm to 800 nm, of the electromagnetic spectrum. Imaging in the infrared (IR) region of the spectrum allows one to "see" the small differences in temperature in the environment. This ability is highly useful for surveillance and security applications as it enables detection of objects in absolute darkness. Conventional IR imagers have been used by law enforcement and military agencies. However, this IR imager technology relies on semiconductor sensors, which are expensive and bulky due to the necessary cooling to liquid nitrogen temperatures (77 K)[48]. Newer, uncooled imagers are based on custom materials and are expensive to fabricate.

In this chapter, a CMOS micromachined infrared (IR) sensitive pixel that senses temperature by measuring capacitance change due to lateral motion induced by differences in thermal coefficient of expansion (TCE) of two materials is described. The temperature-induced capacitance change is measured by an on-chip circuit with input D.C. bias feedback and double-correlated sampling. The device is fabricated using a standard 0.5 μm CMOS process followed by a maskless CMOS micromachining process. The dimensions of the pixel sense element are 20 μm x 40 μm. Measured pixel sensitivity is 0.57 mV/K with equivalent temperature noise of 6 mK $\sqrt{Hz}$, corresponding to 0.2 aF/ $\sqrt{Hz}$ of equivalent capacitance noise. An imager architecture consisting of 16x16 pixels has been proposed. This architecture can be expanded easily to a larger array. CMOS imagers compete with traditional CCD cameras for visible light imaging applications due to advantages of cost brought about by the use of standard processing. Similarly,

a CMOS micromachined IR sensitive pixel may lead to cost effective uncooled IR imagers with widespread application.

Newer uncooled infrared imagers consisting of an array of bolometers, and ferroelectric devices are commercially available [49][50][51]. However, they require custom processes and therefore are expensive, leading to a limited penetration of these IR imagers into the consumer market. Calculations indicate that the proposed pixel could be integrated into an IR imager with less than 50 mK noise equivalent difference temperature (NEΔT) after process enhancements.

A bolometer consists of a suspended plate, thermally isolated from the substrate with an integrated resistor. Vanadium Oxide (VO_x) is commonly used as the resistive material for its high temperature coefficient of resistance (~2%/K). The incident infrared radiation induces a temperature change that is detected by measuring the change in resistance. The devices are limited by the flicker noise in the sense resistor. The design requires a low electrical resistance connection between the sense resistor and the external circuits, while maintaining high thermal isolation. This leads to trade-off in the design of the thermal isolation, while maintaining a small pixel size. The ferroelectric uncooled detectors developed by Texas Instruments use an array of devices whose polarization and dielectric constants change with temperature, resulting in charge on a capacitor as the scene temperature varies [52]. The material used for the detector is a 25-75 μm thick ceramic - barium strontium titanate (BST). The main drawback of this device is that the scene input needs to be AC coupled using a mechanical chopper. Moreover, the performance of the imager depends on the ability to produce good quality BST thin films, which are difficult to manufacture with good yields.

Several other approaches have been proposed for IR sensing [48]. Suspended CMOS transistors, whose threshold voltage is a function of temperature using a novel current balancing circuits was proposed in [54]. The minimum detectable temperature difference with this approach is limited by the 1/f noise of the transistors.

Another CMOS based imager uses a n+ polysilicon and gold thermocouple to measure the temperature difference between the pixel and the substrate. The pixel size of this approach is limited by the need for a large area for the thermopiles[55][56][57].

A 16 x 16 array of pyroelectric detectors using a poly-vinylidene flouride (PVDF) film deposited on CMOS has been demonstrated by Binne et al. [58]. This approach requires an external mechanical chopper for operation for charge measurement and has a large pixel size.

Sarnoff research center [59][60] is working on a pixel design based on sensing of capacitance change due to motion induced by infrared radiation onto a plate suspended by a bimetallic element from the substrate. The capacitance change between the substrate and the plate is proportional to the incident radiation, and is measured by circuits that are fabricated on the silicon below the device. The thermal isolation is designed using SiC, and the electrical contact to the sense circuits is made by a thin layer of aluminum. The control of residual stress in the bi-metal is a challenge with this approach. Residual stress gradients can cause the structure to either stick to the substrate, or produce a very large gap between the substrate and the plate. These problems makes the device difficult to manufacture.

In the present work, we exploit the lateral thermo-mechanical motion and capacitance change for IR sensing [61], in contrast to vertical motion. The pixel rejects common-mode mechanical effects such as unwanted spurious lateral and vertical external forces, and the consequent resonant oscillations. The residual stress gradients of the CMOS process are exploited to improve the performance of the device. Each pixel consists of a spring connected to a parallel-plate capacitance sensor. Each spring is a micro-mechanical bimetallic strip that responds to a change in pixel temperature and deflects laterally. This deflection changes the capacitance, which is then detected by on-chip circuitry. The novel features of this device include the utilization of lateral thermo-mechanical motion [19] for temperature sensing, the implementation in CMOS and the pixel thermal isolation techniques. It should be noted that the performance of this device is not limited by *1/f* noise of the sensing mechanism, unlike some other techniques for IR sensing. The

Table 3.1: Comparison of the IR imager pixel reported in literature.

	Wood [50]	**Hanson et al. [52]**	**Lui et al [54]**	**Baer et al [55]**	**Binnie et al [58]**
Principle	bolometer	Ferroelectric	Active heat-balancing	Thermopile	Pyroelectric
Process	Custom	Custom	CMOS	CMOS	CMOS
Pixel size	50μm x 50μm	50μm x 50μm	100μmx100μm	250μmx250μm	105μm x 105μm
Bandwidth	30 Hz	30	30	NA	30
Noise Equivalent Power	30×10^{-12} W/$\sqrt{Hz}$	NA	300×10^{-12} W/$\sqrt{Hz}$	330×10^{-12} W/$\sqrt{Hz}$	2.4×10^{-11} W/$\sqrt{Hz}$
Detectivity	5×10^{8}	NA	3×10^{7}	7.7×10^{7}	4.4×10^{8}
NEDT	25mK	100mK	NA	320mK	NA

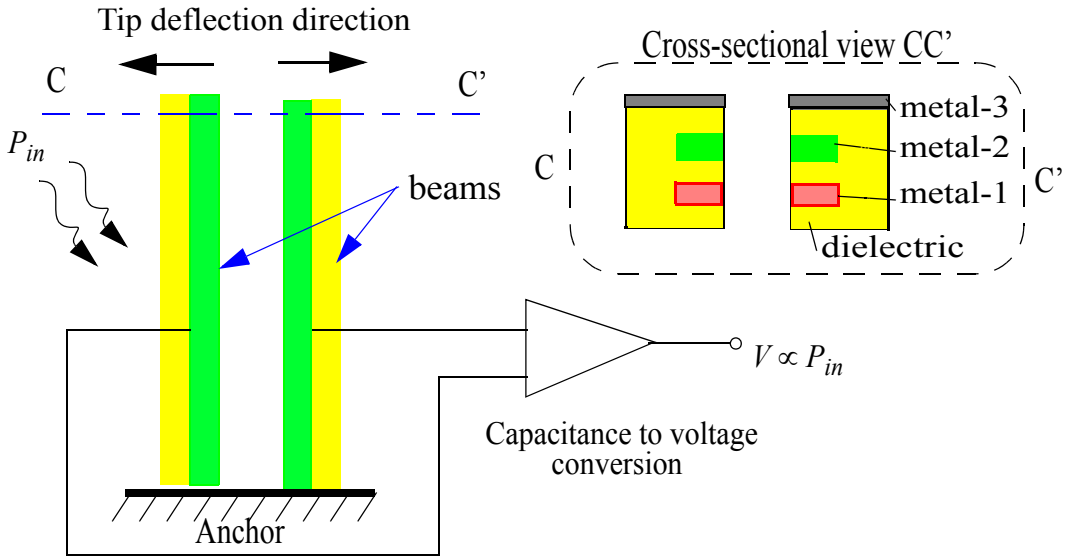


Figure 3.1 Schematic of the pixel operation. Temperature change induces a lateral deflection that is measured as a capacitance change.

1/f noise due to capacitance sense circuits can be reduced by correlated double sampling techniques.

3.2 Operating Principle

To illustrate the operating principle of the IR pixel, consider two adjacent CMOS micromachined beams that have embedded metal-1 and metal-2 layers intentionally aligned to the right and left sides, as shown in Figure 3.1. The TCE of aluminum (23μ /K) is much larger than that of the CMOS inter-layer dielectric (0.4 μ/K). When a temperature change is induced in the beams due to incident IR, a lateral internal bending moment is produced, causing the beam to bend. The beam bending is proportional to difference in the TCE of aluminum and inter-layer dielectric. The lateral motion increases the inter-beam separation and decreases the capacitance between the beams. This change in capacitance is measured by integrated CMOS circuits.

Each imager pixel has four important parts as illustrated in Figure 3.2:

1. The *spring* is designed using intentionally misaligned metal layers. The spring deflects laterally when there is a temperature change due to the difference in thermal expansion coefficients of the metal and dielectric. The out-of-plane curl of the spring is identical and does not cause any performance degradation.

2. The *interdigitated beam fingers* are connected to the laterally deflecting spring. The gap between the fingers changes with temperature. This produces a capacitance change that is measured by the sense circuits.

Table 3.2: Specifications of an ideal IR pixel

Parameter	Value	Unit
Frame rate	30	s^{-1}
Thermal time constant	10	ms
IR spectral band	1-100	μm
Fill Factor	100%	
Pixel Area	625	μm^2
F number of lens	1	

3. The capacitance change in the pixel is measured by an *on-chip CMOS amplifier*. This amplifier has been implemented as a simple four transistor gain stage, with a single-ended source follower buffer D.C. biased using a diode, followed by a common source amplifier.

4. The *Thermal isolator* connects the spring and the substrate. Its main purpose is to minimize the heat loss from the pixel. The isolator must, however, allow sufficient heat loss to maintain the pixel bandwidth at the video rate of 30 frames per second.

5. Test heater, an integrated polysilicon heater is embedded in the surrounding frame to test the pixel. The heater can be set to adjust the contrast of the imager.

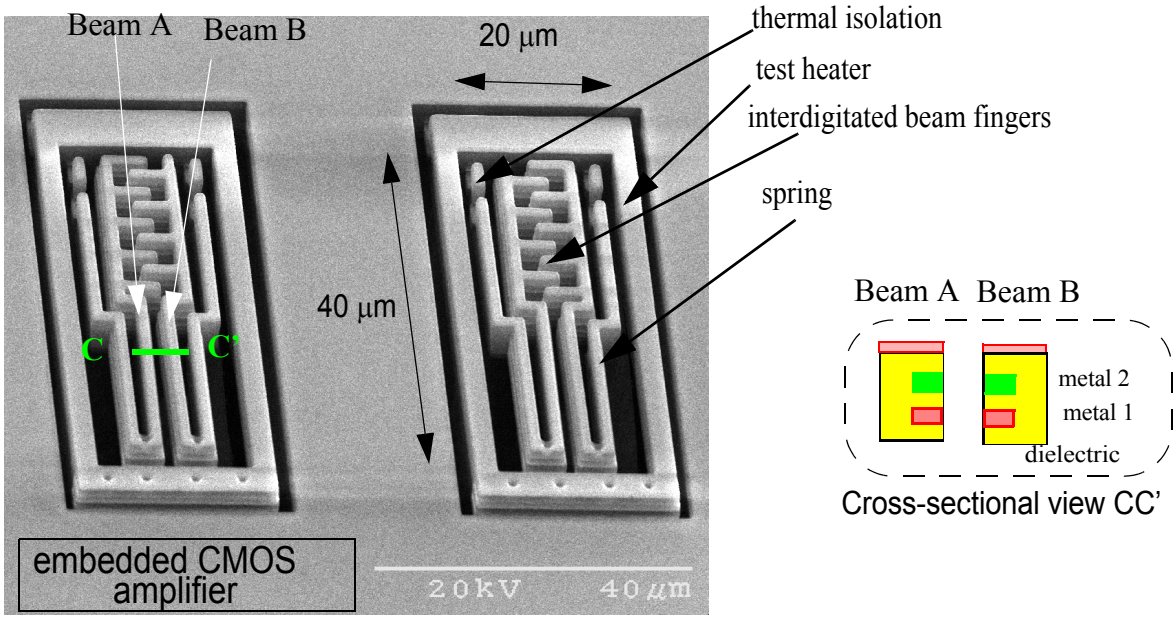


Figure 3.2 SEM micrograph of the fabricated IR pixel with the various parts labeled.

3.2.1 Theoretical Performance Limits of the Infrared Pixel

The desired specifications of an imager are listed in Table 3.2. The thermal equivalent circuit for the pixel is shown in Figure 3.3. This approximate model that helps understand the trade-off in the design of the sensor. The anchor is modeled using a thermal resistance, R_{anc}. The thermal resistance of the spring with the misaligned metal layers is denoted by R_{spring}. The comb drive structure is approximately modeled as a thermal plate, with thermal heat capacity given by C_{th}. The incident radiation from the scene to the device is modeled by a thermal resistance R_{thr}. The heat losses due to radiation from the spring and the comb, are modeled by another thermal resistance, R_{thrp}. The analysis neglects the heat losses due to air conduction from the anchor and the spring, as these devices are normally operated under vacuum.

The anchor and the spring equivalent resistance is expressed as

$$R_{spring} = \frac{L_{spring}}{w_{spring} t_{spring} \kappa_{spring}} \tag{3.1}$$

$$\kappa_{spring} = \frac{\sum_{i=1}^{n} \kappa_i w_i t_i}{\sum_{i=1}^{n} w_i t_i} \tag{3.2}$$

where, L_{spring}, w_{spring}, and κ_{spring} are the total length, width and the effective thermal conductivity of the spring. The effective thermal conductivity of the spring material is the area-weighted average of the beam cross section. The thermal material properties of films used in the CMOS process have been studied in [62][63][22][64], and have been used for these calculations.

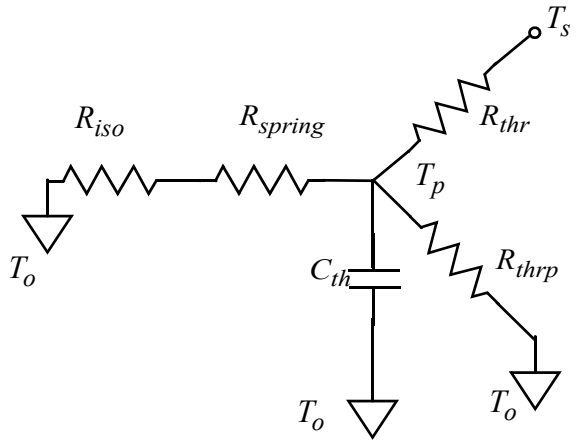


Figure 3.3 Schematic of the thermal equivalent circuit of the IR sensor.

The effective thermal conductivity of the beam designed using metals 1, 2 and 3, with width w, can be expressed as

$$\kappa_{m123} = \frac{(t_{o1}\kappa_{ox} + t_{m1}\kappa_m + t_{o2}\kappa_{ox} + t_{m2}\kappa_m + t_{o3}\kappa_{ox} + t_{m3}\kappa_m)}{(t_{o1} + t_{m1} + t_{o2} + t_{m2} + t_{o3} + t_{m3})} \tag{3.3}$$

where, t_{o1}, t_{o2}, t_{o3} are the thicknesses of the oxide layers and t_{m1}, t_{m2}, t_{m3} are the thicknesses of the metal layers 1, 2 and 3 respectively. Figure 2.6 shows some of the cross sections of the beam, in the CMOS micromachining process. κ_{ox} and κ_m are the thermal conductivities of the oxide and metal (aluminum) respectively. Similarly the thermal isolator equivalent resistance is given by

$$R_{iso} = \frac{L_{iso}}{w_{iso} t_{iso} \kappa_{iso}} \tag{3.4}$$

where, L_{iso}, w_{iso}, t_{iso} and κ_{iso} are the total length, width, thickness and the effective thermal conductivity of the spring respectively. The comb structure is assumed to be at the same temperature and is modeled as a thermal capacitance

$$C_{th} = V_{comb} c_{eff} \tag{3.5}$$

where, c_{eff} is the effective volumetric heat capacity of the comb structure and V_{comb} is the volume of the comb. c_{eff} is calculated as the cross-section-area-weighted mean of the volumetric heat capacity of the comb material.

$$c_{eff} = \frac{(t_{o1}c_{ox} + t_{m1}c_m + t_{o2}c_{ox} + t_{m2}c_m + t_{o3}c_{ox} + t_{m3}c_m)}{(t_{o1} + t_{m1} + t_{o2} + t_{m2} + t_{o3} + t_{m3})} \tag{3.6}$$

where, c_m and c_{ox} are the volumetric heat capacity of the metal and the oxide respectively. The radiation resistance coupling the scene temperature to the device for small temperature differences can be calculated as

$$R_{thr} = \frac{1}{4\varepsilon_p \sigma A_p T_p^{\,3}} \tag{3.7}$$

where, A_p is the area of the exposed device that absorbs the IR radiation, T_p is the temperature of the pixel and ε_p is the emmisivity of the device, given by integration of the Planck's distribution, $E_{b\lambda}$, between the wavelengths of interest (λ_1=8μm to λ_2=18μm).

$$\varepsilon_p = \frac{1}{\sigma T^4} \int_{\lambda_2}^{\lambda_1} E_{b\lambda} \varepsilon_\lambda d\lambda \tag{3.8}$$

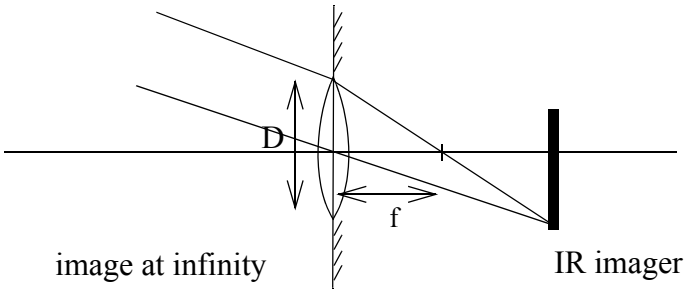
$$E_{b\lambda} = \frac{C_1 \lambda^{-5}}{e^{\frac{C_2}{\lambda T}} - 1} \tag{3.9}$$

where, σ is the Stefans constant (5.669×10^{-8} W-m^{-2}), and C_1=3.743×10^{-16} W-m^2 and C_2=1.438×10^{-2} K-m are constants. The value of $\varepsilon_\lambda = 1$ is used, since the detector is approximated as a perfect black body. The emmisivity of the bottom and the sides of the pixel, ε_s, can be similarly calculated. The calculation of parasitic thermal radiation resistance from the bottom and the sides is similar to (3.7), and is given by

$$R_{thrp} = \frac{1}{4\varepsilon_s \sigma A_b T_p^{\,3}} \tag{3.10}$$

This value is much larger than R_{thr} as $\varepsilon_s << \varepsilon_p$. This is because the top surface of the pixel is coated with an IR absorbing layer, while the bottom and the sides are oxide or metal. The value of ε_s is obtained by integrating (3.8), for all wavelengths. As the device operates in vacuum, air conduction has been neglected. A_b is the area of the back of the pixel. The IR lens focuses the radiation on th the device, and increases the intensity of the pixel by a factor of $4F^2$, where F is the F-number of the lens. F-number of a lens is defined as the ratio of its focal length to its diameter. The use of the IR lens in an imager is illustrated in Figure 3.4. If I_p is the intensity of the IR at the pixel, and I_s is the IR intensity at the scene, then

$$I_p = (2F)^2 I_s \tag{3.11}$$



$$I_S = (2F)^2 I_p$$

$$F = \frac{f}{D}$$

Figure 3.4 Schematic of the IR imager and focussing optics.

as pixel size is reduced, The change in temperature of the device is related to the scene temperature by γ, defined as the change in scene temperature per unit change in device temperature, and is expressed as

$$\gamma = \frac{dT_s}{dT_p} = 4F^2\left(1 + \frac{R_{thr}}{R_{deff}}\right)\left(1 + \frac{\varepsilon_s}{\varepsilon_p}\right) \tag{3.12}$$

where R_{deff} is the total frequency-dependent thermal resistance of the device, given by

$$R_{deff} = \frac{R_{deff0}}{\sqrt{1 + (\omega_{th}\tau_{th})^2}}, \tag{3.13}$$

$$R_{deff0} = \frac{(R_{spring} + R_{anc})R_{thrp}}{R_{spring} + R_{anc} + R_{thrp}}, \tag{3.14}$$

$$\tau_{th} = \frac{1}{R_{deff0}C_{th}} \tag{3.15}$$

τ_{th} is the thermal time constant of the pixel, and ω_{th} is the frequency of the thermal excitation. The spring temperature is assumed to be the same as device temperature, as the thermal resistance of the anchor is much larger than that of the spring. Temperature change in the device induces a lateral deflection causing a change in capacitance, which is seen as voltage change by the measurement electronics. The sensitivity of output voltage with change in device temperature is expressed as

$$S_{v,\,T_d} = \frac{dV_{out}}{dT_d} = \left(\frac{dV_{out}}{dC_d}\right)\left(\frac{dC_d}{dx}\right)\left(\frac{dx}{dT_d}\right) \tag{3.16}$$

where dx is the lateral deflection induced by the temperature change, dC_d is the capacitance change due to the lateral deflection and dV_{out} is the output voltage change. The deflection at the center of the comb is calculated from the dimensions of the spring.

$$dx = \frac{L_{spring}^2}{2\rho_x} \tag{3.17}$$

where, ρ_x is the in-plane radius of curvature of the spring. The temperature dependent deflection of the beam is obtained from (2.15) is given by

$$\frac{\mathrm{d}x}{\mathrm{d}T_d} = \frac{\mathrm{d}}{\mathrm{d}T_d}\left(\frac{L_{spring}^2}{2\rho_x}\right) = \left(\frac{L_{spring}^2}{2}\right)\frac{-\sum_{i=1}^{n}\alpha_i A_i y_{ic} E_i}{\sum_{i=1}^{n} E_i I_{xic}} \cong K_{\rho x}\left(\frac{L_{spring}^2}{2}\right) \tag{3.18}$$

where, α_i is the thermal expansion coefficient of each layer, A_i is the cross-sectional area, and the moment of inertia, I_{xic}, about a line parallel to the x axis and passing through the neutral axis. For simplicity, the cross-sectional and material properties of the spring are included in the constant $K_{\rho x}$. The change in capacitance is approximated by a parallel plate expression,

$$\frac{\mathrm{d}C_d}{\mathrm{d}x} = 2\varepsilon_o n t_{comb}\left(\frac{1}{g} + \frac{w}{x_o^2}\right) \tag{3.19}$$

where, n is the number of fingers of the comb, g is the distance between the fingers, x_o is the initial separation of the two combs, determined by the residual stress gradients when the device is released, and t_{comb} is the thickness of the beam of the comb structure. The schematic of the comb fingers is shown in Figure 3.5.

The capacitance of the device is measured by a bridge circuit that measures the capacitance change with respect to a fixed reference capacitor as illustrated in Figure 3.6. The sensitivity of the bridge circuit, to change in device capacitance is

$$\frac{\mathrm{d}V_{out}}{\mathrm{d}C_d} = \frac{G_o}{2C_d + C_p}(V_{rp} - V_{rn}) \tag{3.20}$$

where, V_{rp} and V_{rn} are the reference voltages at the device and the reference capacitors respectively. If a chopper stabilization based capacitance detection can be used, then V_{rp} and V_{rn}

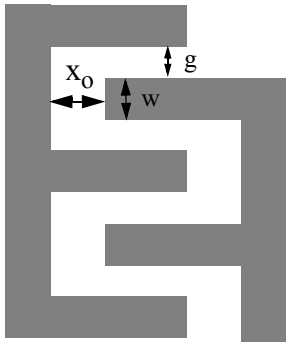


Figure 3.5 Schematic of the comb-drive showing the gap (g), initial separation (x_o) and the width (w) of the finger.

are square wave inputs, at the chopper frequency. C_p is the parasitic capacitance due to interconnect design. G_o is the gain of the external electronics.

From (3.16), (3.18), (3.19) and (3.20), the pixel voltage sensitivity to the device is given as

$$S_{v,\,T_d} = \frac{\mathrm{d}V_{out}}{\mathrm{d}T_d} = \frac{(\varepsilon_o n t_{comb} G_o K_{\rho x} L_{spring}^2)(V_{refp} - V_{refn})\left(\frac{1}{g} + \frac{w}{x_o^2}\right)}{(2C_d + C_p)} \tag{3.21}$$

The responsivity of an infrared detector is a commonly used metric, defined as the output voltage per unit incident power. The incident power on the pixel, ϕ_i, is given by

$$\Delta\phi_i = \frac{\Delta T_d}{R_{deff}} \tag{3.22}$$

and the responsivity can be expressed as

$$\Re = R_{deff} S_{v,\,T_d} = \frac{R_{deff0}(\varepsilon_o n t_{comb} G_o K_{\rho x} L_{spring}^2)(V_{refp} - V_{refn})\left(\frac{1}{g} + \frac{w}{x_o^2}\right)}{(2C_d + C_p)\sqrt{1 + (\omega_{th}\tau_{th})^2}} \tag{3.23}$$

3.2.2 Noise Sources

The noise in uncooled IR imagers is not limited by background-limited infrared performance (BLIP) [65][66], which refers to the noise produced by the scene due to its terrestrial background temperature. Uncooled IR imagers are limited by the noise due to the thermal radiation from the other surrounding pixels, this radiation is much higher than the background radiation from the scene. The dominant noise is therefore modeled by considering the conductive path from the pixel to the substrate, determined by the thermal resistance R_{deff} and parasitic radiation resistance R_{thrp}.

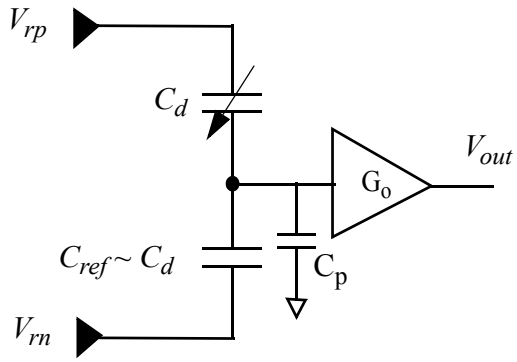


Figure 3.6 Example of a capacitance sense circuit.

The bandwidth of the thermal resistance noise source is limited by the thermal bandwidth, dependent upon heat capacity of the pixel. The noise due to the parasitic radiation resistance is much smaller than that due to the thermal resistance noise and is neglected. The main advantage of capacitance sensing is that there is no inherent 1/f noise in the sense mechanism, if a high enough modulation frequency. The thermal noise power, ϕ_{th}, in the pixel is expressed as

$$\Delta\phi_{th}^{\ 2} = \frac{4k_B T_p \Delta f_{th}}{R_{deff}}, \text{ and} \tag{3.24}$$

$$\Delta f_{th} = \frac{1}{2\pi R_{deff} C_{th}}\left(\frac{\pi}{2}\right) \tag{3.25}$$

where, k_B is the Boltzmann's constant. Δf_{th} is the effective thermal bandwidth of the sensor. The total temperature noise is

$$\Delta T_{th} = \sqrt{\frac{k_B T_p}{C_{th}}} = \sqrt{\frac{k_B T_p R_{deff}}{\tau_{th}}} \tag{3.26}$$

The mechanical Brownian noise can be neglected since the device operates under high vacuum. Quality factors can be expected to as much as 10,000. This is a reasonable estimate, as MEMS resonators proposed for use in communication applications, have Q factors exceeding 100,000 [67]. The dominant natural frequency of the device is high (~ 235kHz) due to its small size.

The capacitance sense circuits also contribute to the noise. The output voltage is typically sensed using a source follower circuit, followed by a correlated double sampling circuit (CDS). If the modulation frequency is sufficiently high compared to the knee of the *1/f* noise, then the noise is white. With careful attention to circuit design, a circuit dominated by the white noise of the input stage transistor can be designed. The sensing is done at a frequency that is much higher than the 1/f knee of the input transistors, as shown in Figure 3.7. The input referred voltage noise of such a circuit be expressed as

$$v_{wn}^2 = 4k_B T_s\left(\frac{2}{3g_{mi}}\right)\Delta f_e = \frac{\frac{8}{3}k_B T_s}{\sqrt{2I_d \mu C_{ox}\frac{W}{L}}}\Delta f_e \tag{3.27}$$

where, g_{mi} is the transconductance of the input MOS transistor, Δf_e is the noise effective bandwidth of the measurement circuits, I_d is the bias current through the input transistor, μ is the mobility of the electron (for n channel MOSFET) or hole (for p channel MOSFET)., C_{ox} is the capacitance of the gate, W is the channel width, and L is the channel length of the transistor. The 3 dB cutoff for the measurement circuit depends on the design of the imager architecture. For the best architecture, it is equal to the frame rate of the imager, typically about 30 Hz. For the 16 x 16 pixel architecture, it is 480 Hz. The circuit noise can be minimized at the expense of higher bias current (I_d), and the size of the transistor (W/L). A larger transistor area also helps to reduce the flicker noise in the transistor.

The circuit noise can be converted to an equivalent scene temperature noise using the conversion factor in (3.21). The total root mean square temperature noise of the pixel is the sum of the circuit noise, expressed a device noise temperature and the noise obtained from the sensor. The total noise of the device, expressed as a device temperature noise is

$$T_{dn}^2 = \frac{8k_B T_s \Delta f_e}{S_{v,\,T_d}^2 \sqrt{18 I_d \mu C_{ox} \frac{W}{L}}} + \frac{k_B T_p}{C_{th}} \tag{3.28}$$

The device noise temperature is expressed as an equivalent scene temperature noise, using (3.12).

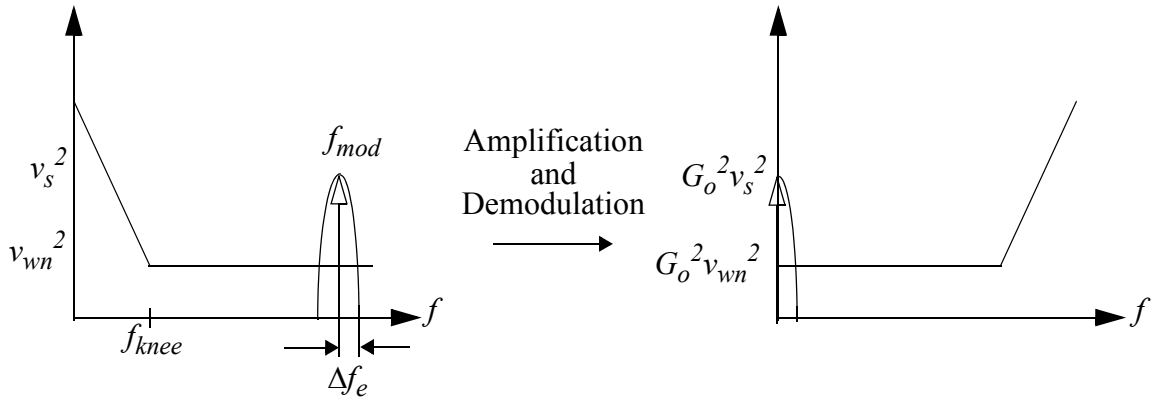


Figure 3.7 Illustration of the improvement in signal noise ratio achieved by chopper stabilization, or correlated double sampling, (a) Output of the preamplifier, when the modulation frequency is much higher than the knee of the 1/f noise. (b) The circuit output after amplification and demodulation. The signal is moved back to the base-band. The 1/f noise is eliminated by a low pass filter, with a cut-off frequency equal to the signal bandwidth. The final signal to noise ratio is limited by the white noise of the preamplifier.

$$T_{sn}^2 = \gamma^2 T_{dn}^2 = \gamma^2 \left(\frac{8k_B T_s \Delta f_e}{S_{v,T_d}^2 \sqrt{18 I_d \mu C_{ox} \frac{W}{L}}} + \frac{k_B T_p}{C_{th}} \right) \text{K}^2 \quad (3.29)$$

The total noise equivalent power of an IR detector is defined as the total noise power incident on the device, per unit area, and is expressed as

$$NEP = \frac{T_{sn}}{R_{deff}} = \frac{\gamma}{R_{deff0}} \sqrt{\left(\frac{8k_B T_s \Delta f_e}{S_{v,T_d}^2 \sqrt{18 I_d \mu C_{ox} \frac{W}{L}}} + \frac{k_B T_p}{C_{th}} \right) (1 + (\omega_{th} \tau_{th})^2)} \quad \text{nW} \quad (3.30)$$

For our imager pixel this value is calculated to be 4.2 nW. The normalized detectivity of the imager is defined as

$$D' = \frac{\sqrt{A_d \Delta f_e}}{NEP} = \frac{R_{deff0}}{\gamma} \sqrt{\frac{A_d}{\left(\frac{8k_B T_s}{S_{v,T_d}^2 \sqrt{18 I_d \mu C_{ox} \frac{W}{L}}} + \frac{k_B T_p}{\Delta f_e C_{th}} \right) (1 + (\omega_{th} \tau_{th})^2)}} \ \text{m}\sqrt{Hz}/\text{W} \quad (3.31)$$

This value is 7.04 x 10^5 cm$\sqrt{Hz}$/W, for the imager pixel. The performance of an IR imager is measured as a noise equivalent difference temperature (NEΔT). NEΔT is the crucial measure of the detectors performance; it is essentially the output noise to signal ratio. The NEΔT for the pixel is expressed as

$$NE\Delta T = 8F^2 \left(1 + \frac{R_{thr}}{R_{deff}}\right) \left(1 + \frac{\varepsilon_s}{\varepsilon_p}\right) \sqrt{\frac{2k_B T_s (2C_d + C_p) \Delta f_e}{\left(\varepsilon_o n t_{comb} G_o K \rho x L_{spring}^2\right) (V_{refp} - V_{refn}) \left(\frac{1}{g} + \frac{w}{x_o^2}\right) \sqrt{18 I_d \mu C_{ox} \frac{W}{L}}} + \frac{k_B T_p R_{deff}}{\tau_{th}}} \ \text{K} \quad (3.32)$$

The theoretical limit of the IR pixel is calculated using the above expression to be 6 mK. This expression is useful for optimization of the device geometry and thermal design. It is clear that for best performance, it is necessary to

- maximize the emmisivity of the pixel. This can accomplished by coating the pixel with gold or platinum black.
- minimize the emmisivity of the back and sides of the pixel. Quarter wavelength resonant cavities between the device and the substrate have been proposed in literature [51] for minimization of radiation losses from the bottom of the pixel.

- maximize the thermal isolation provided by the anchor. Oxide bridges with polysilicon conducting wire can be used.
- minimize thermal radiation resistance (R_{thr}) from the scene to the device. This can be achieved by increasing the detector area.
- lens with the highest F-number should be used.

Note that the NEΔT of an imager is not determined by how sensitive the sense mechanism is, but ultimately by the thermal isolation of the pixel. A high sensitivity just helps to lower the circuit noise and make the ultimate performance more achievable. A higher thermal isolation will increase the inherent device noise, but will reduce γ. The pixel design will be optimal when the contribution from the device noise is equal to that of the circuits. Table 3.3 summarizes the theoretical performance limit of the imager.

3.3 Pixel Design

To demonstrate the working principle of the proposed IR imaging pixel, a design was proposed that optimizes performance in the CMOS micromachining process. A test chip was fabricated using the Agilent 0.5μm CMOS process [34].

3.3.1 Mechanical Design

The main constraint for the design of the pixel was the minimization of the device area, while achieving the maximum capacitance change due to thermal motion. The device area was minimized to maximize the number of pixels that could be placed economically on a single chip. The geometry of the pixel, shown in Figure 3.2, was designed for maximum sensitivity through manual iteration of the simulated response. A meandering spring design with the beam cross-section similar to that shown in Figure 3.1 is used to maximize the tip deflection within the pixel area. The thermally induced lateral bending of the meandering spring is similar to that of a single long beam. The tip of the meandering spring is populated with interdigitated fingers to maximize the capacitance change. The differences in residual stresses in the embedded layers cause the comb fingers to move closer together after the mechanical release from the substrate. This leads to gaps that are smaller than the design rules of the process, thereby improving device sensitivity. The use of interdigitated comb fingers is better than as single parallel plate as the deflection of the beams is angular. The lateral bending produces an angular motion, resulting in a tip motion that is larger than that at the bottom part of the beam. The used of comb fingers results in a better overall

Table 3.3: Summary of the ultimate performance of the Imager

Symbol	Parameter	Value	Units
L_{comb}	Comb length	20	μm
L_{spring}	Total spring length	44	μm
W	Finger width	1.8	μm
g	Finger gap	1.2	μm
x_o	Post release gap	0.5	μm
L_{iso}	Thermal isolator length	15	μm
-	Top metal thickness thermal isolator	0.0	μm
-	Top metal thickness sensor area	0.5	μm
R_{deff}	Effective device thermal resistance	3.31×10^{6}	sK/J
C_{th}	Thermal heat capacity	4.25×10^{-9}	J/K
τ_{th}	Thermal time constant	13	ms
ε_p	Emmisivity (top)	1	-
ε_s	Emmisivity (bottom)	0	-
R_{thr}	Radiation coupling resistance	3.75×10^{8}	J/K
F	Lens F number	1	-
γ	dT_s/dT_d	458	-
C_o	Sensor Capacitance	33.27	fF
dC_o/dT_d	Capacitance sensitivity	3.02	aF
dV_{out}/dT_d	Voltage sensitivity (Analytical)	2.07	mV/K/V
dV_{out}/dT_d	Voltage sensitivity (FEM)	2.03	mV/K/V
T_p	Photon noise (device referred)	0.144	$\mu K/\sqrt{Hz}$
T_{ckt}	Amplifier noise (device referred)	0.896	$\mu K/\sqrt{Hz}$
NEP	Noise Equivalent Power	4.02	nW
D'	Normalized Detectivity	7.04×10^{5}	$cm\sqrt{Hz}/W$
NEΔT	Noise Equivalent Difference Temperature	6.08	mK

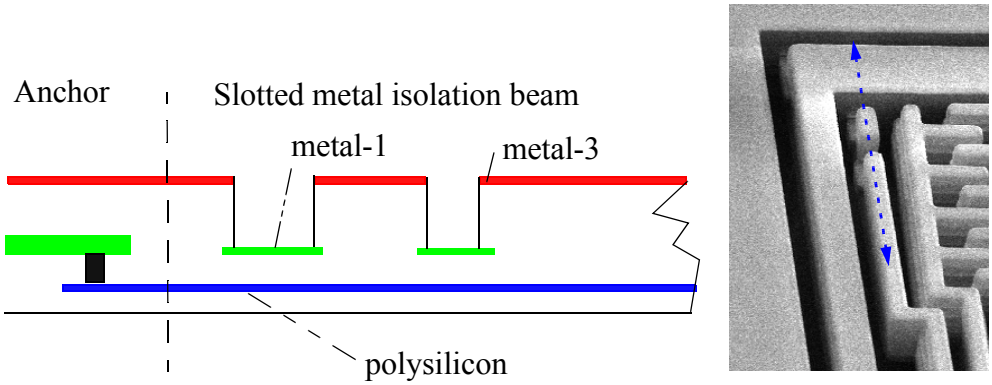


Figure 3.8 Cross-section along the length of the thermal isolation beam as shown in SEM.

sensitivity. Finite element simulations indicate the nominal sense capacitance to be 4 fF after pixel self biasing due to residual stress, and the device sensitivity to be 40 aF/K.

Design of the thermal isolation between the device and the substrate is critical in IR sensor design to improve the NEΔT. The cross-section along the length of the thermal isolation beam is shown in Figure 3.8. To minimize thermal conductance, the thermal isolation beam has slotted metal lines, and electrical contact from the comb to the circuits is made by minimum width (0.6 μm) polysilicon interconnect. The higher electrical resistance of the interconnect does not pose limitations to the device performance unlike bolometers. The oxide beam is covered by thin metal layer that can be removed by a later post-CMOS processing step. This metal removal was not performed in the tested devices.

The right and the left parts of the device are not designed identically, resulting in different mechanical resonances for each side. This helps reject spurious mechanical oscillations of the device that affect device performance in high vacuum since the beat frequency is out of the signal band. Another concern in micromachined IR pixels is the sensitivity to external accelerations. External accelerations affect the right and the left parts of the pixel and very little relative motion between the pixel is observed. The acceleration sensitivity of the pixel has been simulated and the results are summarized in Table 3.4

Table 3.4: Finite element results of acceleration sensitivity of Pixel for 1 G input

Direction	x	y	z
Pixel displacement per G (m/G)	2.96×10^{-13}	1.19×10^{-13}	4.88×10^{-13}
Equivalent pixel temperature change (μK/G)	2.84	0.114	0.469

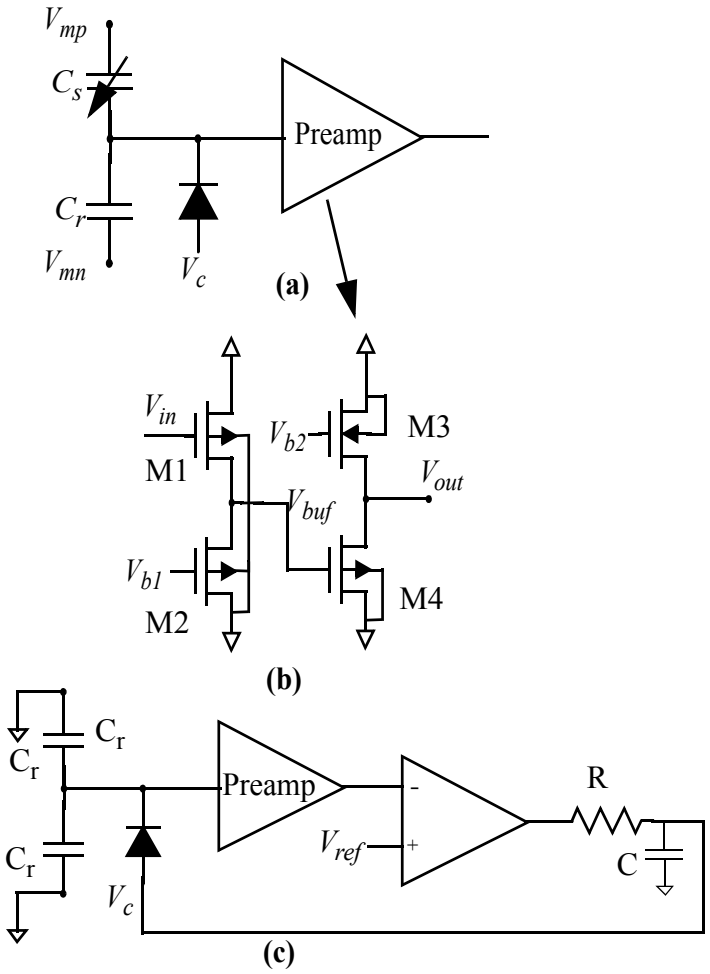


Figure 3.9 Schematic of the pixel capacitance sense circuit. (a) The diode biased capacitance sense circuit. (b) Schematic for the preamp circuit. (c) The replica bias circuit that sets the diode D.C. voltage, V_c.

3.3.2 Interface CMOS Circuit Design

The capacitance sense circuit for the pixel uses correlated-double sampling to reduce *1/f* noise and feed-through. The schematic of the sense circuit is shown in Figure 3.9. The first stage is a source follower to minimize input parasitics. The gain is provided by a common-source amplifier. The D.C. bias at the input is set by a reverse-biased diode. The value of the D.C. bias voltage is determined by a replica biasing circuit such that the output voltage is centered. The replica bias circuit is designed identical to the actual device except that no modulation voltage is applied. The bandwidth of feedback signal for the D.C bias of the diode is limited by a low-pass frequency. This biasing scheme reduces the effects of D.C. drifts and maximizes the dynamic range. The diode can latch high, which is a potential problem; however, this is prevented in the

measurements by illuminating the diode. The D.C. feedback circuit maintains the output from the common source amplifier within its dynamic range.

Sinosoidal signals, 180 degrees out-of-phase, at a frequency higher than the *1/f* knee of the input MOSFET (M1) are applied to V_{mp} and V_{mn}. The initial mismatch between the pixel and the reference capacitor are corrected by adjusting the relative peak to peak amplitude of V_{refp} and V_{refn}. The initial offset voltage due to capacitance mismatch is reduced to zero when,

$$C_d V_{refp} = C_r V_{refn} \tag{3.33}$$

The output of the preamplifier circuit is demodulated using analog multipliers off-chip to obtain a measure of the pixel capacitance change. Another technique to compensate for capacitance mismatch between pixels is to control electrical sensitivity and consequently, the contrast of the imager, using a polysilicon resistor embedded within the frame surrounding the pixel sense element. The frame is heated by passing current through the resistor. With a suitable array architecture design, the temperature of each pixel can be kept constant independent of the operating temperature using the heaters.

3.4 Experimental Results

The experimental setup for measuring pixel electrical performance was simplified by using Joule heating in the surrounding frame. This method avoids the complexity of an experimental setup with infrared optics and vacuum packaging. The capacitance change as a function of temperature change in the frame was measured. The temperature of the pixel was determined from the resistance of the polysilicon heater. The thermal coefficient of resistivity of the polysilicon heater resistance was obtained by measuring the resistance in a temperature-controlled oven and correcting for the device temperature gradient. The chip temperature was measured using the junction voltage of an on-chip well-substrate diode. The correction for the non-uniform heater temperature was made using a shape factor of the temperature profile obtained by electrothermal modeling [35]. An example temperature distribution due to the heating of the surrounding polysilicon resistor with 1 mA of current is shown in Figure 3.10. Electrical feed-through from the polysilicon heater was eliminated by the use of correlated double sampling.

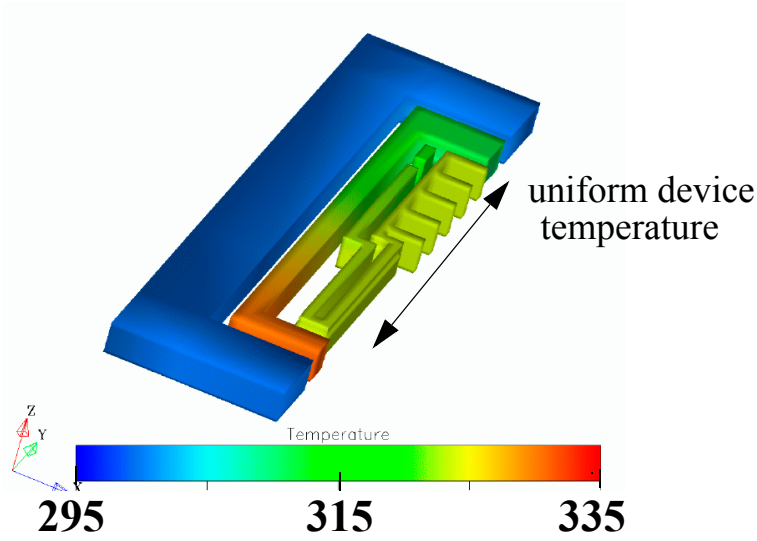


Figure 3.10 Electrothermal finite-element simulation of the temperature distribution in the device in air for an 1 mA polysilicon heater current.

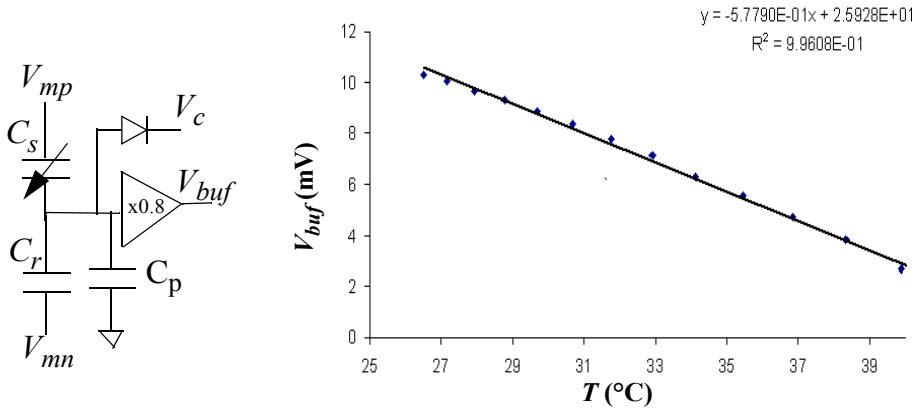


Figure 3.11 The measured buffer output as a function of device temperature produced by the heater.

3.4.1 Electrical Characterization

Data were collected for sampling frequencies ranging from 100 kHz to 2 MHz. The gain of the entire preamp was designed to be 10, with a gain of 0.8 in the first stage buffer. A plot of the output of the capacitive bridge circuit with temperature is shown in Figure 3.11. The temperature sensitivity was 0.29 mV/K/V across the capacitive bridge (without gain) per volt of modulation input. This is better than the 0.207 mV/K/V, and 0.203 mV/K/V expected from hand calculation and FEA respectively. The discrepancy can be explained by the higher positional sensitivity of the fabricated device and the error in estimation of the parasitic capacitor. The value of the parasitic capacitor was obtained using a layout parasitic extractor, of the CMOS process. The spectral output of the sinosoidal heating of the integrated heater with a 25 mV and 30 Hz heater input

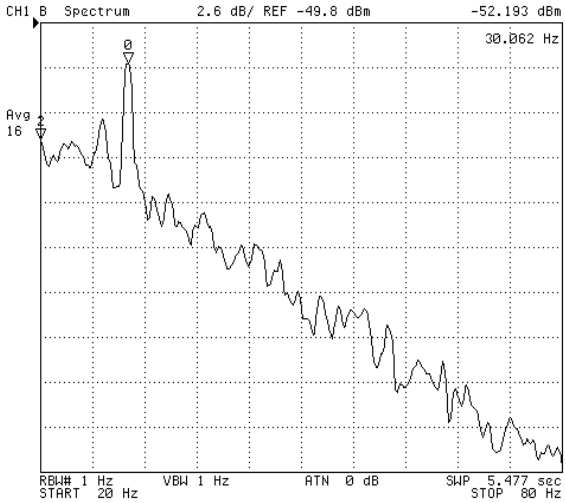


Figure 3.12 Demodulator output for a 25 mV (peak), 30 Hz heater input signal corresponding to a 12 mK peak signal The equivalent temperature noise is 6 mK//*Hz*.A modulation frequency of 95 kHz was used for this measurement.

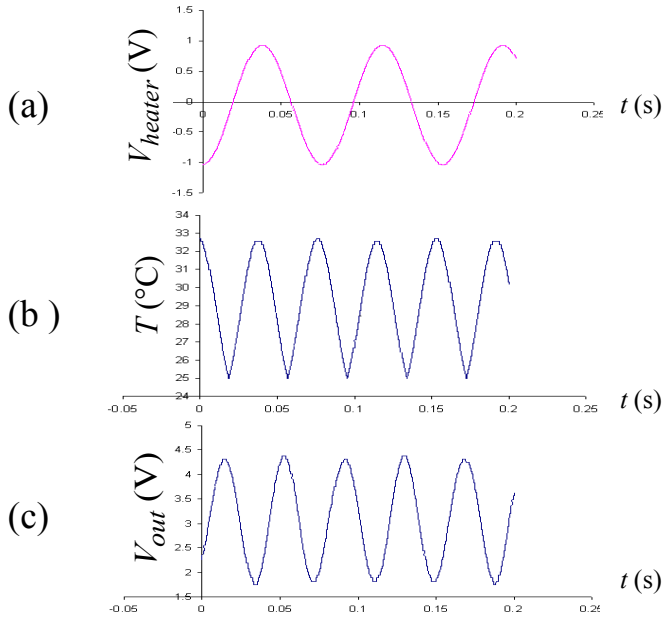


Figure 3.13 Measured transient response of the IR pixel. (a) Voltage applied to the polysilicon heater. (b) Temperature of the pixel. (c) Output of the pixel sense circuit.

signal, corresponding to a 12 mK peak temperature change is shown in Figure 3.12. The noise floor of the pixel was measured to be 6 mK/$\sqrt{Hz}$ after demodulation. This corresponds to 0.2 aF of equivalent capacitance noise measured in a 1 Hz bandwidth. The transient response of the pixel with a sinosoidal temperature change induced by electrical heating is shown in Figure 3.13.

The noise at the output of the demodulator is seen in Figure 3.14. A modulation frequency of 95 kHz was used in this measurement. This frequency is below the knee frequency of the 1/f noise

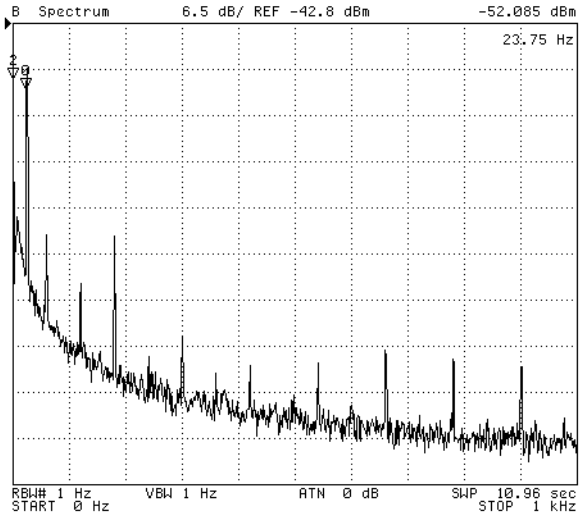


Figure 3.14 The output noise spectrum from the demodulator, for 24 Hz sinosoidal heater input voltage.

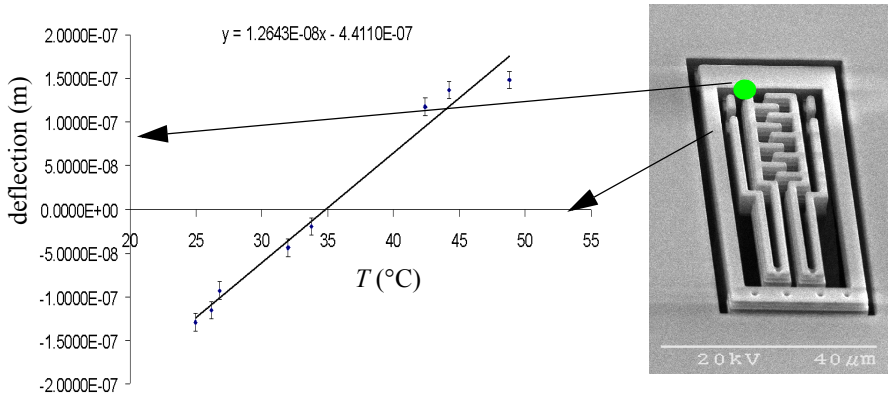


Figure 3.15 Measured pixel tip deflection as a function of temperature produced by integrated heater.

process, and hence, the noise of the pixel is limited by a 1/f noise of the amplifier. The frequency could not increased, due to the limitations of the demodulator.

3.4.2 Mechanical Characterization

The lateral motion sensitivity was measured to be 126 Å/K (Figure 3.15) using the MIT microvision system [27]. Finite-element modeling predicted a lower sensitivity of 104 Å/K. Sidewall etching during the release process yields thinner beams that improve sensitivity. The mask alignment mismatches, during the fabrication process also contribute to sensitivity variations. The mechanical resonant frequency of the right and the left half of the pixel was measured to be 245 kHz and 230 kHz, respectively. The beat frequency due to spurious resonances in both the beams is 15 kHz, which is outside the sense bandwidth of 30 Hz. The device was measured in a vacuum of 1 mT, and no peaks were observed due to low frequency

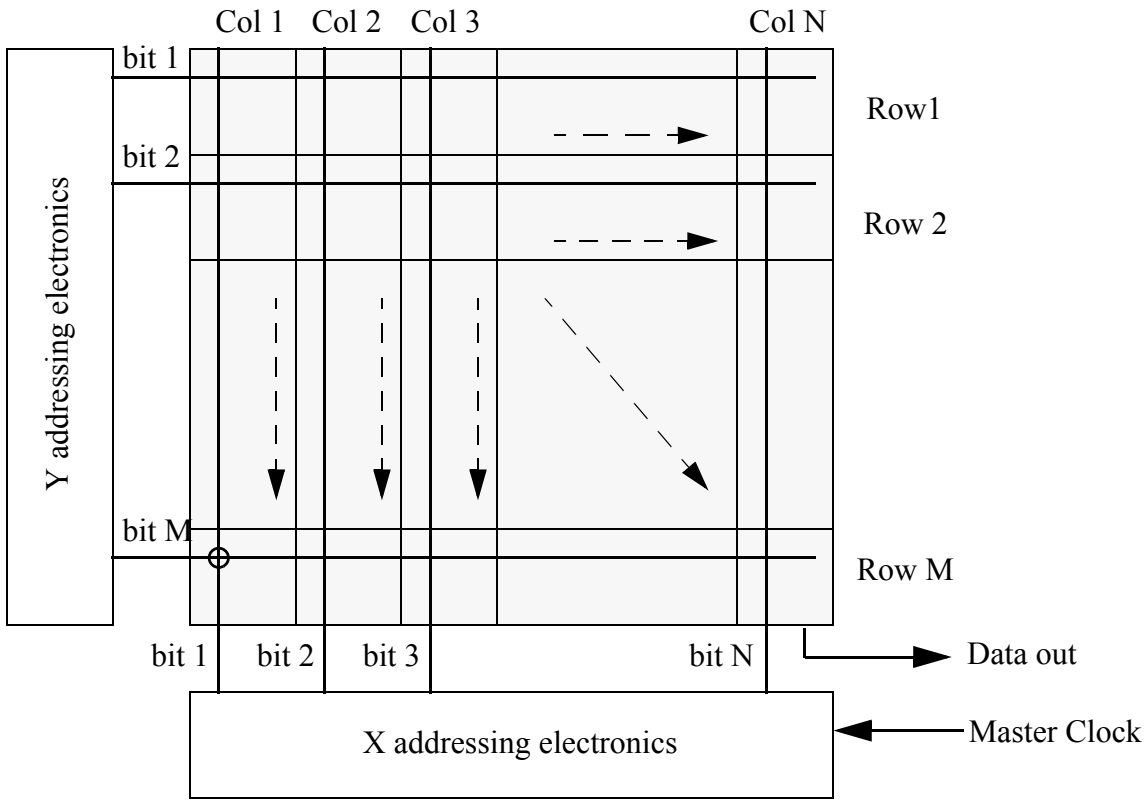


Figure 3.16 Schematic of the XY addressing electronics for the IR image.

electrostatic excitation of the device at the beam resonant frequencies or the beat frequencies. The thermal time constant of the surrounding heater and imager pixel is 2.8 ms.

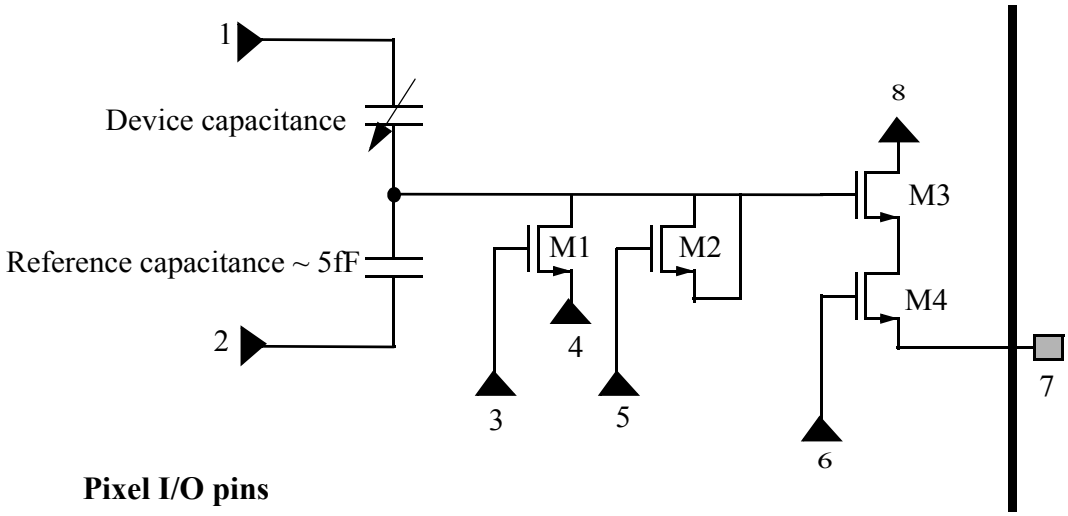
3.5 X-Y Addressing Electronics For The IR Array

For the pixel to be used in a IR imager, X-Y addressing electronics that generate a frame must be designed. The proposed IR imager array consists of N rows and M columns. The pixels are addressed individually by a row and column select electronics, once every image scan. The schematic of the array is shown in Figure 3.16. A pixel in the m-th row and the n-th column is selected when both bit lines M and N are logic high. The bit lines for the X-Y addressing are generated using shift registers and are synchronized by a master clock.

3.5.1 Improved Pixel Circuit Design

The architecture has been designed to minimize the number of transistors placed at every pixel. The signal from each pixel feeds a shared source follower, that is selected when the row select bit is logic high. The schematic of the pixel design is shown in Figure 3.17. All row pixel outputs in a single column are connected together. Since only one row is activated by the Y address generation shift register, no two pixels are ever connected to the common column I/O pin. The capacitance bridge, created by the sensor capacitance and the reference capacitance are

driven by two out-of-phase signals. These signals enable double correlated sampling based capacitor detection. Any initial mismatch between the sensor and the reference capacitance is eliminated by adjusting the ratio between the positive and the negative voltage references. The ratio can adjusted by an external gain control circuit. The reset switches set the D.C. voltage at the output. The switch injection errors are reduced by addition of a dummy compensating switch driven by a delayed and inverted reset signal. Equal and opposite charge is injected by the switching of the dummy transistor to cancel the charge injected during the switching. The diode biasing circuits used in the earlier design were abandoned due to voltage drift problems. The circuit had to illuminated to generate sufficient leakage current in the bias diodes. The mismatches in the replica bias circuit and the actual sense circuits caused the output to drift over time, till it saturated. Without the D.C bias circuit, the voltage drift was not satisfactory.



Pixel I/O pins

I/O pin	Description
1	Vref Positive
2	Vref Negative
3	reset
4	ANALOG GROUND
5	reset compensation
6	Row select
7	Common Column
8	VDD= 5V

Transistor sizing

Transistor	W/L ratio
M1	2.4μm/0.6μm
M2	1.2μm/0.6μm
M3	6μm/0.6μm
M4	4.2μm/0.6μm

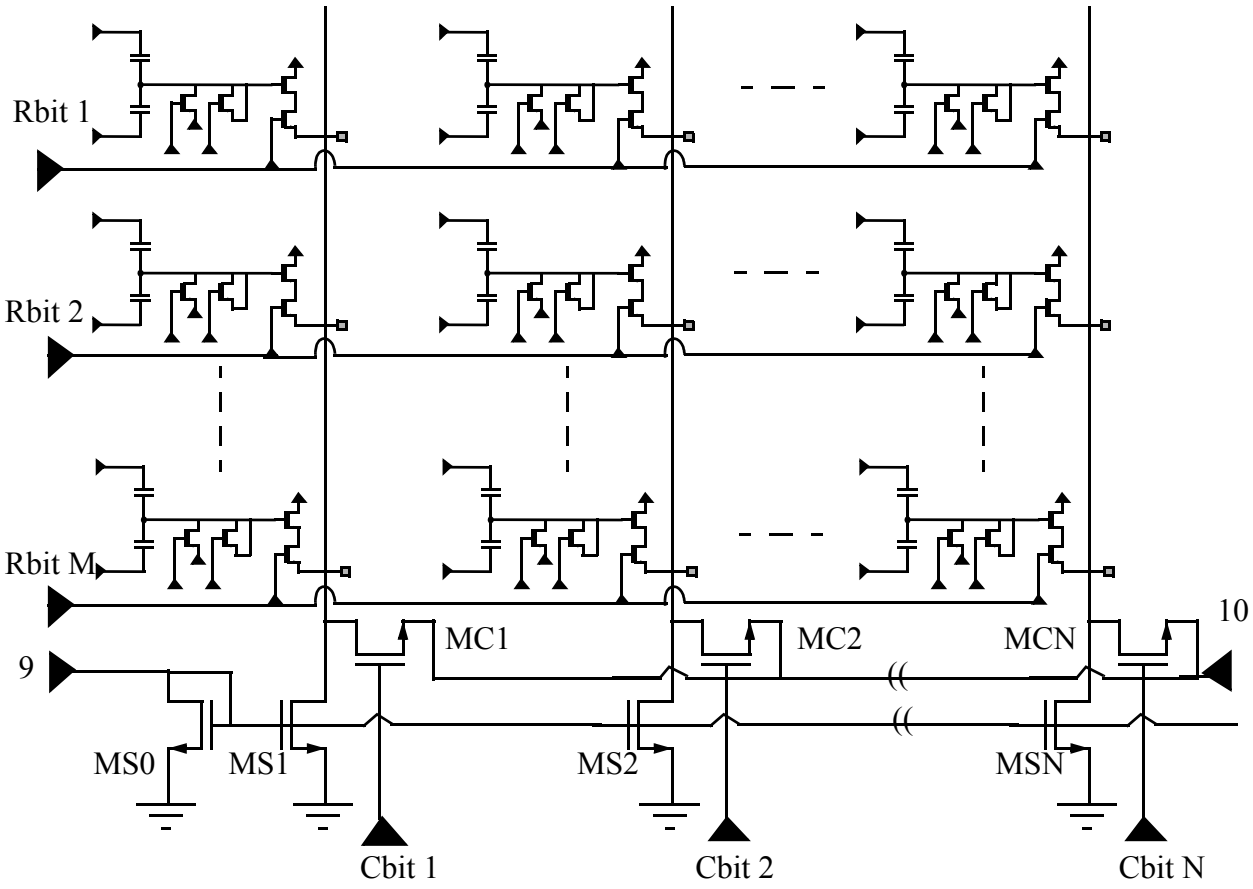
All N channel transistor body terminals are tied to VSS or 0V

Figure 3.17 Circuit per pixel for sensing capacitance change

The detailed schematic of the array circuit is shown Figure 3.18 The active column is selected by a high on the column select bit and an active pixel is selected by a high on the row select lines. The output of the array is a single wire. The correlated double sampling circuit for capacitance measurement is shared by all the pixels.

3.5.2 Clock Scheme

A sample clock scheme for a 2 x 2 pixel is depicted below. The most important waveforms are shown in Figure 3.19. The positive and negative voltage references that are input to the



I/O pin description

I/O pin	Description
9	Bias current input
10	Imager output
Cbit 1-Cbit N	column select bits
Rbit 1-Rbit N	Row select bits

Transistor Sizing

Transistor	W/L ratio
MS0-MSN	10μm/2μm
MC1-MCN	3μm/0.6μm

Figure 3.18 Detailed schematic of pixel addressing electronics

capacitance bridge are analog signal centered about the analog ground voltage. The frequency of the sampling is related to the scan rate of the image. The master clock frequency is obtained by

$$F_{clock} = 2(N)(M)(S)(n) \tag{3.34}$$

where S is the scan rate of the image and n is the number of pixel output measurements made per cycle. For a 16 x 16 array, working at 30 frames per second and 1 measurement per cycle, the master clock frequency would be 15360Hz.

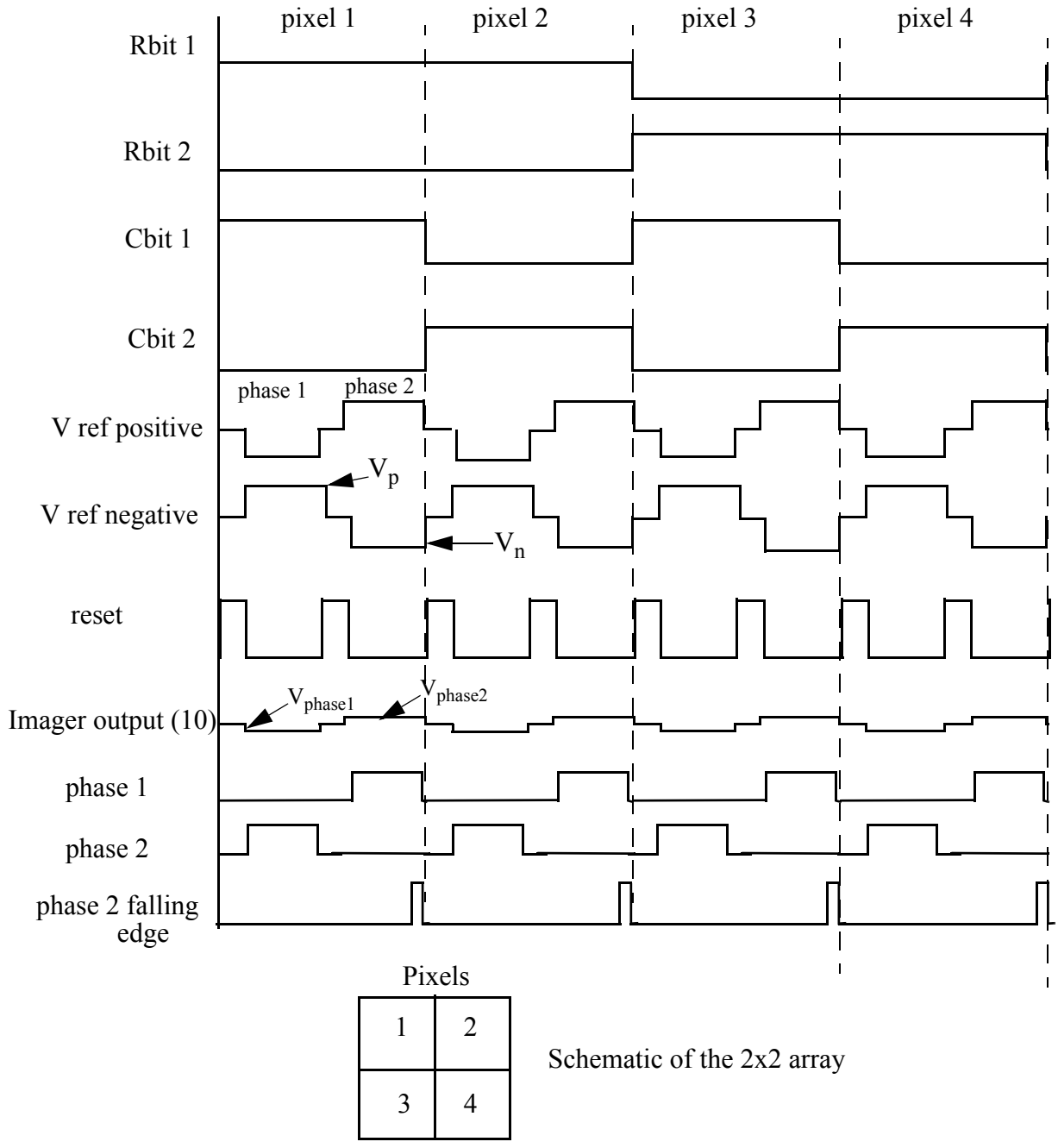


Figure 3.19 The clocking scheme for the 2 bit pixel example.

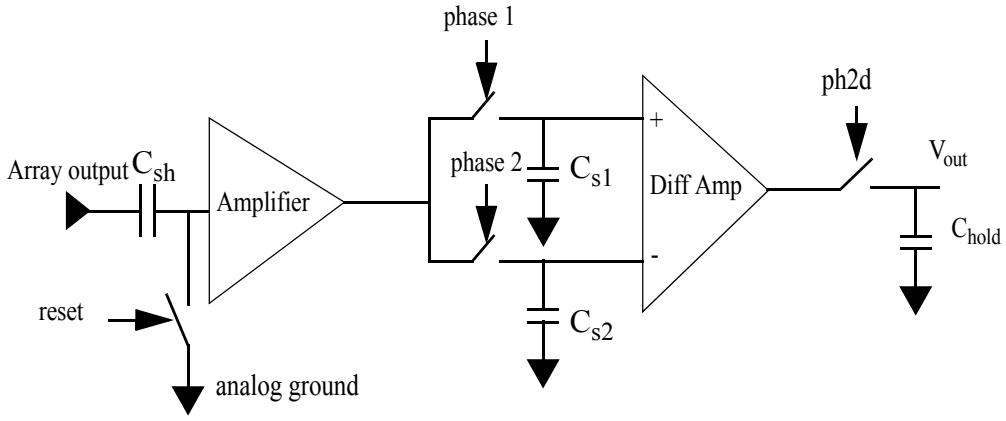


Figure 3.20 Simplified schematic of the circuit to subtract the voltage measured at the two phases. phase 1 and phase 2 are signal that are on during the phase 1 and sample time respectively.

3.5.3 Detection of Capacitance

The output capacitance is converted to a voltage using double correlated sampling. The voltage proportional to the capacitance change is computed by the difference of the samples during the phases of the measurement. The output voltages during the first and second clock phase are

$$V_{phase1} = V_p \frac{C_d}{C_d + C_{ref} + C_p} + V_n \frac{C_{ref}}{C_d + C_{ref} + C_p} \tag{3.35}$$

$$V_{phase2} = V_n \frac{C_d}{C_d + C_{ref} + C_p} + V_p \frac{C_{ref}}{C_d + C_{ref} + C_p} \tag{3.36}$$

The capacitance is computed by a circuit that computes the difference in the two phases.

$$V_{out} = V_{phase1} - V_{phase2} = \frac{(V_p - V_n)(C_d - C_{ref})}{C_d + C_{ref} + C_p} \tag{3.37}$$

The output voltage is proportional to the change in capacitance relative to the reference capacitor. A simple implementation of the circuit is shown in Figure 3.20. The capacitor, C_{sh}, samples the D.C. offset voltage introduced by the source follower on every pixel. The signal is amplified and the output of phase1 and phase2 is sampled on capacitors C_{s1} and C_{s2} respectively. The difference is then calculated using a difference amplifier. The output is valid on the falling edge of phase 2 (ph2d) and is latched by a sample and hold circuit. For details on the design of the circuit blocks the reader is referred to Chapter 4, Section 4.3.

3.6 Conclusions

A new method of temperature sensing suitable for small infrared pixel applications has been demonstrated. The device performance is expected to improve with CMOS scaling. The thicker stack height due to the increasing number of interconnect metal layers in modern CMOS will increase the sense capacitance. Smaller feature sizes will also allow better definition of gaps and beam widths. The lateral motion produced due to temperature change has a cubic dependence on the beam width. The advantage of capacitive sensing over resistive sensing (e.g., bolometers) is there is no self-heating due to the sense current. This means that the thermal isolation between the sensor and substrate can be made of very thin polysilicon lines without affecting sensitivity. An ion milling step can remove the top metal at the anchor leaving oxide with low thermal conductivity. Power and noise trade-off can be made by the design of the capacitive sense circuit.

Chapter 4. CMOS Micromachined Z-axis Accelerometer

Inertial sensors, such as accelerometers and gyroscopes, convert real-world motions into electrical signals. Accelerometers measure translational motion while gyroscopes measure rotational motion. Modern industrial control, aerospace and military technology would be impossible without inertial sensors. Now the automotive, consumer and entertainment markets are beginning to rely on these versatile devices as well. Emerging high-growth markets include augmented Global Positioning Systems (GPS), computer gaming and automotive navigation, to name a few. For example, silicon micromachined accelerometers are the enabling technology for automotive airbag safety systems [1].

4.1 Introduction

In the future, three-axis accelerometers and gyroscopes on a single chip will be integrated on a single chip, to create an integrated inertial measurement unit (I-IMU). The integration of this functionality will provide a cost effective solution for many augmented GPS applications. CMOS micromachining technology described in Chapter 1 has the potential to deliver an I-IMU, and accelerometers and gyroscopes in all three axes have been demonstrated in this process [3][4][5][6][7].

This chapter presents a z-axis accelerometer based on a out-of-plane comb drive. The design procedure for the comb drive, the mechanical design and the interface circuits has been explained. The accelerometer has a noise floor of less than $1\text{mG}/\sqrt{Hz}$. The linearity of the device was better than 3% over 20G input range. The cross-axis sensitivity between the in-plane and the out-of-plane axes was 32 dB. This device was designed to be used as a testbed to demonstrate temperature stabilization of CMOS micromachined sensors. Such a device is expected to have a large coefficient of temperature dependence, as the sensitivity is a function of out-of-plane curl.

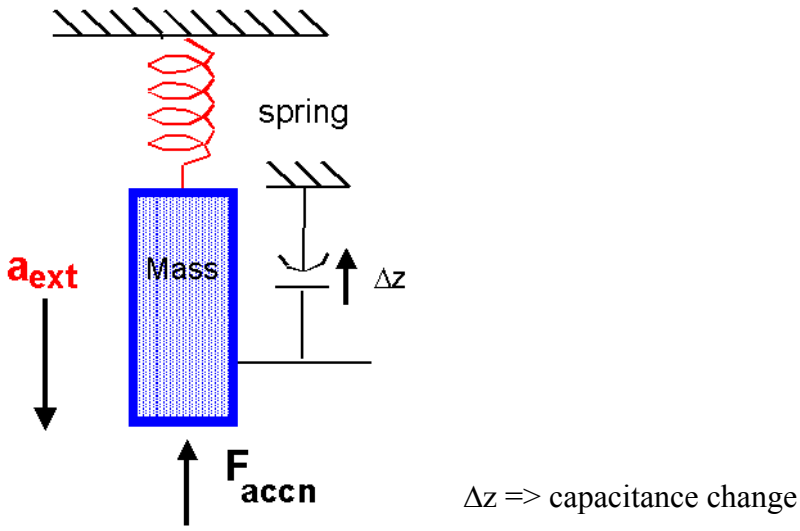


Figure 4.1 The external acceleration produces a force F_{accn} that is compresses the spring until an equal and opposite reaction force is developed. The motion of the mass is sensed by vertical capacitance change.

4.2 Device Design

The z-axis accelerometer is a spring and a mass system, illustrated in Figure 4.1. The force due to external acceleration is balanced by a spring force. If M is the mass of accelerometer, a_{ext} is the external acceleration, k_z is the spring constant, and Δz is the change in z-position of the mass; then ignoring the dynamics of the device, Δz is directly proportional to external acceleration,

$$\Delta z = \frac{Ma_{ext}}{k_z} \tag{4.1}$$

The design process aims to maximize the mechanical sensitivity of the device. Higher device sensitivity helps to improve the signal to noise ratio, if the circuit noise is dominant noise process. The spring is designed to be compliant in the out-of-plane direction, while stiffer in the x and y modes. The accelerometer was designed to fit within a fixed (500 μm x 500 μm) area. A careful consideration to the area occupied by the mass and the combs is necessary. A larger mass helps increase the mechanical sensitivity and reduce the noise floor, while a large comb drive reduces the effects of parasitic interconnect capacitance, hence, improving the sensitivity. The motion of the proof mass is detected by a change in capacitance between a fixed set of stator comb fingers and the moving set of rotor comb fingers. The capacitance sense mechanism is sensitive to out-of-plane changes, while rejecting capacitance changes due to in-plane motion. To maximize the capacitance sensitivity of the device, the area of the combs is maximized; 75% of the device area

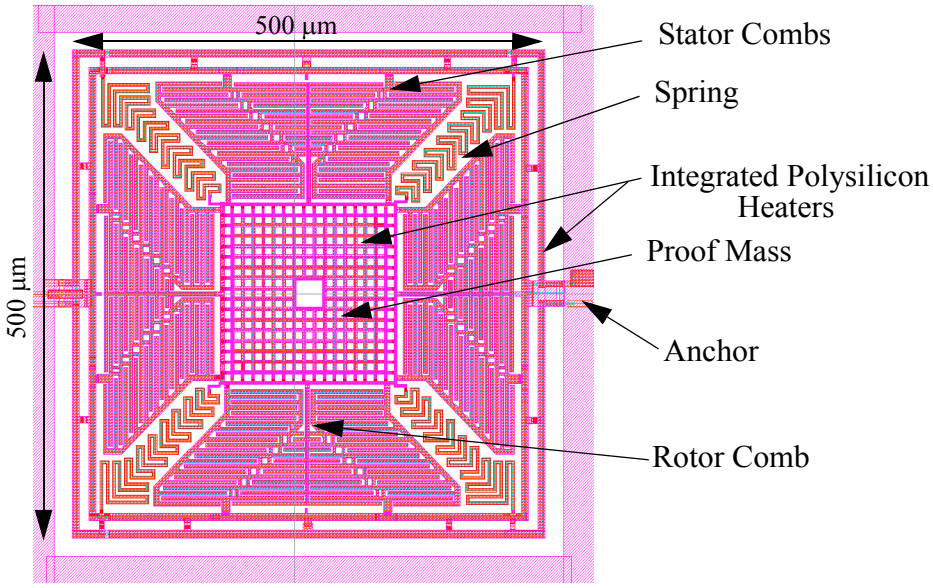


Figure 4.2 Layout of the Z axis accelerometer with the proof mass, spring, and anchor shown. The polysilicon heaters are integrated within the rotor proof-mass and combs and stator frame.

is occupied by comb fingers. The comb fingers also contribute significantly to the mass. The layout of the accelerometer is shown in Figure 4.2. The total area of the device is 500 µm x 500 µm. The proof mass is at the center of the device. The rotor is suspended from a stiff frame. The frame allows the curl of the stator fingers to be controlled and the entire device is thermally isolated from the substrate. The spring is designed using beams with both metal-1 and metal-2, to reduce thickness, providing more compliance in the out-of-plane direction. A metal-1 spring was not used, as the resistance of the metal wire leading to the polysilicon heaters is then significantly larger than with the metal-1 and metal-2 layers connected in parallel. This interconnect resistance is desired to be minimal. The spring was made compliant along z by increasing the number of meanders. A scanning electron microscope image of the accelerometer design in the Agilent 0.5mm process is shown in Figure 4.3.

4.2.1 Out-of-Plane Sensing Comb

In lateral comb drives that have been used for MEMS capacitance sense and electrostatic applications [70][71], the lateral comb finger assumes that both rotor and stator comb fingers are in plane. The vertical sensing comb intentionally have the rotor and the stator combs in different planes. Figure 4.4 shows the cross-section of the comb drive. An out-of-plane displacement causes the overlap area of the combs to change and thus changes the capacitance of the combs.

If z_{ov} is the overlap length between the comb fingers, the overall capacitance is approximately,

$$C_s = \frac{\varepsilon_o z_{ov} L_t}{g_c} \tag{4.2}$$

where, L_t is the total length of all the gaps, and g_c is the separation between the rotor and the stator comb fingers. This simple parallel plate expression is inaccurate, since it neglects fringing field effects. Nonetheless it does provide an understanding of the operation of this device. The normalized change in capacitance per unit z displacement is

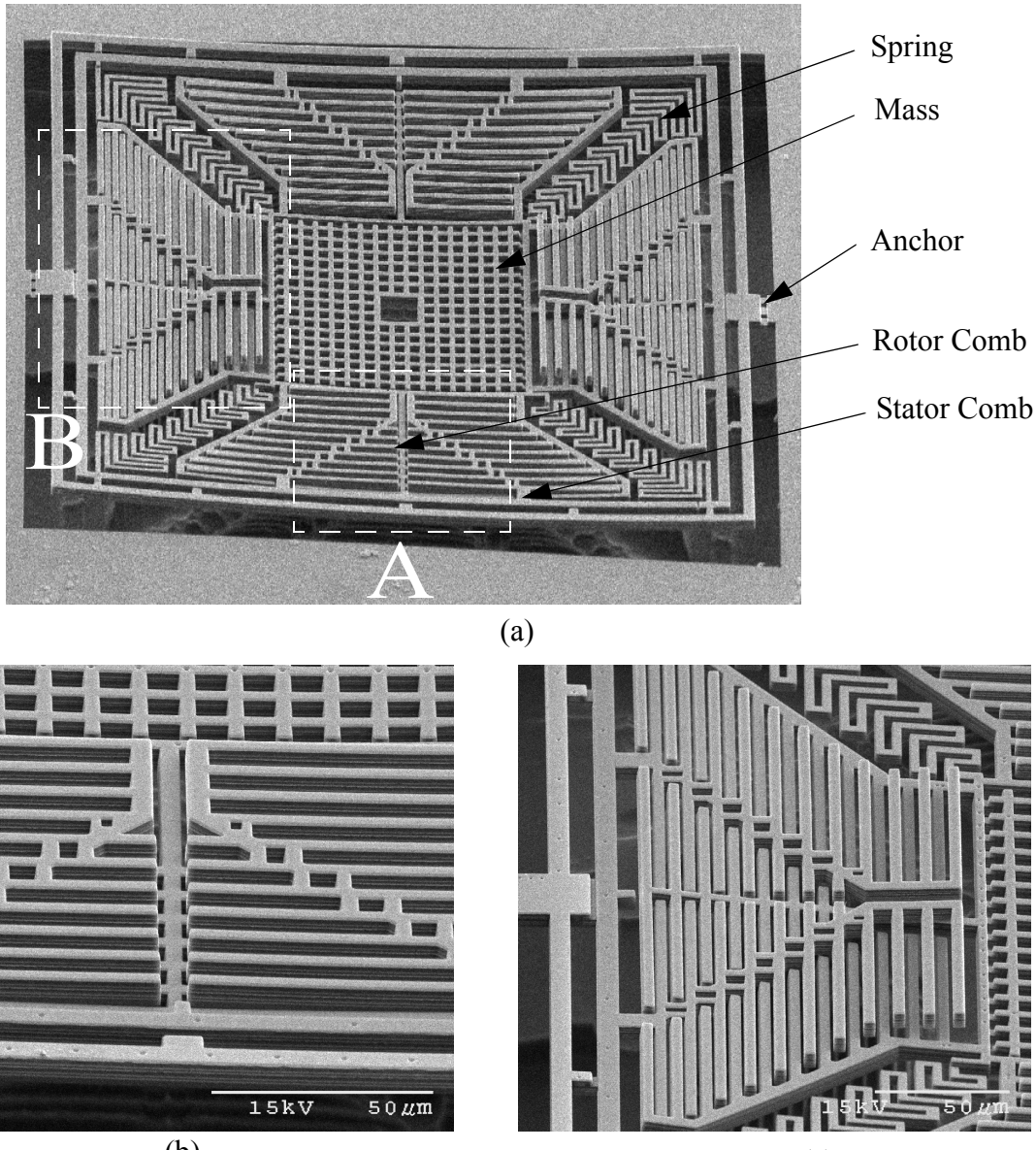


Figure 4.3 (a) Scanning electron microscope image of the fabricated Z axis accelerometer (b) Close-up of the comb fingers near the anchor (Box A) (c) Close-up of the comb fingers perpendicular to the anchor.(Box B).

$$\frac{1}{C_s}\frac{dC_s}{dz} = \left(\frac{g_c}{\varepsilon_o z_{ov} L_t}\right)\frac{\varepsilon_o L_t}{g_c} = \frac{1}{z_{ov}} \tag{4.3}$$

This expression indicates that engineering the overlap area can improve the device sensitivity. The equation is not valid when the combs are not engaged. An inherent problem with this comb drive is that the direction of displacement cannot be determined if the combs are completely in plane. This problem is overcome by designing combs so that they are not completely aligned.

CMOS micromachining offers multiple combinations of metal and oxide beams for mechanical structure design. Each of the layers, due to manufacturing reasons, has different residual stress gradients. The details of the residual stress gradient on the different combinations of metal and oxide beams has been studied in Chapter 2. With the inclusion of the residual stress gradients in the design process, we can introduce a z-offset between the rotor and the stator. FEM simulations, using the procedure outlined in Chapter 2, were used to design for this curl. The design aim is to produce a z-offset between the rotor and the stator combs, ensuring that the stator combs are always above the rotor combs.

Curl in Stator Frames

The curl in stator frames can be computed from the internal bending moments extracted for each beam type. Consider a simple stator frame, as shown in Figure 4.5, where the length of the anchored beam is L_1, and that of the frame is L_2 A simplified analysis can help understanding the behavior of curled structures. We neglect the effect of axial stress in the beams, although this stress will have an effect on the structural curl, for fixed-fixed structures.

Using symmetry, only one half of the frame is considered. The horizontal (x) beam has a guided-end boundary condition. The problem is reduced to that of a cantilever with a moment

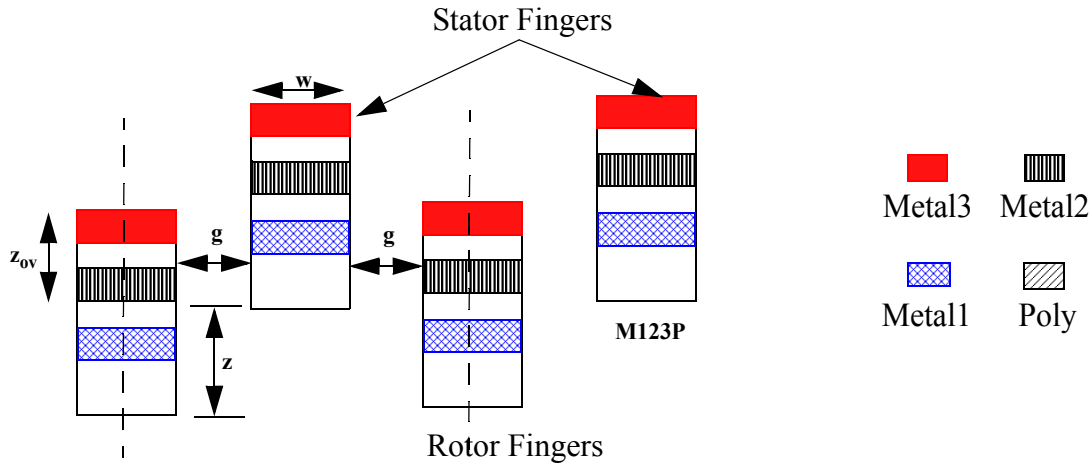


Figure 4.4 Cross-section of an out-of-plane comb-drive.

acting at the tip. The vertical (y) beam is a cantilever with a built-in boundary condition which enforces $M_y=0$. This implies that the x beam will produce torsion in the y beam. At the junction of the beam the following boundary conditions apply,

$$\left.\frac{dz}{dx}\right|_{beam1} = \left.\frac{dz}{dx}\right|_{beam2} = \theta_2 \tag{4.4}$$

$$M_2 + M_{2int} + M_{1t} = 0 \tag{4.5}$$

where M_2 is the bending moment acting on the y beam that is produced due to curling, M_{2int} is the internal bending moment due to process-induced residual stress gradients and M_{1t} is the moment produced due to torsion in the y beam on the x beam. Then the internal bending moment of beam 2 is

$$M_{2int} = (EI)_2\frac{2\theta_2}{L_2} + (GJ)_1\frac{\theta_2}{L_1} = \theta_2\left(\frac{2(EI)_2}{L_2} + \frac{(GJ)_1}{L_1}\right) = \frac{(EI)_2}{\rho_2} \tag{4.6}$$

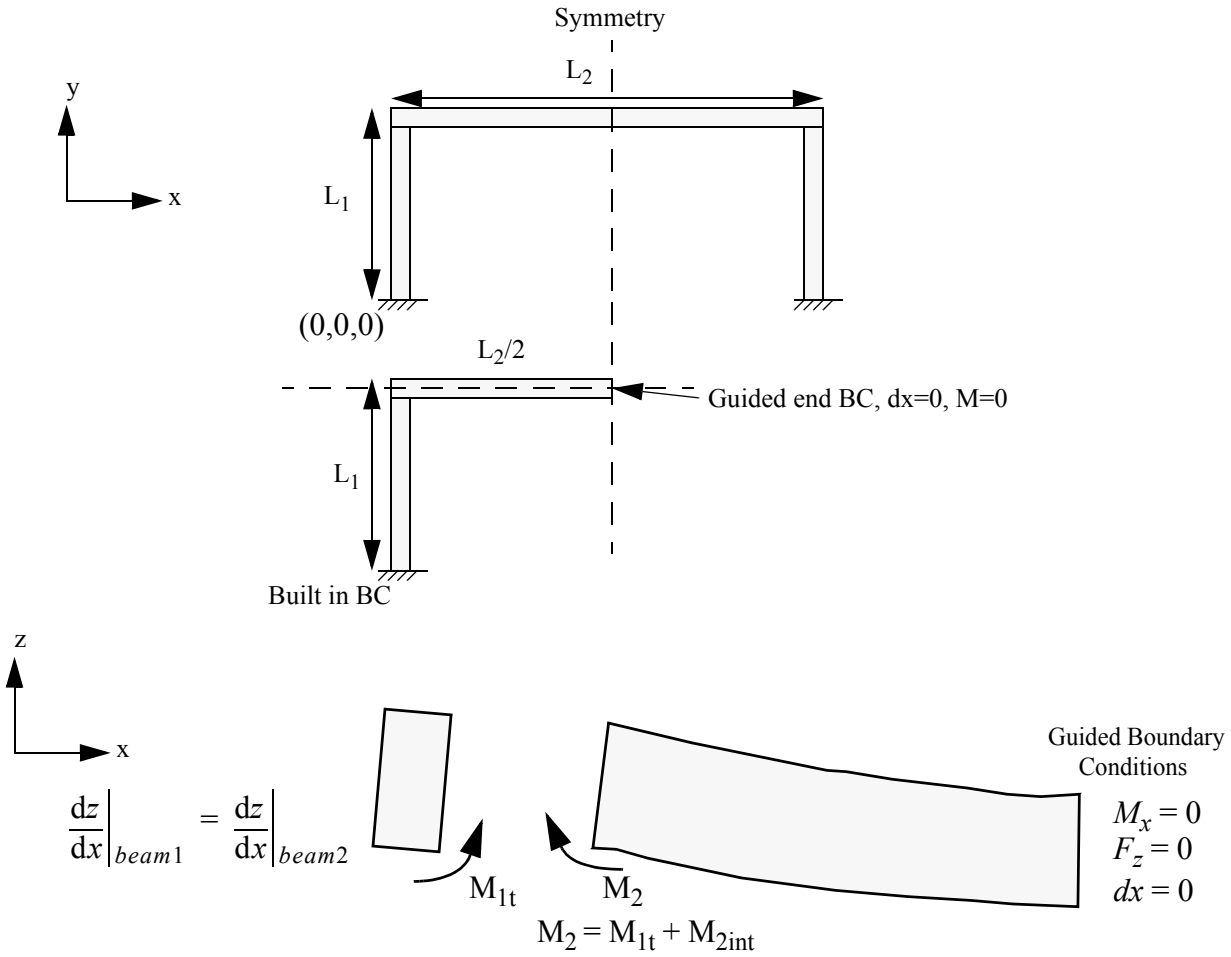


Figure 4.5 Reduction of the stator frame to a 2 cantilever problem.

$$\text{as, } \frac{1}{\rho} \approx \frac{\mathrm{d}^2 z}{\mathrm{d}x} = \int_0^L \frac{\mathrm{d}z}{\mathrm{d}x} dx = \frac{\theta}{L} \tag{4.7}$$

where $(EI)_2$, is the effective stiffness, and ρ_2 is the radius of curvature of beam 2, $(GJ)_1$ is the torsional stiffness of beam 1. For a beam with effective Young's Modulus, E_{eff}, effective Poisson ratio ν, width w and height h, the torsional stiffness [72] can be expressed as

$$(GJ) = G_{eff} J_{eff} = \frac{E_{eff}}{2(1+\nu)} \left(\frac{1}{3} a b^3 \left(1 - \frac{192b}{a\pi^5} \tanh\left(\frac{\pi a}{2b} \right) \right) \right) \tag{4.8}$$

where $a = max(w, h)$ and $b = min(w, h)$. This is an approximate expression that neglects the multi-layer nature of the beam. The effective stiffness (EI) for the uniform cross-section assumption can be calculated as

$$(EI) = \frac{E_{eff}}{12} w h^3 \tag{4.9}$$

Further, substituting for θ_2,

$$\frac{1}{\rho_2} = \frac{1}{\rho_{2f}} \left(1 + \left(\frac{L_2}{2L_1} \right) \frac{(GJ)_1}{(EI)_2} \right) \tag{4.10}$$

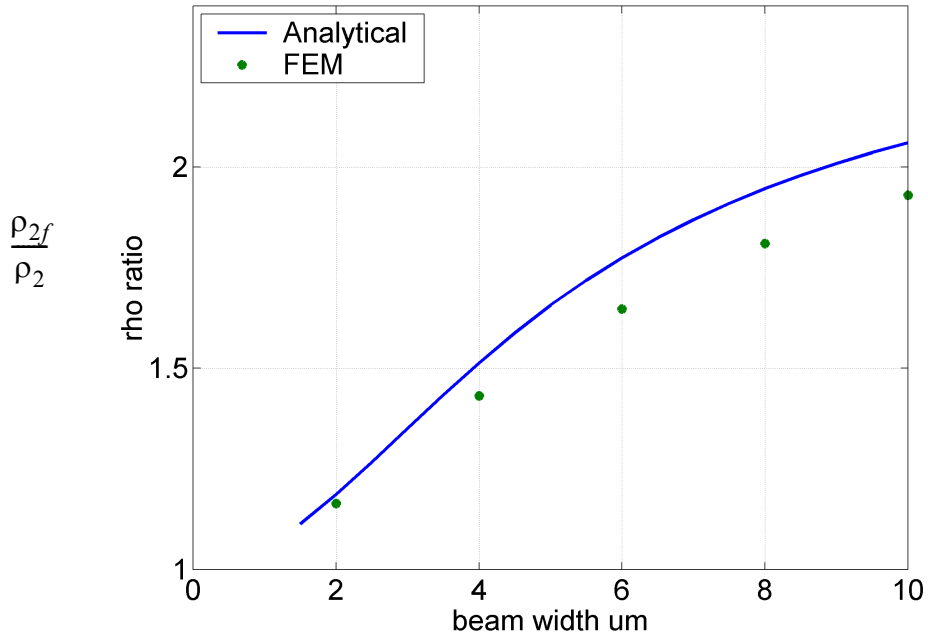


Figure 4.6 Plot of the ratio of the x beam radius of curvature, to that of the y beam, for $L_2 = 2L_1$, for different beam widths (w_1=w_2).

where ρ_{2f} is the final radius of curvature of the x beam. The curvature of the horizontal beam is lower than that of a single cantilever beam. A plot of the ratio of the x beam radius of curvature vs. that of the y beam, for a stator with $L_2 = 2L_1$, with different beam widths is shown in Figure 4.6. The z-deflection of any point of the stator can now be calculated. The z-deflection of any point on the y beam and x beam of the stator is calculated as,

$$z_1 = \frac{y^2}{2\rho_2}, \qquad 0 < y < L_1 \tag{4.11}$$

$$z_2 = \frac{L_1^2}{2\rho_1} - \frac{x^2}{2\rho_{2f}}, \qquad 0 < x < \frac{L_2}{2} \tag{4.12}$$

In the z accelerometer design, the stator comb fingers start from different points on the stator. The choice of the starting point can help design offsets such that the z_{ov} is uni-directional and tuned for the highest sensitivity. Figure 4.7 shows the regions occupied by the rotor and the stator combs. If ρ_3 is the radius of curvature of the material of the stator comb fingers, and y_{off1} is the y co-ordinate at which stator comb fingers are connected to the y beam, then the vertical offset of the stator fingers can be written as

$$z_{stat1} = \frac{y_{off1}^2}{2\rho_2} + \frac{(x)^2 + (y - y_{off1})^2}{2\rho_3} + \frac{y_{off1}}{\rho_1}(y - y_{off1}), \text{ in region } R_1 \tag{4.13}$$

Similarly, if x_{off2} is the x co-ordinate of the in x beam connected stator fingers, then curl is expressed as

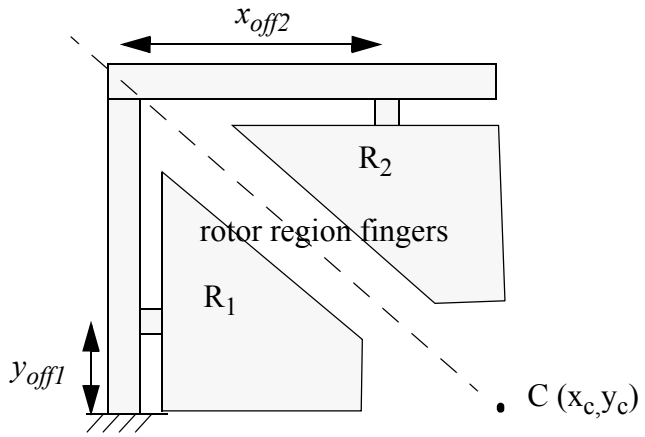


Figure 4.7 The area R_1, occupied by the y beam-connected stator comb, and area R_2, the x beam-connected stator combs.

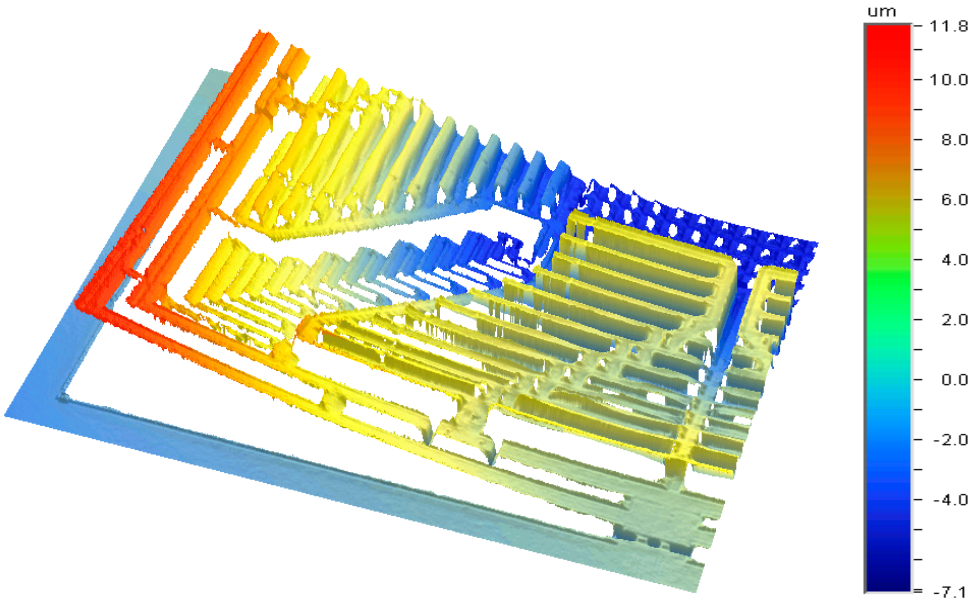


Figure 4.8 Curl of the accelerometer measured by a white light interferometer, indicating the relative displacement between the rotor and the stator fingers.

$$z_{stat2} = \frac{L_1^2}{2\rho_1} - \frac{x_{off2}^2}{2\rho_2} + \frac{(x - x_{off1})^2 + (L_1 - y)^2}{2\rho_3} + \frac{L_1}{\rho_1}(L_1 - y), \text{ in region } R_2 \tag{4.14}$$

Rotor Curvature

The rotor curvature can be assumed to be symmetrical about the x and the y-axes, if the residual stress in the film are equal along the x and the y directions. This has been verified through measurement to be true for the CMOS micromachining process. The rotor deflections can be described by a spherical surface about the center of the rotor

$$z_r = z_c + \frac{(x - x_c)^2 + (y - y_c)^2}{2\rho_r}, \text{ in region } R_1 \text{ and } R_2 \tag{4.15}$$

where x_c, y_c, z_c are coordinates of the center of the stator. The value of z_c is determined by the axial stress in the spring. To the first order, if the curl of the spring is assumed to be the same as that of the rotor material, then we can write

$$z_c = \frac{L_1^2}{2\rho_1} - \frac{(x_c^2 + (y_c - L_1)^2)}{\rho_r} \tag{4.16}$$

The measured curl of the accelerometer measured using a WYKO white light interferometer [73] is shown in Figure 4.21. The rotor is seen to be lower than the stator to maintain the same signed

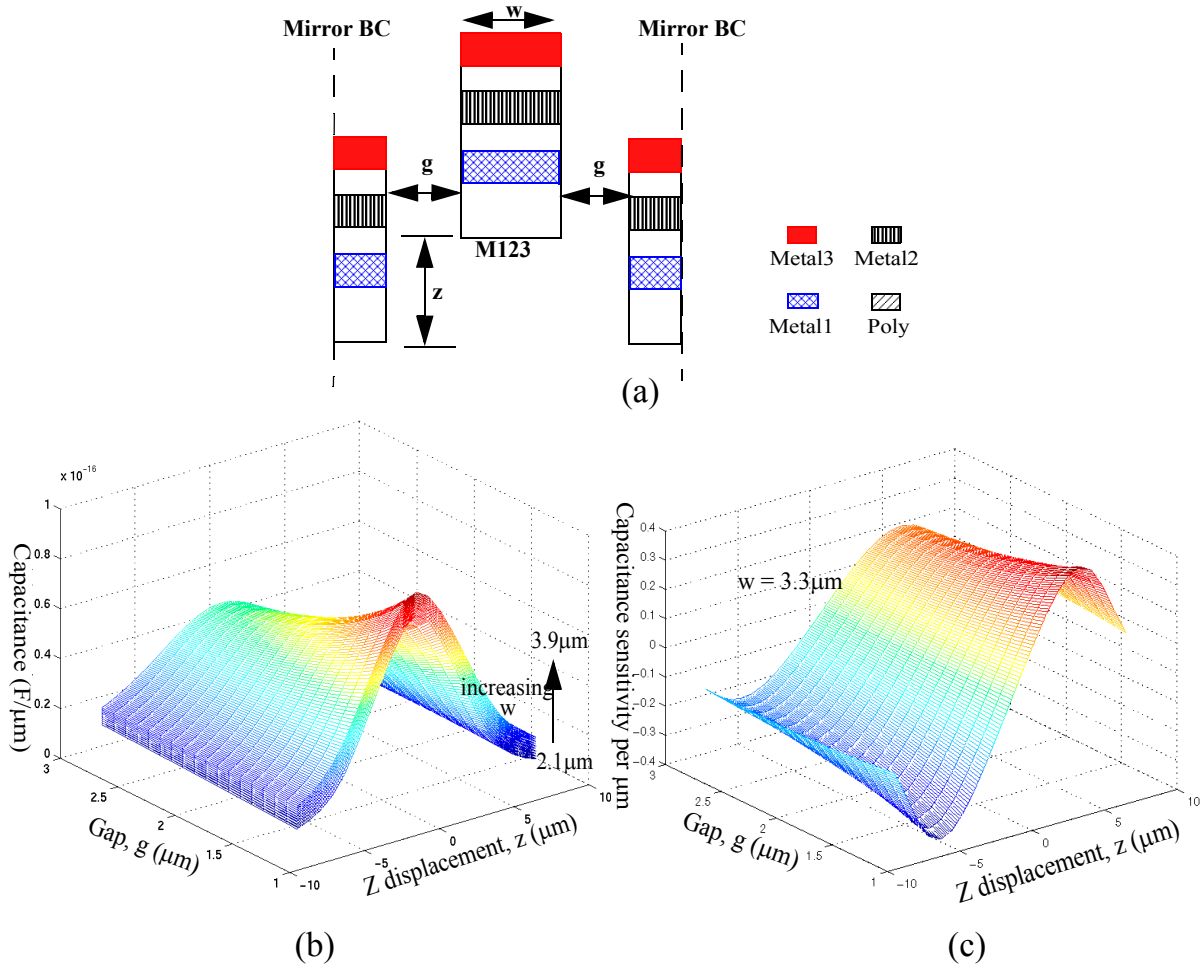


Figure 4.9 (a) Two-dimensional simplification of the vertical comb drive for simulation. (b) Variation of the comb finger capacitance with the width (w), the gap (g) and the z displacement (c) The sensitivity of the device

sensitivity. The average overlap distance between the rotor and the stator is using s, and (4.15) using MATLAB [33].

4.2.2 Simulation-Based Capacitance Change Model

Simple parallel-plate expressions stated in the previous chapter do not account for the fringing capacitance. This capacitance is very significant when the comb fingers are barely engaged. A parameterized equation, fit to finite element simulation data, was developed for the out-of-plane comb drive. The cross section of the sensing comb fingers is shown in Figure 4.9a RAPHAEL simulations [75] were run on a single pair of comb fingers, exploiting the mirror symmetry of the problem. Design parameters are the width of the comb finger, *w*, the gap between the stator and the rotor comb fingers, *g,* and the out-of-plane z-displacement, *z*. The simulation data can be summarized in a regression expression

$$C = a_0 + a_1 w^2 + a_2 w + \left(a_3 + \frac{a_4}{g} + a_5 w\right) \exp\left(\frac{-(a_6 - z)^2}{a_7 + a_8 w + a_9 g}\right) \quad (4.17)$$

The coefficients were obtained by a regression analysis using SPLUS[76] as, a_0=4.44 x 10-18 F/μm, a_1=3.72 x 10^{-19} F/μm^2, a_2=4.00 x 10^{-18} F/μm, a_3=1.58 x 10^{-18} F/μm, a_4= 8.35 x 10^{-17} F/μm^2, a_5=7.86 x 10^{-19} F/μm^2, a_6=7.42 x 10^{-4} μm, a_7=5.25 μm^2, a_8=7.4e-4 μm and a_9=6.89 μm. The residual sum of squares for the fit was 1.91 x 10^{-33} F^2, for 11240 observations. The capacitance per unit micron and the sensitivity of the capacitance change per micron of z-displacement is shown in Figure 4.9. It is observed that the sensitivity has a maxima when the combs are just engaged, when the z-displacement is about 5 μm. The design process therefore tries to optimize z-offsets to achieve this maximum sensitivity

4.2.3 Mechanical Structure Design

The mechanical design of the structure has two objectives: to maximize compliance in z while being as stiff as possible in the x-y directions; and to obtain optimal curl in the stator and the rotor to achieve maximum sensitivity. The specifications for the design and the manufacturing-constrained design rules are listed in Table 4.1. The spring is designed to be compliant in the out-of-plane direction, while being stiffer in the x-y modes. The spring constants are k_z = 0.198 N/m, k_x=1.93 N/m and k_y=2.12 N/m.

The design flow used for the mechanical design process is described in Figure 4.10. The mechanical and comb drive z-offset designs are decoupled to speed up the design process. To maximize the sensitivity of the device, the area of the combs is maximized. 75% of the device area (500 μm x 500 μm) is occupied by comb fingers. The mechanical simulation uses a two-layer approximation of the full structure. This approximation is necessary for smaller thickness of the metal 1-2 spring. This methodology reduces the number of elements in the simulation, compared to meshing all the layers. The device was meshed using the auto-meshing tool described in Chapter 2. Equivalent material properties are used for the two layers. These iterative simulations define the dominant natural frequency and separation modes of the device. The summary of the modes is shown in Figure 4.11.

The design of the rotor and the stator curl that determines the z-offset between the rotor and the stator combs is a function of the residual stress gradients. A full multi-layer simulation using

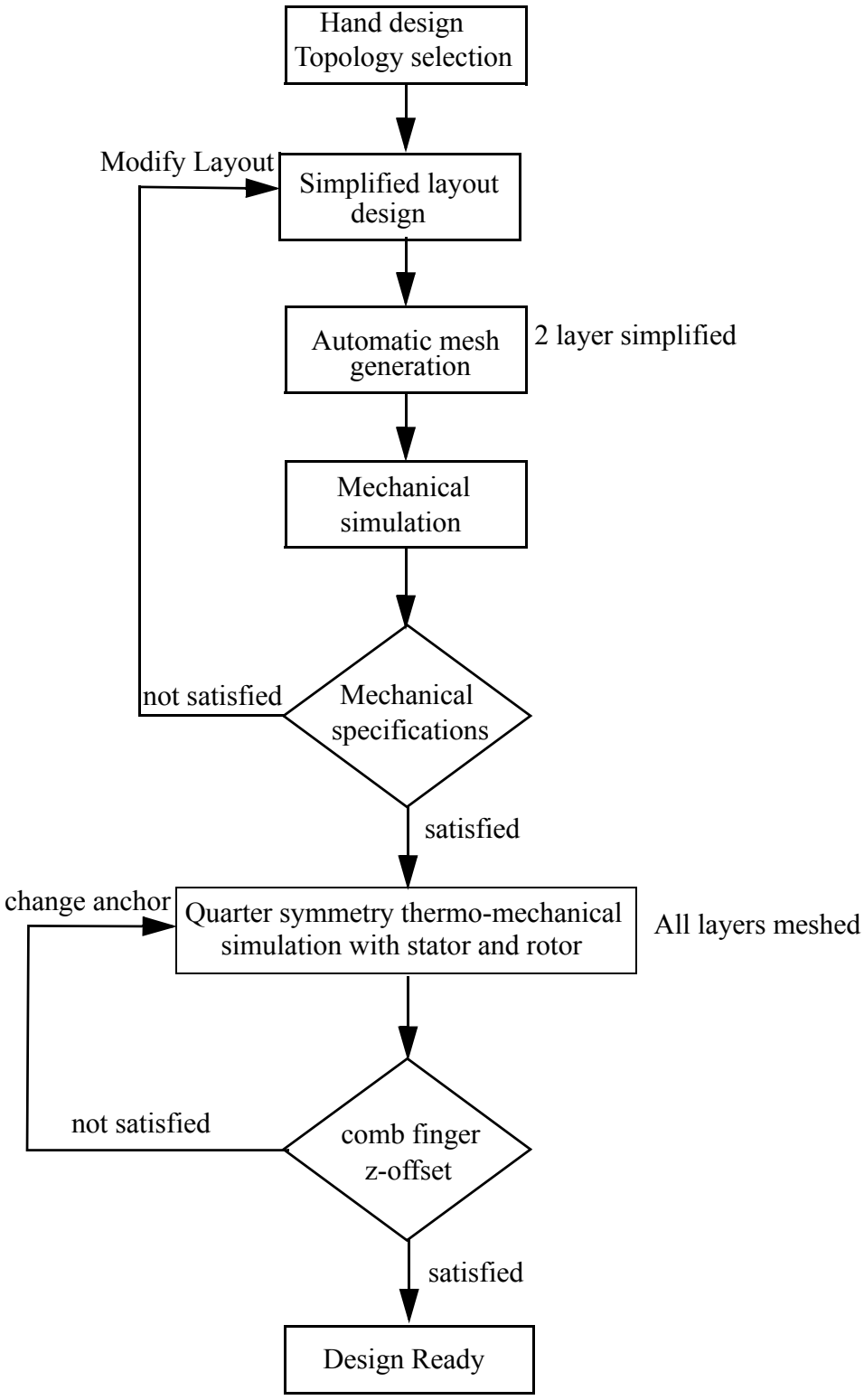
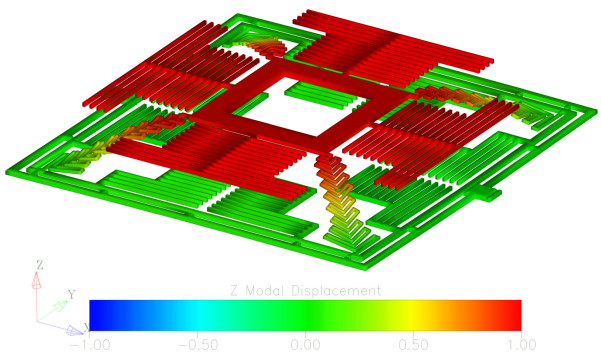
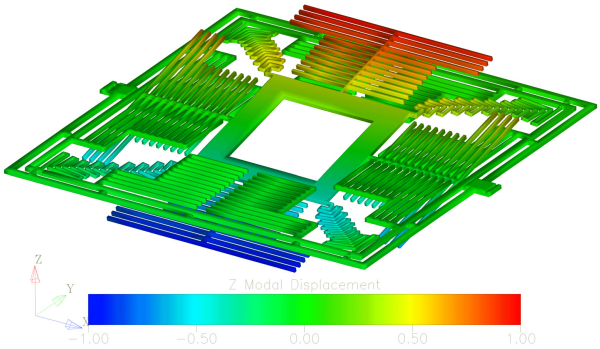


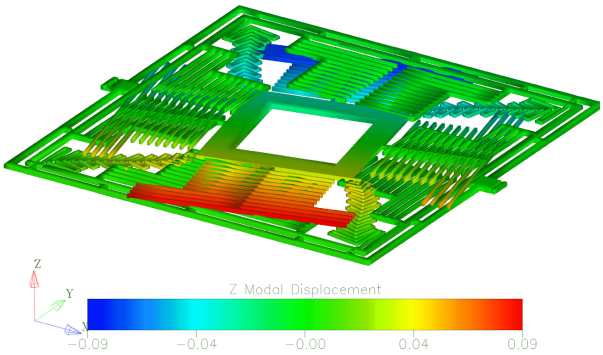
Figure 4.10 Flowchart describing the design process for optimization of the mechanical structure as well as the out-of-plane comb drive. The two design problems are decoupled.



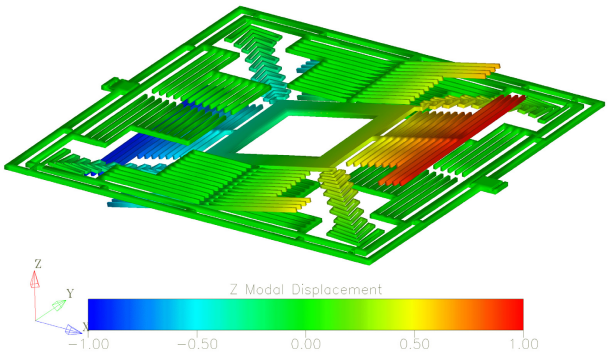
Mode 1: f = 5.48 kHz



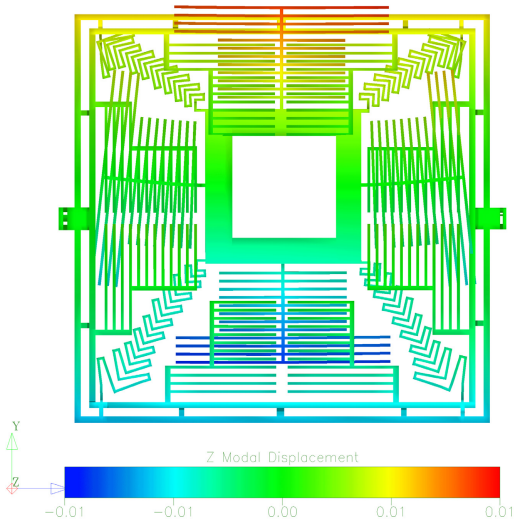
Mode 2: f =9.84 kHz



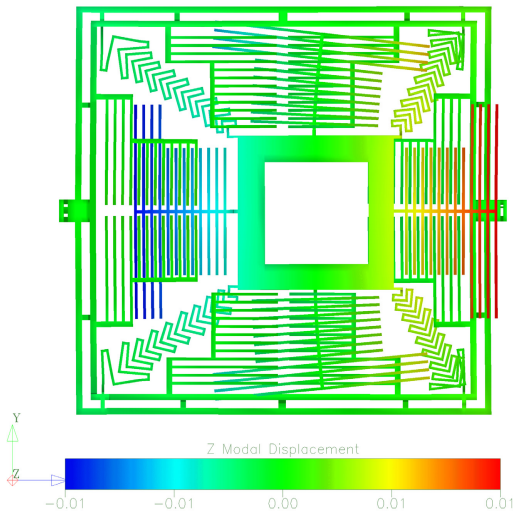
Mode 3: f = 9.90 kHz



Mode 4: f = 10.16 kHz



Mode 5: f = 19.49 kHz



Mode 6: f = 20.04 kHz

Figure 4.11 Finite element simulation results of the resonant modes for the z axis accelerometer. This simulations was done using a two layer approximation of the CMOS structure.

techniques described in Chapter 2 is required. Due to the limitations of the simulation tool, a full device simulation is time consuming. However, the device's quarter symmetry can be exploited to reduce the simulation complexity. This simulation does not capture all the mechanical modes of the device, but captures the rotor and stator curvature accurately. The aim of this set of simulations is to place the stator comb anchor point such that a desirable z-offset is obtained between the rotor and the stator, and that the sign of the capacitance change due to z-displacement is always the same. The results of the simulation are shown in Figure 4.12.

4.2.4 Sensor Mechanical Noise

Brownian noise from impingement of air molecules and structural damping acts as a force generator acting on the accelerometer structure. The force noise source, F_n, is given by [77]

$$F_n^2 = 4k_B T b \Delta f \tag{4.18}$$

where, k_B is the Boltzmann's constant (1.38 x 10^{-23} J/K), T is absolute temperature of the device, and b is the mechanical damping coefficient. This noise force can be translated to a noise equivalent acceleration, as

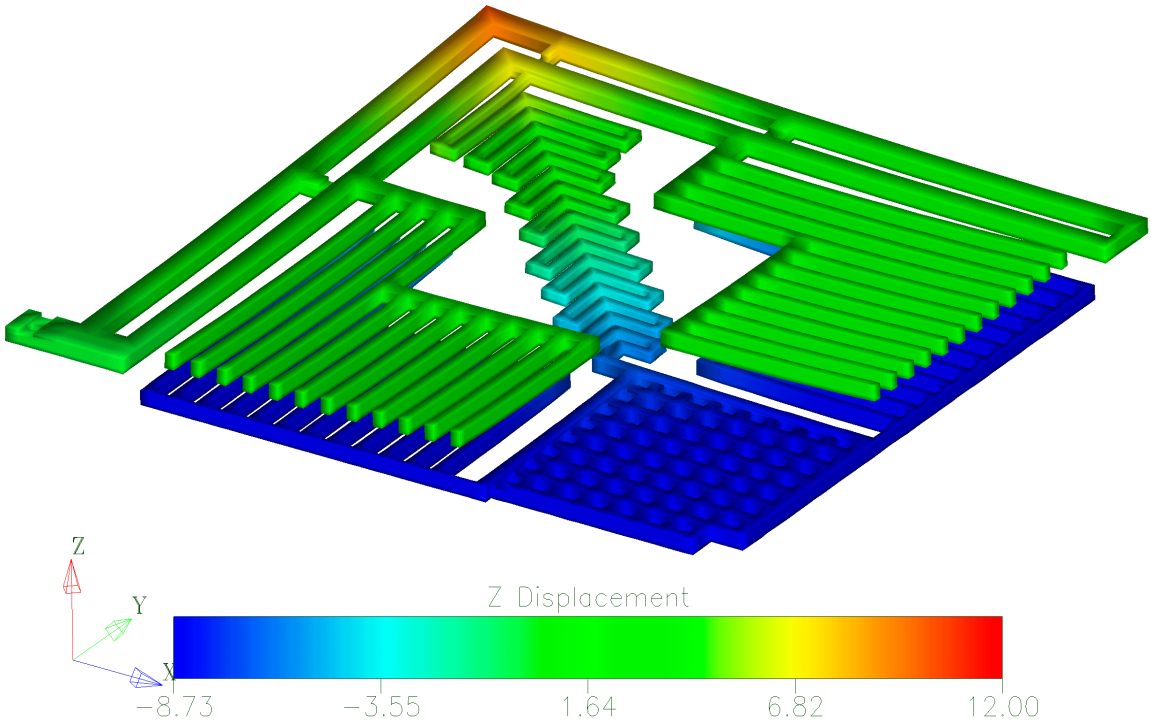


Figure 4.12 Finite element of structural curl with all metal layers and complete proof-mass.

Table 4.1: Design specifications and constraints

Parameter	Value	Unit
Area	500μm x 500μm	μm^2
Z natural frequency	< 6	kHz
Mode separation	2x	-
Cross axis sensitivity	40	dB
Minimum spring width	3.0	μm
Minimum beam width	3.6	μm
Minimum gap	1.5	μm

$$a_{nd}^2 = \frac{4k_B T\omega_r}{mQ_z}\Delta f \tag{4.19}$$

where ω_r is the resonant frequency of the dominant mode, m is the mass, and Q_z is the quality factor of the out-of-plate mode. The quality factor of the accelerometer is limited by the energy dissipative processes, such as the viscous drag of the surrounding air. In general, when the characteristic dimension like the thickness, d, of the structure is much larger than the mean free path of air at atmospheric pressure, L_{air}, then the flow is in the continuum regime. When $d < \lambda_{air}$, then the flow is in the molecular regime. The intermediate regime in which $\lambda_{air} < d < 1000\lambda_{air}$ is the Knudsen-flow region. The characteristic dimension of a CMOS micromachined device is in the order of 1 to 5 μm ($17\lambda_{air}$ - $83\lambda_{air}$), and, therefore, operates in the Knudsen-flow region. However, a continuum flow is assumed in our analysis. The quality factor for the dominant mode of the device is limited by the squeeze film damping between the plate and the substrate, and by Couette-flow damping in the numerous comb fingers of the out-of-plane comb drive, as illustrated in Figure 4.13. Squeeze film damping occurs when the gap between two closely spaced parallel plate changes. The quality factor due to squeeze film damping, Q_{zs} is expressed for square plates in [68] as

$$Q_{zs} = \frac{m\omega_r g_s^3}{0.42\mu l^4} \tag{4.20}$$

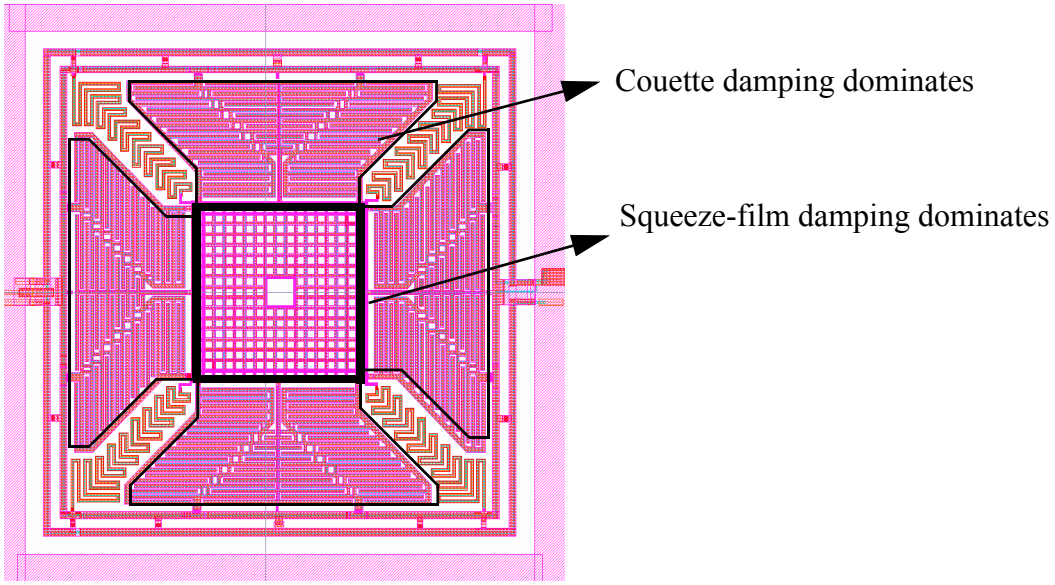


Figure 4.13 The Couette damping dominated in the out-of-plane combs, where as squeeze-film dominated in the proof-mass that sits closer to the substrate.

where, l is the length and width of the square plate, μ is the viscosity of air, and g_s is the average separation between the substrate and the device. The average separation between the substrate and the plate was measured to be 11 μm by exposing the bottom silicon by removal of the device on a test die. The brownian noise of the sensor can be lowered by reducing ω_r, increasing the mass and increasing the quality factor by reducing damping. This expression is accurate for cases when the dimensions of the plate are much larger than the separation between the plate and the substrate. The application of (4.20) leads to large errors in the case of z-axis accelerometer due to the presence of holes, therefore an effective length (l_{peff}) less than the actual length of the plate may be used. The squeeze film damping in the comb fingers is neglected because of the much larger separation between the fingers and the substrate, because of the curvature of the rotor structure. The Couette-flow damping between the comb fingers can be expressed as

$$Q_{zc} = \frac{m\omega_r g_c}{\mu A_{ov}} \tag{4.21}$$

where A_{ov} is the total overlap area between the comb fingers. This equation generally tends to overestimate the Q_{zc}, and correction factors have been proposed in literature [72][78]. The effective quality factor for the out-of-plane mode of the accelerometer is given by

$$\frac{1}{Q_z} = \frac{1}{Q_{zc}} + \frac{1}{Q_{zs}} \tag{4.22}$$

For the accelerometer design with m=4.7 x 10^{-10} Kg, ω_r=2.92 x 10^4 rad/s, effective length of the plate l_{peff}=134 μm, g_c = 1.5 mm, μ=1.8 x 10^{-5}, z_{ov} = 2.1 μm and A_{ov}=1.55 x 10^5 μm^2, the quality factor due to squeeze film (Q_{zs}) damping is calculated to 7.4, and that due to Couette damping ($Q_{zc)}$ is 8.25. The quality factor of the device in the dominant mode (Q_z) is 3.9. The Brownian noise due to mechanical structure is 52 μG/$\sqrt{Hz}$.

4.3 Design of Fixed-Gain Temperature Independent Circuit

The input acceleration is sensed by measuring the change in capacitance between the rotor and the stator fingers. The capacitance change is across a single capacitor, unlike the fully differential capacitance change seen in other CMOS micromachined accelerometers [5][6]. The total sense capacitance of the accelerometer (C_{accn}) is estimated using (4.2), to be 229 fF, for an average overlap (z_{ov}) of 2.1 μm between the stator and the rotor fingers, calculated from the analysis in Section 4.2.1. The capacitance change sensitivity with input acceleration is

$$\frac{\partial C_{sav}}{\partial a_{in}} = \left(\frac{\partial C_{accn}}{\partial z}\right)\left(\frac{\partial z}{\partial a_{in}}\right) = \left(\frac{\varepsilon_o L_t}{g_c}\right)\left(\frac{m}{k_z}\right) = \left(\frac{\varepsilon_o L_t}{g_c}\right)(\omega_r^2) \tag{4.23}$$

For the accelerometer design, a proof mass moves by 11.5 nm for 1 G of input acceleration. This motion corresponds to a 1.32 fF of capacitance change. A bridge configuration is used to sense the capacitance change. The reference capacitor for the bridge is designed using an identical mechanical structure whose rotor motion is mechanically constrained. If the stator and the rotor are assumed to overlap completely, the value of the reference capacitance (C_r) is 574 fF. (this is not entirely accurate as the stator and the rotor curl differently). The parasitic capacitance (C_p) due to the layout is estimated using parasitic extraction provided in DIVA [79], to be 390 fF. The parasitic is large as to the long routing between the combs and the circuits, are shielded from the heater routing wires by a ground plane. This shielding is important to protect the high impedance capacitance sense node from the temperature control circuit transients. A approximate model of the capacitance bridge is shown in Figure 4.14

Capacitance sensing circuits need to set the D.C level at the output of the bridge. Several techniques have been used to set this voltage, including reverse-biased diode [69], a sub-threshold MOS transistor [5], and high-valued resistors [2]. These techniques allow continuous time sense

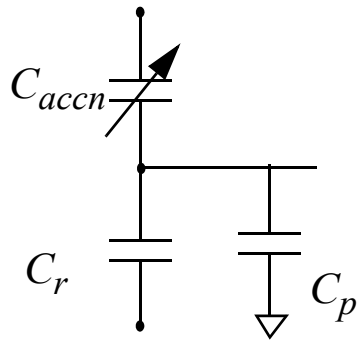


Figure 4.14 Model of the capacitance sense bridge circuit, including routing parasitic capacitance.

capacitance circuits. These topologies can yield the best noise performance, as the sampling time is maximized. However, the problems with such topologies is that the D.C. offset voltages. are a function of the biasing mechanism and the gain of the circuit is a function of temperature. Earlier versions of the capacitance sense circuits used a reverse biased diode to set the D.C voltage. However, due to the problems described in Section 3.5.1, this approach was not pursued for the accelerometer design. A circuit based on a chopper-stabilized approach was designed. Chopper stabilized approach has been previously used for capacitive sensors in [80]. The most important specifications for the circuit are low D.C. bias drift and constant gain over temperature. This ensures this circuit can be used to measure the micromechanical transducer temperature effects without introducing its own temperature drift.

A simplified architecture of the circuit along with the clock scheme for the capacitance chopper stabilized circuit is shown in Figure 4.15. The capacitance bridge, consisting of the device and the reference are driven by two signals, V_{modp} and V_{modn}, opposite in phase. These signals are generated by switching reference voltages V_{rp} and V_{rn} using clocks *p1* and *p3*. V_{modp} is at V_{rp} when p1 is high, and at V_{rm} when p3 is high; V_{modn} is at V_{rn} when p1 is high, and V_{rp} when p3 is high. The sense node is reset by a charge-injection compensated NMOS switch by clock *p2*, to set a D.C. voltage at the node. The schematic of the charge injection compensated switch used at the sense node is shown in Figure 4.16. The charge injected, when the switch is opened, is canceled by an equal and opposite charge injection from the dummy switch. The area of the dummy transistor is half that of the switch transistor. The voltage, V_{ft}, is used to compensate for charge injection errors that are not entirely cancelled by the relative sizing of the switch and the dummy. The sense node voltage is set to the analog ground voltage and clocks *p1,p2,p3* are non-overlapping. An error voltage is developed when the switches are turned off, due to charge

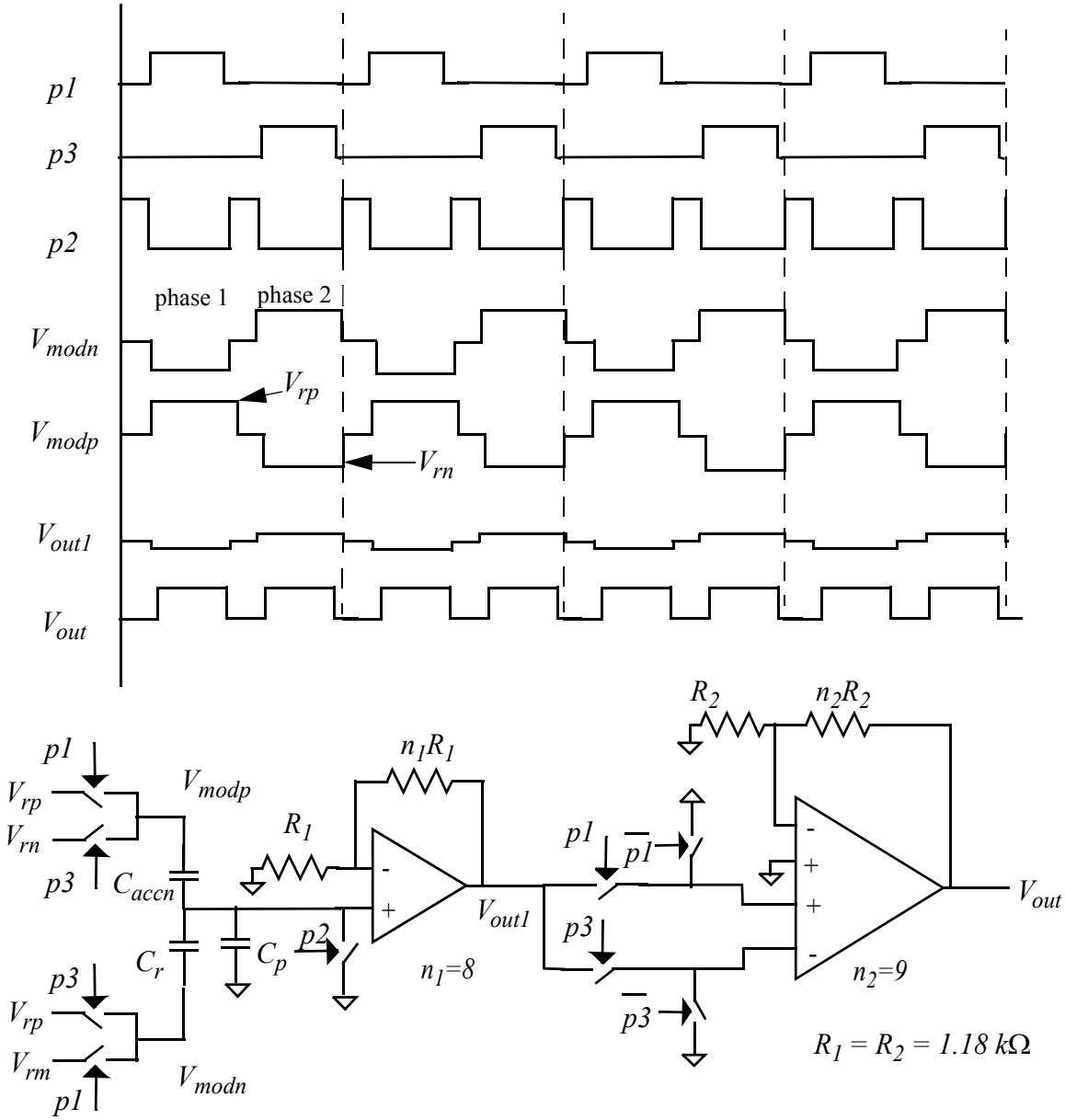


Figure 4.15 Schematic of the capacitance sense circuits, along with the control signals

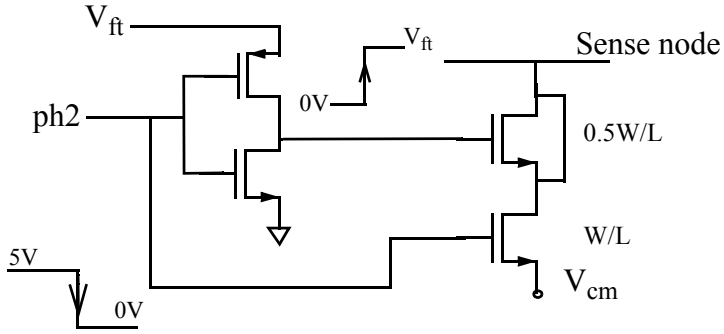


Figure 4.16 Charge-injection compensated NMOS switch. The voltage, V_{ft}, is used to control the charge dump.

injection, and D.C. input offset voltage of the first stage opamp. All these sources can be lumped together as a single error voltage, $V_{offset1}$. The gain of the input stage is $1+n_1$, where n_1 is the ratio of the feedback resistors. The output voltage when $p1$ is high can be written as

$$V_{p1} = (1+n_1)\left(V_{rp}\frac{C_{accn}}{C_{accn}+C_r+C_p} + k_s V_{rn}\frac{C_r}{C_{accn}+C_r+C_p}\right) + (1+n_1)V_{error1} \tag{4.24}$$

where k_s is a scaling factor for mismatch compensation. It is difficult to design the reference capacitor to be of the same value as that of the accelerometer. Therefore, an offset cancellation circuit has been included. The scale factor k_s is set by resistive division of the reference capacitor drive voltage or accelerometer, to cancel the D.C offsets and maximize the dynamic range. Mismatch compensation is essential, as the nominal values of C_{accn} and C_r are not identical. This mismatch is measured as a capacitance by the sense circuit. The difference between the reference and the accelerometer capacitance is large enough to saturate the output. To allow for maximum dynamic range, the factor k_s is tweaked, so that net measured capacitance is zero. This relative gain between the bridge inputs is implemented by a resistive divider at the input. Another way to implement this is by controlling the charge injection from the reset switch at the bridge input depending on the phase of the input. The latter approach was found not to have large enough dynamic offset cancellation range to eliminate the large mismatch related offset between the reference and the sense capacitors. Similarly, the output voltage when $p3$ is high is

$$V_{p3} = (1+n_1)\left(V_{rn}\frac{C_{accn}}{C_{accn}+C_r+C_p} + k_s V_{rp}\frac{C_r}{C_{accn}+C_r+C_p}\right) + (1+n_1)V_{error1} \tag{4.25}$$

The demodulator stage consists of a difference amplifier, whose gain is also set by ratio of two polysilicon resistors, and clocks p1 and p3. When p3 is high, the gain of the difference amplifier is $-(n_2+1)$, and when p1 is high the gain of the amplifier is (n_2+1). The output of the demodulator is then expressed as

$$V_{out} = (V_{p1} + V_{offset2})(1+n_2), \text{ when p1 is high,} \tag{4.26}$$

$$V_{out} = -(V_{p1} - V_{offset2})(1+n_2), \text{ when p3 is high,} \tag{4.27}$$

where, $V_{offset2}$ is the D.C. input offset voltage of the difference amplifier. An output proportional to the capacitance change is obtained by low pass filtering to remove the modulation frequency. If the duty cycle of the reset pulse is γ_r, then the output can be written as

$$V_{out} = \frac{(1-\gamma_r)(1+n_1)(1+n_2)(V_{rp}-V_{rn})(C_{accn}-k_sC_r)}{(C_{accn}+C_r+C_p)} + (1+n_2)V_{offset2} \quad (4.28)$$

The output voltage is proportional to the difference between the device and the reference capacitors. The input D.C. offset voltage from the first stage operational amplifier is cancelled, and only the second stage offset remains. The difference amplifier D.C. offset voltage is dependent on the temperature and can produce errors in the accelerometer measurements. This dependence, normalized to signal gain, can be minimized by increasing the gain before the demodulation. In the implementation described, the gain before demodulation was limited by the need for large dynamic range needed to measure large capacitance change due to temperature changes. The input offset voltage of a two input differential stage is determined by the mismatch in input pair transistors, if the D.C. gain of the operational amplifier is large enough to make the systematic offsets small.

Flicker noise that dominates at lower frequencies is reduced by the use of chopper stabilization, and to lower than the white noise level if high enough modulation frequency is used. The details of the discussion are found in Section 3.3.2.

4.3.1 Design of Circuit Blocks

Opamp Design

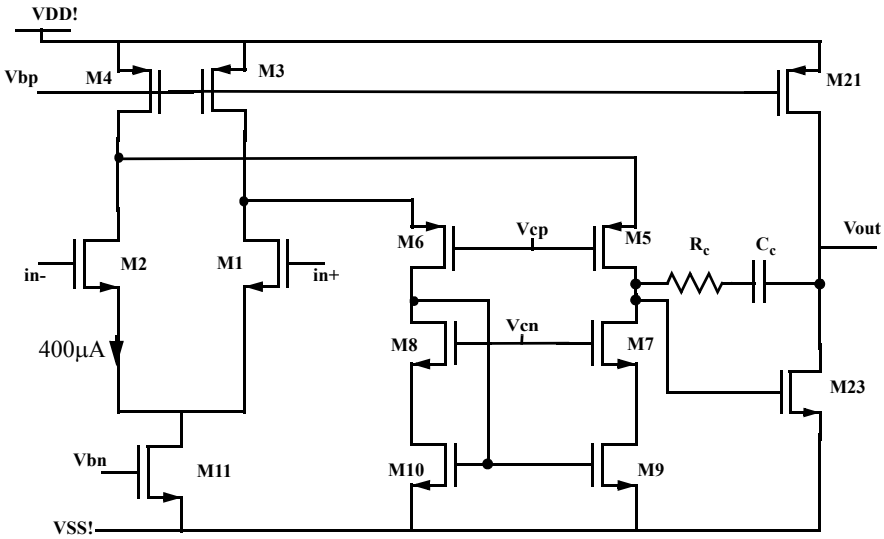
A folded cascode opamp shown in Figure 4.17 was designed for use in the capacitance detection circuit [81]. The opamp is biased by a constant-g_m biasing circuit. The opamp specifications are

- Gain-bandwidth product > 50 MHz, to maximize the modulation frequency.
- High D.C gain > 100dB, to minimize systematic offset voltage.
- Low output impedance, to drive low value feedback resistors for low thermal noise
- Low noise, to minimize contribution of circuit noise.
- Low D.C. input offset voltage, with low temperature coefficient, to minimize D.C. voltage drifts.

The n-channel MOSFETs M1 and M2 provide the input current gain, transistors M5-M8 are the cascoded to increase the output impedance. A common source output stage is added after the folded cascode stage to drive resistive loads, and increase the D.C. gain. The D.C. gain of the opamp is given by

$$A_v = A_1 A_2 = (g_{m1} R_{o1})(g_{m23} R_{o2}) = \left(g_{m1} \left(\frac{g_{mr} r_{dsr}^2}{2} \right) \right) (g_{m23} R_L) \tag{4.29}$$

where A_1, and A_2 are the gains of folded cascode (stage 1) and the common source amplifier (stage 2) respectively, g_{m1} is the transconductance of M1 and M2, g_{mr} is the transconductance of the cascode transistors (M5-M8), and R_{o1} and R_{o2} are the output impedances of the stage 1, and stage 2. R_{o1} and R_{o2} impedance of the stages is expressed in terms of the output impedance of the MOSFET, r_{dsr}. g_{m23} is the transconductance of transistor M23; and R_L is the output load resistor assumed to be much smaller than the output impedance of transistors M21 and M23. The dominant pole of the opamp occurs at the output of the first stage and is determined by C_c, that is added for dominant pole compensation,



Folded cascode transistor dimensions

Transistor	W/L	Transistor	W/L	Transistor	W/L
M1	20µm/0.9µm	M6	450µm/1.8µm	M11	140µm/1.8µm
M2	20µm/0.9µm	M7	180µm/1.8µm	M21	1730µm/1.8µm
M3	1040µm/1.8µm	M8	180µm/1.8µm	M23	600µm/1.8µm
M4	1040µm/1.8µm	M9	150µm/1.8µm		
M5	450µm/1.8µm	M10	150µm/1.8µm		

Figure 4.17 Schematic of the folded cascode opamp used in the capacitance sense circuits along with the dimensions of the transistors.

$$f_{3db} = \frac{1}{2\pi R_{o1} g_{m23} R_L C_c} \tag{4.30}$$

R_c has been included in series with C_c for lead compensation, for the right half plane zero [81]. The gain bandwidth product of the opamp is then

$$GBW = \frac{g_{m1}}{2\pi C_c} \tag{4.31}$$

The transconductance of a MOS transistor is a function of the temperature as it depends upon the carrier mobility. As the temperature is increased, the mobility is degraded and the gain drops. The reduction in opamp gain can lead into increase in input-referred offset voltages, leading to D.C. offset errors.

Constant-transconductance Bias Circuit

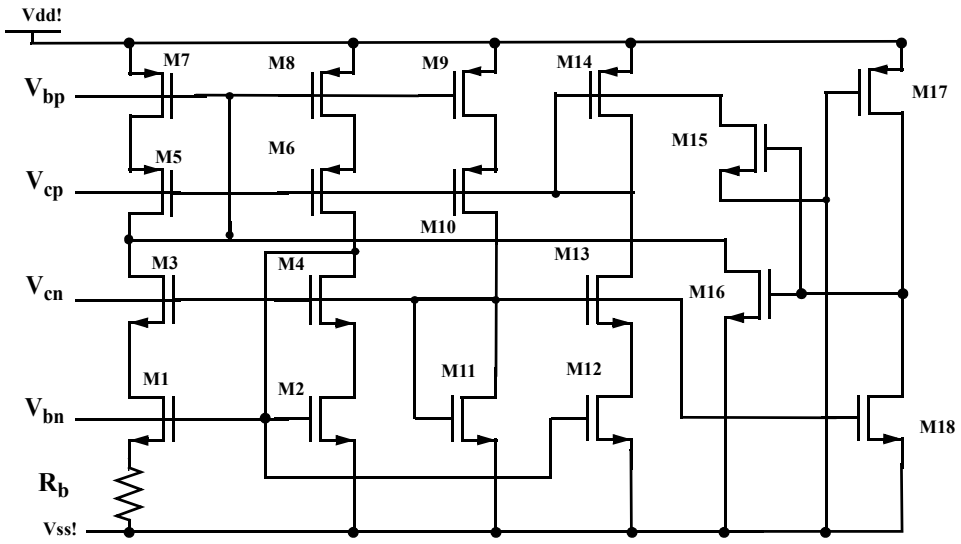
The bias voltages for the opamps are provided by a constant-transconductance or constant-g_m bias circuit [81], that allows wide swing cascode output stages. It was designed to bias the opamp and the difference amplifier. The schematic of the bias circuit is shown in Figure 4.19. Consider transistors M1-M4 along with diode connected transistor M11. The current, I_b, in M1 and M3 is equal to M2 and M4, due to the current mirroring, also the bias voltage of M3 and M4 is derived from M11. Similarly, the current in the two branches is forced equally by the p-channel MOSFETS, M5-M8 and the diode connected M9. The current in the resistor R_b is then determined by the difference in gate-source voltages of M1 and M2, denoted by V_{GSM1} and V_{GSM2} respectively

$$I_b = \frac{V_{GSM2} - V_{GSM1}}{R_b} \text{ , and} \tag{4.32}$$

$$I_b = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GSM1} - V_{Tn})^2 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GSM2} - V_{Tn})^2 \tag{4.33}$$

Substituting V_{GSM1} and V_{GSM2} in terms of the transistor parameters and solving for I_b,

$$I_b = \frac{2}{\mu_n C_{ox} R_b^2}\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}}\right)^2 \tag{4.34}$$



Constant-g_m biasing circuit transistor dimensions

Transistor	W/L	Transistor	W/L	Transistor	W/L
M1	180µm/0.9µm	M7	520µm/1.8µm	M13	120µm/1.8µm
M2	70µm/0.9µm	M8	520µm/1.8µm	M14	60µm/1.8µm
M3	120µm/1.8µm	M9	520µm/1.8µm	M15	10µm/0.6µm
M4	120µm/1.8µm	M10	450µm/1.8µm	M16	10µm/0.6µm
M5	450µm/1.8µm	M11	120µm/1.8µm	M17	1.2µm/10µm
M6	450µm/1.8µm	M12	70µm/1.8µm	M18	10µm/0.6µm

Figure 4.18 Schematic of the constant-g_m biasing circuit, and dimensions of the transistors.

where μ_n is the mobility, C_{ox} is the gate capacitance per unit area, V_{Tn} is the threshold voltage of the n-channel MOSFET, and R_b is the bias current setting resistor. R_b is an off-chip resistor that has a very low TCR. Transistors M15-M18 are used to ensure that the circuit reaches a non-zero current operating point, and avoids the undesirable, but stable operating condition at $I_b = 0$. The g_m of any n-channel MOSFET, biased using this current reference is then independent of the mobility of the transistor, and is expressed as

$$g_m = \frac{\sqrt{2}}{R_b}\sqrt{\left(\frac{W}{L}\right)}\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}}\right) \tag{4.35}$$

The transconductance of the transistors is independent of temperature and is set by geometry and the bias resistance. Such a circuit is necessary to maintain the opamp performance at high temperatures.

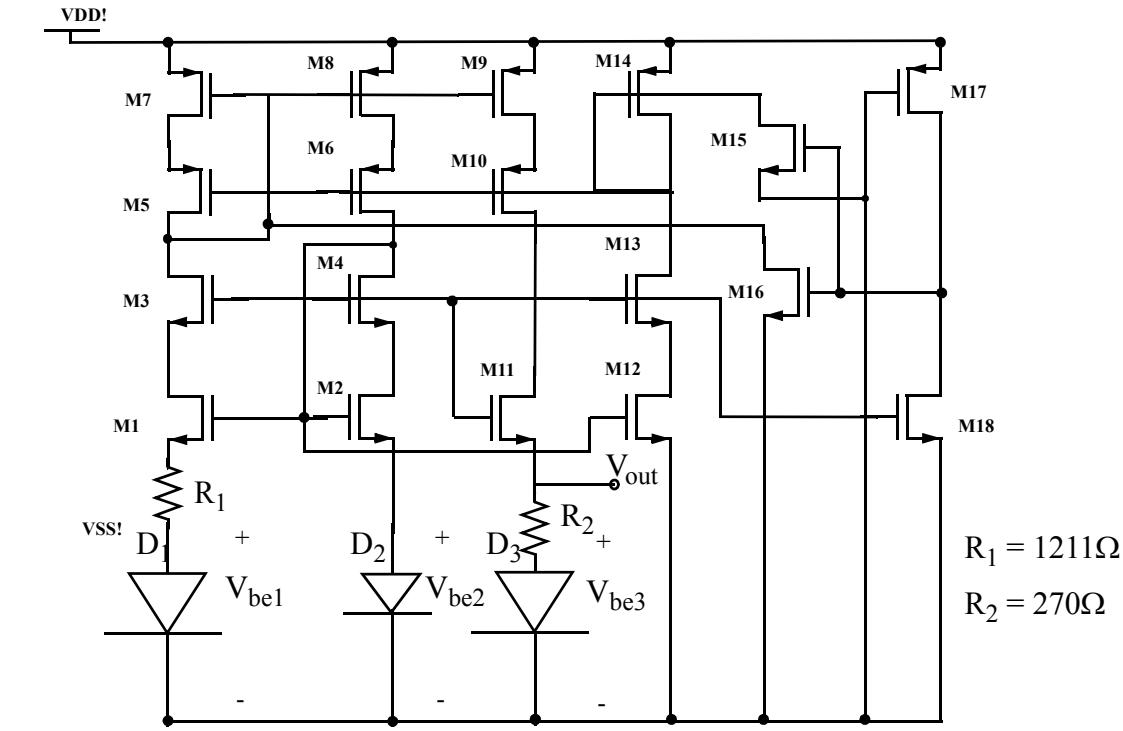
Bandgap Voltage Reference

The capacitance sense circuits use two reference voltages V_{rp} and V_{rn}. The circuit output in (4.28), is proportional to their difference. To derive temperature and power supply independent reference voltages, a bandgap voltage reference circuit was designed. Voltages V_{rp}, and V_{rn} are derived from the bandgap voltage using external non-inverting operational amplifier gain stages. The schematic of the bandgap is shown in Figure 4.19. The output voltage of the bandgap is given by

$$V_b = V_{be3} + \frac{kT}{q} \ln \frac{A_1}{A_2} \left(\frac{R_2}{R_1} \right) \tag{4.36}$$

where A_1 and A_2 are the areas of diode D_1 and D_2. The resistors R_1 and R_2 are designed using thermal-based voltage controlled resistors, and can be tuned so that the bandgap voltage has zero temperature coefficient of voltage at room temperature. A thermal-based voltage controller is designed by placing a polysilicon resistor on a heated plate. The temperature of the plate can be controlled by joule heating of a separated polysilicon heater resistor. A scanning electron microscope image of the voltage controlled resistor is shown in Figure 4.20. The temperature of the polysilicon resistor is determined using (2.36).

The ratio R_1/R_2 can be designed to be independent of ambient temperature using digitally controlled resistor ratio circuit used for temperature control described in Figure 4.21a. The bandgap voltage at room temperature is 1.2954 V, with a temperature coefficient of 457 ppm/^{o}C. The design of the bandgap can be improved with the use of improved SPICE models that accurately model temperature effects on MOSFETs. The models used in the design were found to be accurate for the nominal case, but did not account for the temperature variation. The nominal output voltage matched to 0.3% of the simulated value. The variation of the band gap voltage with temperature of resistor R_2 is shown in Figure 4.21b. The band gap could not be tuned for zero temperature coefficient.



Schematic of the band-gap reference

Transistor	W/L	Transistor	W/L	Transistor	W/L
M1	180μm/0.9μm	M7	520μm/1.8μm	M13	120μm/1.8μm
M2	70μm/0.9μm	M8	520μm/1.8μm	M14	60μm/1.8μm
M3	120μm/1.8μm	M9	520μm/1.8μm	M15	10μm/0.6μm
M4	120μm/1.8μm	M10	450μm/1.8μm	M16	10μm/0.6μm
M5	450μm/1.8μm	M11	120μm/1.8μm	M17	1.2μm/10μm
M6	450μm/1.8μm	M12	70μm/1.8μm	M18	10μm/0.6μm

Figure 4.19 Schematic of the bandgap reference circuit, along with the dimensions of the transistors.

Difference Amplifier

The schematic of the difference amplifier is shown in Figure 4.22. It is similar to the folded cascode opamp, but has two input stages, one sets the gain and the other is used for differential input. The advantage of this design is that the gain can be set by a single ratio of resistances, leading to better common mode rejection ratio, than conventional single opamp based designs using 2 ratioed pairs of resistors.

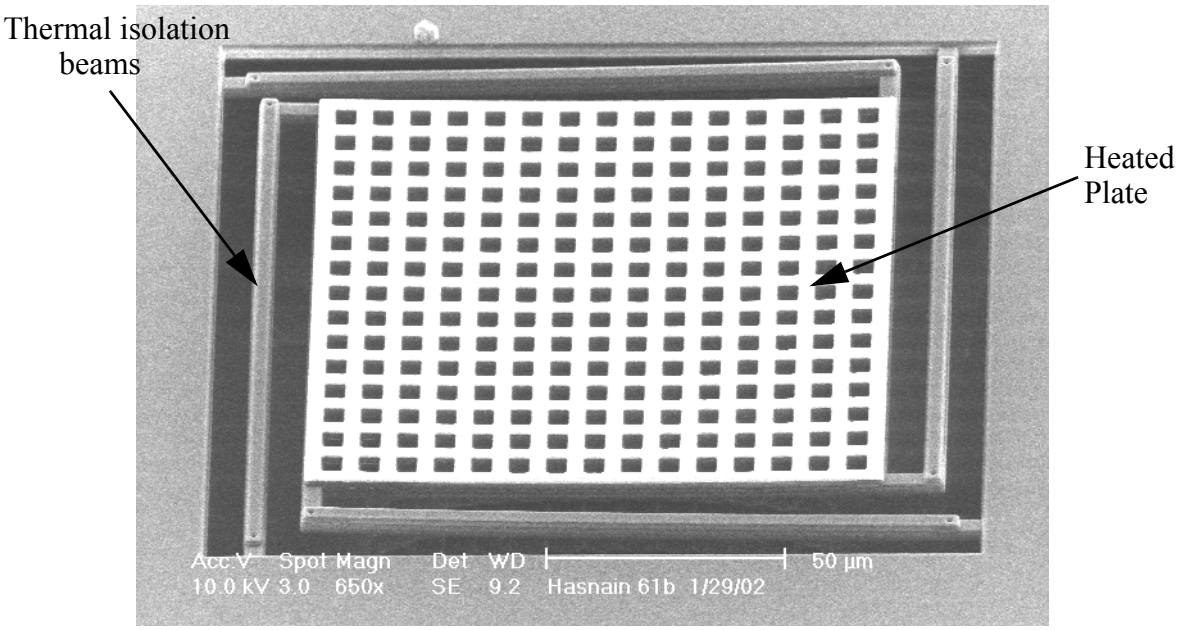


Figure 4.20 SEM of a voltage controlled resistor. A polysilicon resistor is embedded inside a thermally isolated plate. The temperature of the plate is controlled by separate embedded polysilicon resistor.

4.3.2 Circuit Noise

Circuit noise is important in determining the final noise performance of the system. The system noise determined from the circuit noise and the sensor noise.

$$V_{nsystem} = \Delta f \sqrt{V_{nsensor}^2 + V_{in,eq}^2} \tag{4.37}$$

where, $V_{nsystem}$ is the total input-referred noise measured in the system, $V_{nsensor}$ is the total mechanical noise of the sensor referred to the input of the sense circuit, and $V_{in,eq}$ is the input

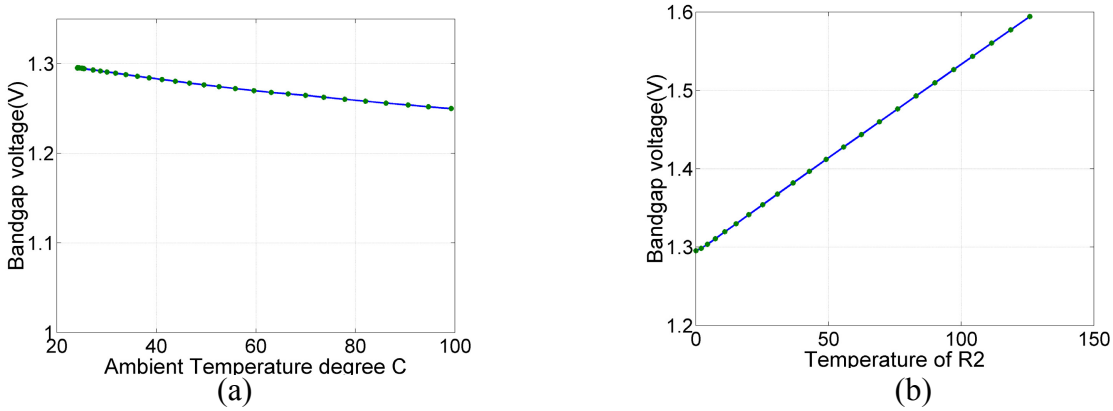
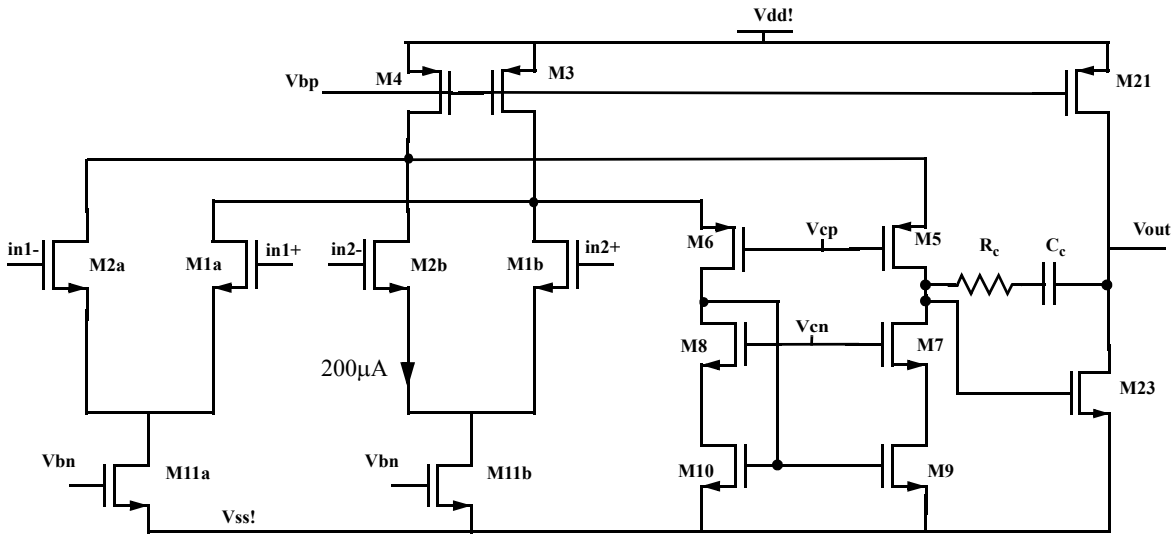


Figure 4.21 The measured output of the bandgap voltage is plotted against (a) the ambient temperature of the chip, and (b) The temperature of R2 at room temperature.



Difference amplifier transistor dimensions

Transistor	W/L	Transistor	W/L	Transistor	W/L
M1a	10μm/0.9μm	M5	450μm/1.8μm	M11a	70μm/1.8μm
M2a	10μm/0.9μm	M6	450μm/1.8μm	M11b	70μm/1.8μm
M1b	10μm/0.9μm	M7	180μm/1.8μm	M21	1730μm/1.8μm
M2b	10μm/0.9μm	M8	180μm/1.8μm	M23	600μm/1.8μm
M3	1040μm/1.8μm	M9	150μm/1.8μm		
M4	1040μm/1.8μm	M10	150μm/1.8μm		

Figure 4.22 Schematic of the difference amplifier used in the capacitance sense circuits along with the dimensions of the transistors.

referred noise of the circuits, within the bandwidth of the measurement, Δf. The input referred noise is calculated by summing the noise contribution from the various components of the sense circuit.

Opamp Noise

The circuit noise is dominated by the noise of the input stage. The noise of the successive stages can be ignored if the gain of the first is large. The noise of the input stage is calculated by considering the input referred noise of the first stage opamp (Figure 4.17). The input referred noise of the opamp is determined by the input transistors M1-2, and the current bias transistors M3-4, M9-10. The noise due to the cascode transistors M5-8, is degenerated by the output

resistance of the bias and input transistors. The input-referred noise, $V_{inn,opamp}$, of the opamp can be written as

$$V_{inn,\,opamp}^2 = 2V_{nm1}^2 + 2\left(\frac{g_{m3}}{g_{m1}}\right)^2 V_{nm3}^2 + 2\left(\frac{g_{m9}}{g_{m1}}\right)^2 V_{nm9}^2 \tag{4.38}$$

where V_{nm1}, V_{nm3}, and V_{nm9} are the input-referred noise of the transistors M1, M3, and M9 respectively. g_{m1}, g_{m3}, and g_{m9} are the transconductances of transistors M1, M3 and M9. The input referred noise for a MOSFET is a sum of the white noise and flicker noise and can be written as

$$V_{nm}^2 = \frac{8k_BT\sqrt{L}}{3\sqrt{2IW\mu_nC_{ox}}} + \frac{K_{fn}}{WLC_{ox}f} \tag{4.39}$$

where K_{fn} is a flicker noise constant for the n-channel MOSFET dependent upon the device characteristics and varies widely with different devices in the same process. C_{ox} is the gate capacitance per unit area, W and L are the width and length of the transistor. Flicker noise is significant in MOS circuits and typically dominates at low frequency. The presence of flicker noise is one motivation for use of chopper stabilization. Typically, p-channel transistors have *1/f* noise lower than n-channel transistors, since holes are less likely to be trapped. The *1/f* noise is large in the Agilent 0.5μm process available from MOSIS [34].

The noise of the operational amplifier for a bias current of 400 μA through each input transistor, and assuming the knee of the flicker noise to be 1MHz, at 29.1 nV/$\sqrt{Hz}$ at 70kHz, and 16.2 nV/$\sqrt{Hz}$ at 1.5 MHz.

Total Circuit Noise

The noise of the circuit is dominated by the noise of the first stage opamp amplifier. The first stage of the sense circuit along with the noise sources is represented in Figure 4.23. The input-referred noise of the capacitance sense circuit, $V_{in,eq}$, is given by

$$V_{in,\,eq}^2 = V_{inn,\,opamp}^2 + V_{R1}^2\left(\frac{R_2}{R_1+R_2}\right)^2 + V_{R2}^2\left(\frac{R_1}{R_2}\right)^2 [\tag{4.40}$$

where V_{R1} and V_{R2} is the noise due to resistors feedback resistors R_1 and R_2. The noise in the resistor, R, is given by

$$V_R^2 = 4k_B TR + \frac{\alpha_I I_{dc}^2}{WLf} R^2 \tag{4.41}$$

where, W and L the with length of the polysilicon resistor, α_I is a constant that incorporates the technology dependence of noise in polysilicon resistor [82], and I_{dc} is the D.C. current flowing through the resistor. The resistors are chosen to be low value (order of 1 kΩ) to minimize their noise contribution.

For, R_1=1180Ω, and R_1=9440Ω, and α_I=5.6 x 10^{-10}m^2/s, obtained from [82], the input referred noise of the circuit is 48.8 nV/$\sqrt{Hz}$ at 70kHz, and 21.2 nV/$\sqrt{Hz}$ at 1.5 MHz. For a sensitivity of 500 μV/G, and modulation frequency of 1.5 MHz, a theoretical input-acceleration equivalent noise floor of 42.5μG/$\sqrt{Hz}$ is possible. The device noise floor obtained from (4.37), is expected to be 67μG/$\sqrt{Hz}$.

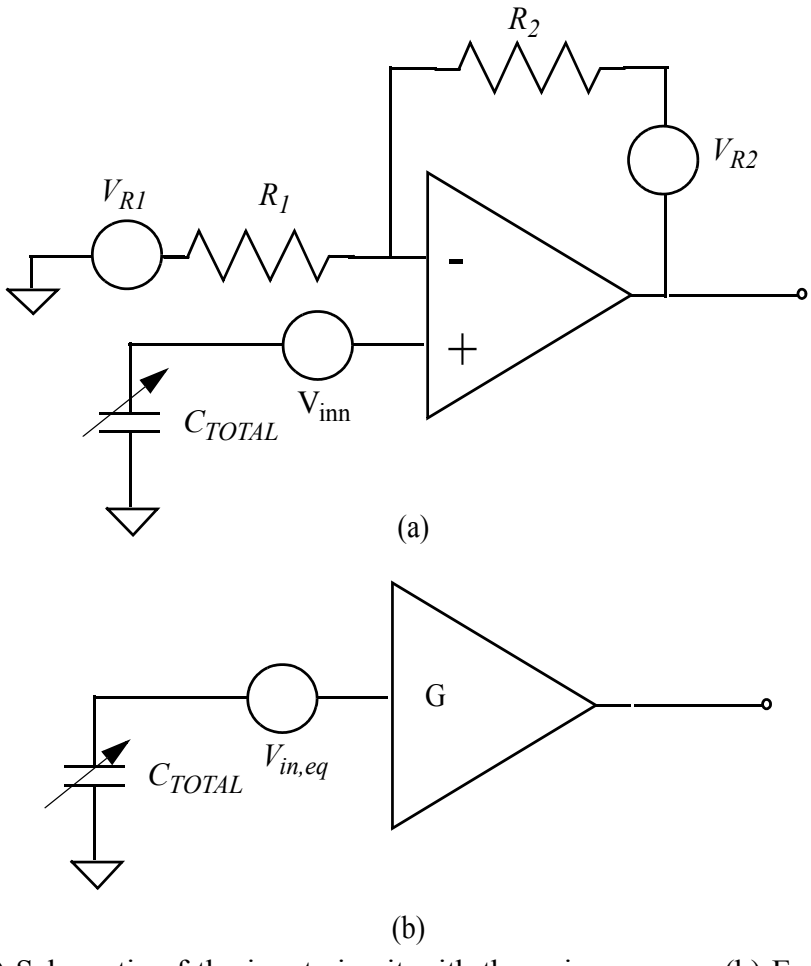


Figure 4.23 (a) Schematic of the input circuit with the noise sources. (b) Equivalent circuit showing the input referred voltage noise source.

4.4 Experimental Results

4.4.1 Z-accelerometer Device Performance

The layout of the prototype chip fabricated in the Agilent 0.5μm process [34] is shown in Figure 4.25. The z-axis accelerometer was wire-bonded in a 40 pin DIP package A custom printed circuit board with power supply voltage regulators, master clock generator, reference voltage generator (V_{rp} and V_{rn}) and low pass filter was designed. The duty cycle of the reset phase is determined by the duty cycle of the master clock. The details of the board design are included in the appendix II. A picture of the accelerometer on the PCB is shown in Figure 4.26. The master clock frequency of 141.8 kHz was generated using a 555 timer based clock generator. This modulation frequency does not yield the best noise performance, however the noise performance was adequate for temperature control application, which was the primary purpose of this board. A higher clock frequency can be applied to the board using an external pin.

The entire printed circuit board was placed on a Bruel and Kjaer Model 4808 vibration exciter, to induce different sinosoidal accelerations ranging from 1G to 10G. The acceleration of the exciter was simultaneously measured by a reference accelerometer [83]. The power spectrum measured at the output of the first stage, for an input acceleration of 1 G p-p at 330 Hz, is shown in Figure 4.24 The modulation frequency is 70.9 kHz, which is half that of the master clock frequency. The spectrum of the output of the demodulator and low pass filter is shown in Figure

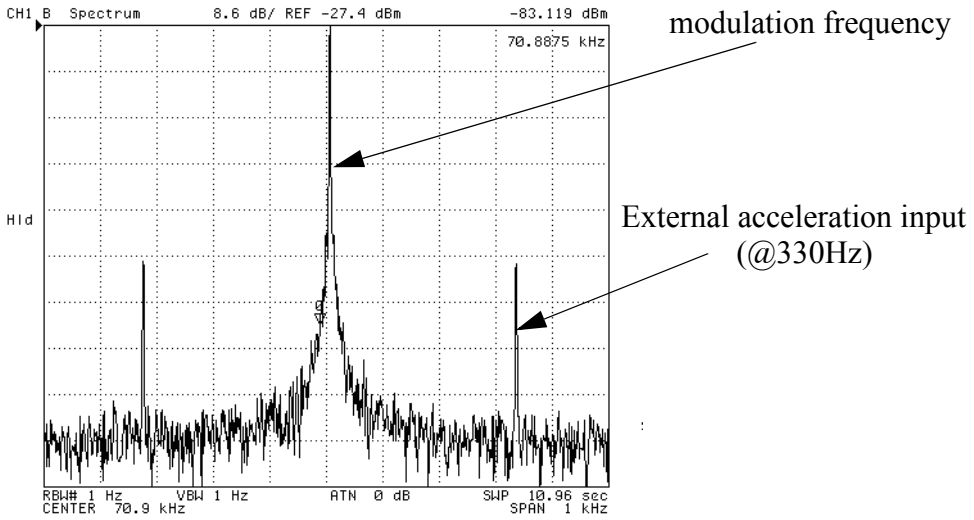


Figure 4.24 The power spectrum measured at the output of the first stage (at V_{out1} in Figure 4.15). Note that the modulation frequency of 70.9 kHz is half that of the master clock at 141.8 kHz.

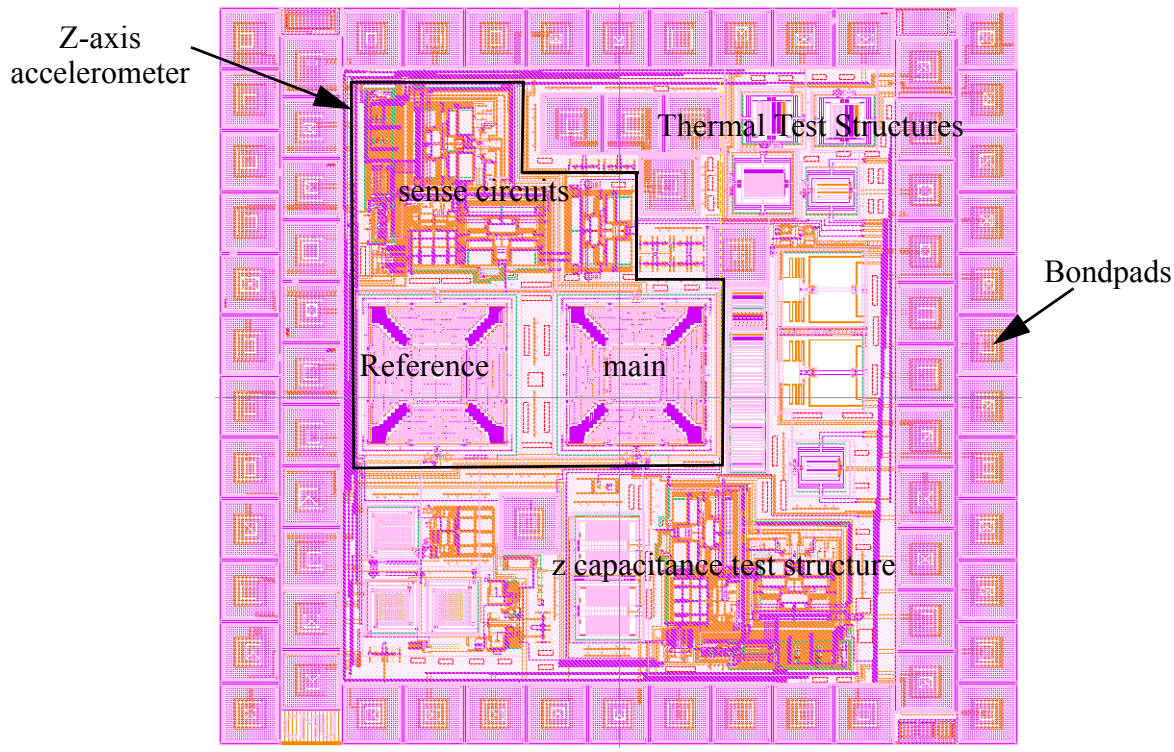


Figure 4.25 The layout of the accelerometer test chip. The accelerometer sense capacitor is at the center next to the reference capacitor. Other test devices and circuits are included on the same chip

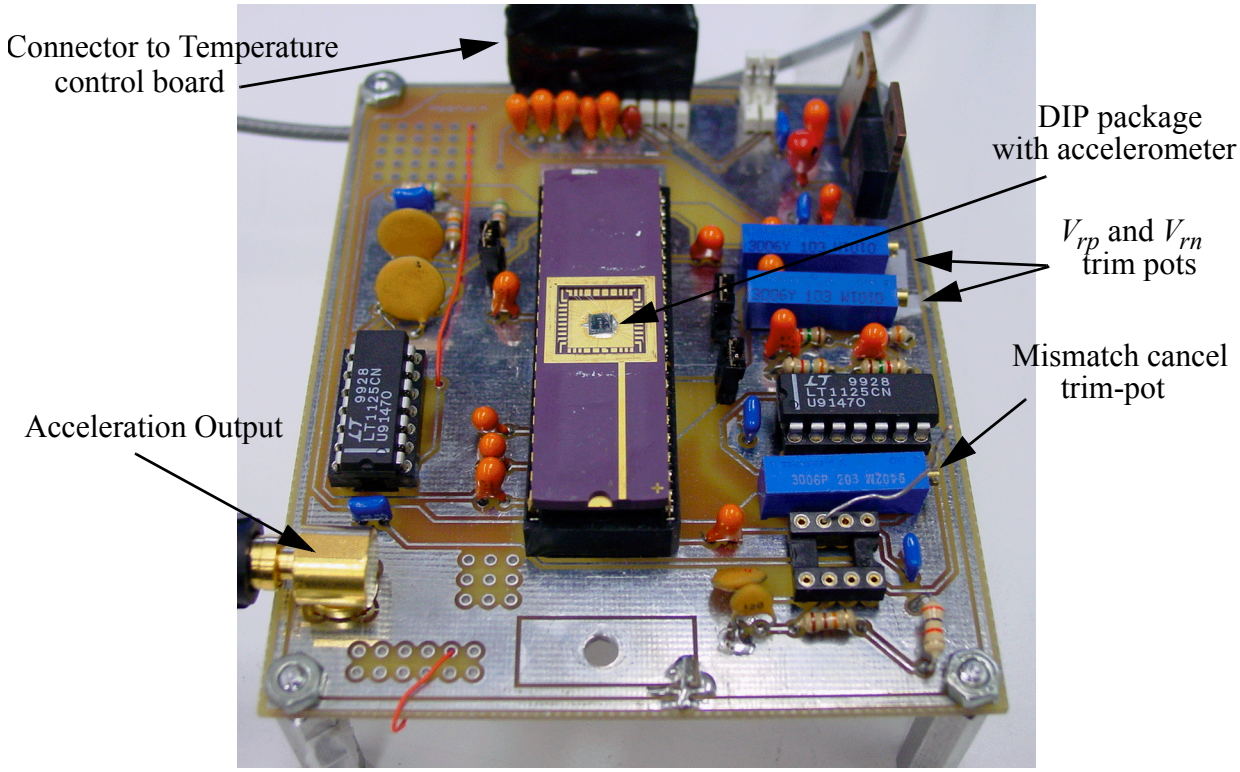


Figure 4.26 Photograph of the printed circuit board, and the test chip packaged in a 40 pin DIP package.

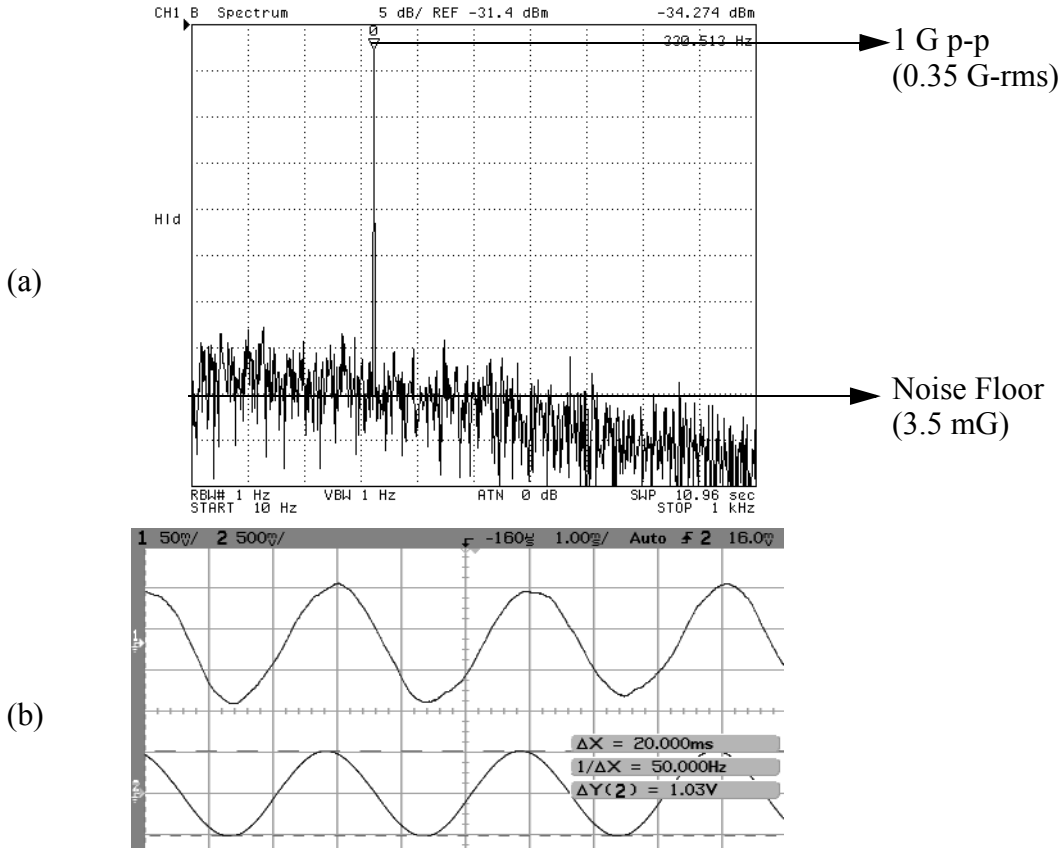


Figure 4.27 (a) Spectrum of the output signal for 330 Hz, 1 G peak to peak acceleration input signal, measured after low-pass filtering. (b) The output signal measured by the oscilloscope.

4.27. The sensitivity of the transducer before circuit gain is 0.13 mV/G/V (for V_{rp}-V_{rn}=1 V), and 9.3 mV/G after on-chip amplification. The measure noise floor ranged from was about 0.7 to 5 mG/$\sqrt{Hz}$ on the eight accelerometers tested. The noise decreases with increase in modulation frequency, indicating that the performance of the accelerometer is limited by flicker noise. The plot of the sensor noise floor with modulation frequency is shown in Figure 4.28. The performance is limited by the circuit noise. The linearity of the device was better than 3% over a 20 G input range. The cross axis sensitivity rejection ratio was 32 dB, and was limited by the test setup, that was not designed for lateral acceleration testing. The mechanical frequency of the accelerometer was measured by sweeping the input frequency of the shaker table. The performance of the accelerometer is summarized in Table 4.2.

The mechanical response of the accelerometer was characterized by electrostatic actuation of the comb fingers and measurement using the MIT microvision system [27]. Actuation of 3 VDC and 3 VAC was applied to the modulation voltage test pin. The sense node was grounded by

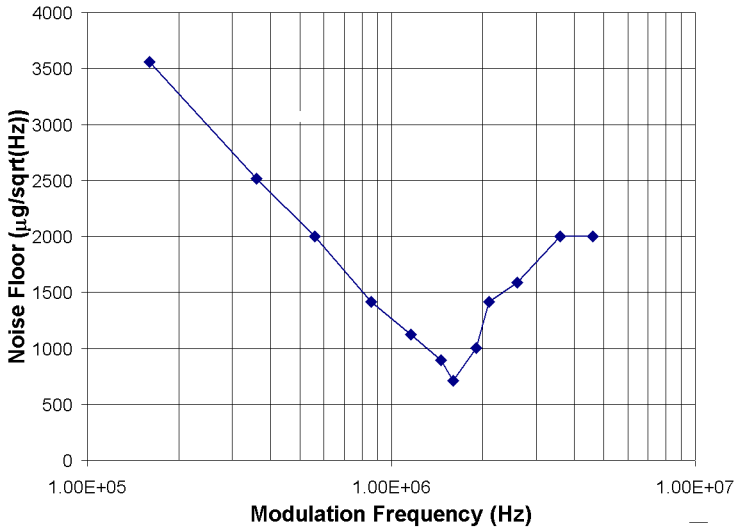
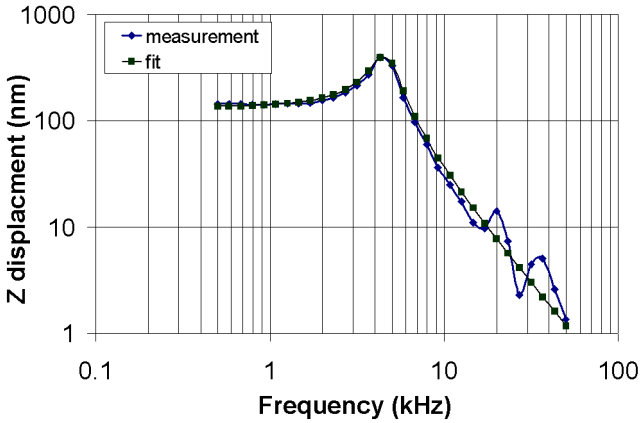


Figure 4.28 Measured noise floor of the device with variations in the master clock frequency.

Table 4.2: Performance summary of the accelerometer

Parameter	Value
Dimensions	500µm x 500µm
Proof Mass	200µm x 200µm (0.47 µg)
Spring Constant (FEA)	k_z = 0.198 N/m k_x = 1.93 N/m k_y = 2.12 N/m
Natural Frequency	5.48 kHz (FEA) 5.61 kHz (Measured)
Sense Capacitance	0.193 pF (Estimate)
Sensitivity	130 µV/G
Noise floor	0.7 mG/$\sqrt{Hz}$ @ f=1.5 MHz 3.5 mG/$\sqrt{Hz}$ @ f=140 kHz
D.C voltage variation	-16 mV/^{o}C or 1.7G/^{o}C
Percentage Sensitivity variation (30-100^{o}C)	103%



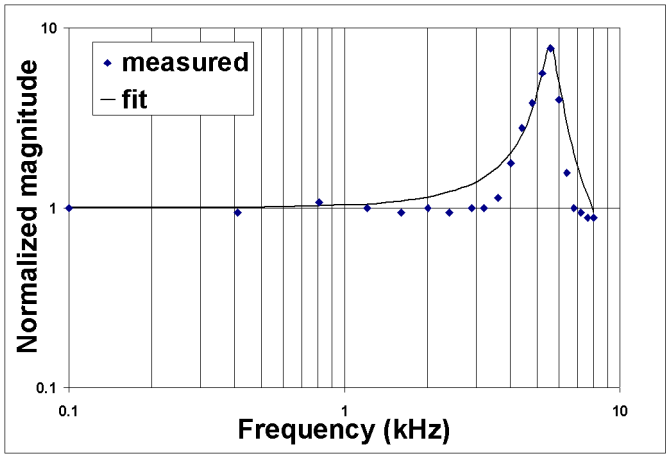
Fit Parameters

ω_n = 4.65kHz

Q_z = 3

Figure 4.29 Out-of-plane displacement measured using the MIT microvision. A second order response was fit to the measured data

turning on the reset transistor. The dominant mode of the sensor was out-of-plane at 4.65 kHz with a quality factor of 3, as shown in Figure 4.30. A slight lowering of the natural frequency is seen due to electrostatic spring softening. The mechanical frequency response of the accelerometer was also measured by changing the excitation frequency of the shaker table. The measurement yielded a resonant frequency of 5.61 kHz, with a quality factor of about 8. It should be noted that D.C. voltage is not applied during capacitance sensing. Therefore, no spring softening effect is seen with this measurement. The mechanical response measured using the circuits is shown in Figure 4.29.



Fit Parameters

ω_n = 5.61 kHz

Q_z = 8

Figure 4.30 The mechanical frequency response of the accelerometer measured using the capacitance measurement circuits. A second order response was fitted to the measured data to extract the natural frequency and the quality factor.

4.4.2 Characterization of Out-of-plane Comb Drive

The capacitance and the sensitivity of the device is dependent upon the relative displacement between the rotor and the stator, and that is determined by the device curl, which is a function of temperature. The change in capacitance as a function of relative curl can be characterized by changing the temperature of the rotor or the stator. The temperature of the rotor can be increased by joule heating of an embedded polysilicon resistor. The plot of the z-accelerometer capacitance with different rotor temperatures is shown in Figure 4.31a. The initial decrease in curl due to increase in temperature increases the overlap between the rotor and the stator, causing the capacitance to increase. At 138^{o}C, the capacitance reaches a maxima, and corresponds to the condition at which the rotor has the least curl. Further heating produces a convex rotor shape and a subsequent decrease in the capacitance. The sensitivity to external acceleration with rotor temperature, shown Figure 4.31b, reduces with increasing temperature as the overlap reduces. The sensitivity reaches a minima at the temperature at which the rotor is flat, and then changes sign to increase in magnitude with further rotor heating. Figure 4.31b only shows the magnitude of the sensitivity as the sign cannot be distinguished by the measurement circuit. This trend is qualitatively similar to the simulation results in Section 4.2.2. The curl of the structure is not uniform and quantitative measurements are difficult. A quantitative verification of out-of-plane capacitance change of an out-of-plane comb drive using a simplified thermally actuated capacitance test structures is described in [19].

4.5 Conclusions

A z-axis accelerometer based on a vertical comb drive along with temperature independent circuits were described. The capacitance measurement circuits based on a chopper-stabilization scheme, with known temperature independent gain, were designed and used to measure the device performance. The device D.C. offset and sensitivity are dependent on temperature. For such a device to be used over a wide temperature range, a temperature compensation scheme is needed. The next chapter describes the implementation of a temperature compensation scheme that maintains the device at a constant temperature, higher than the maximum operating temperature of the device, using embedded polysilicon heaters.

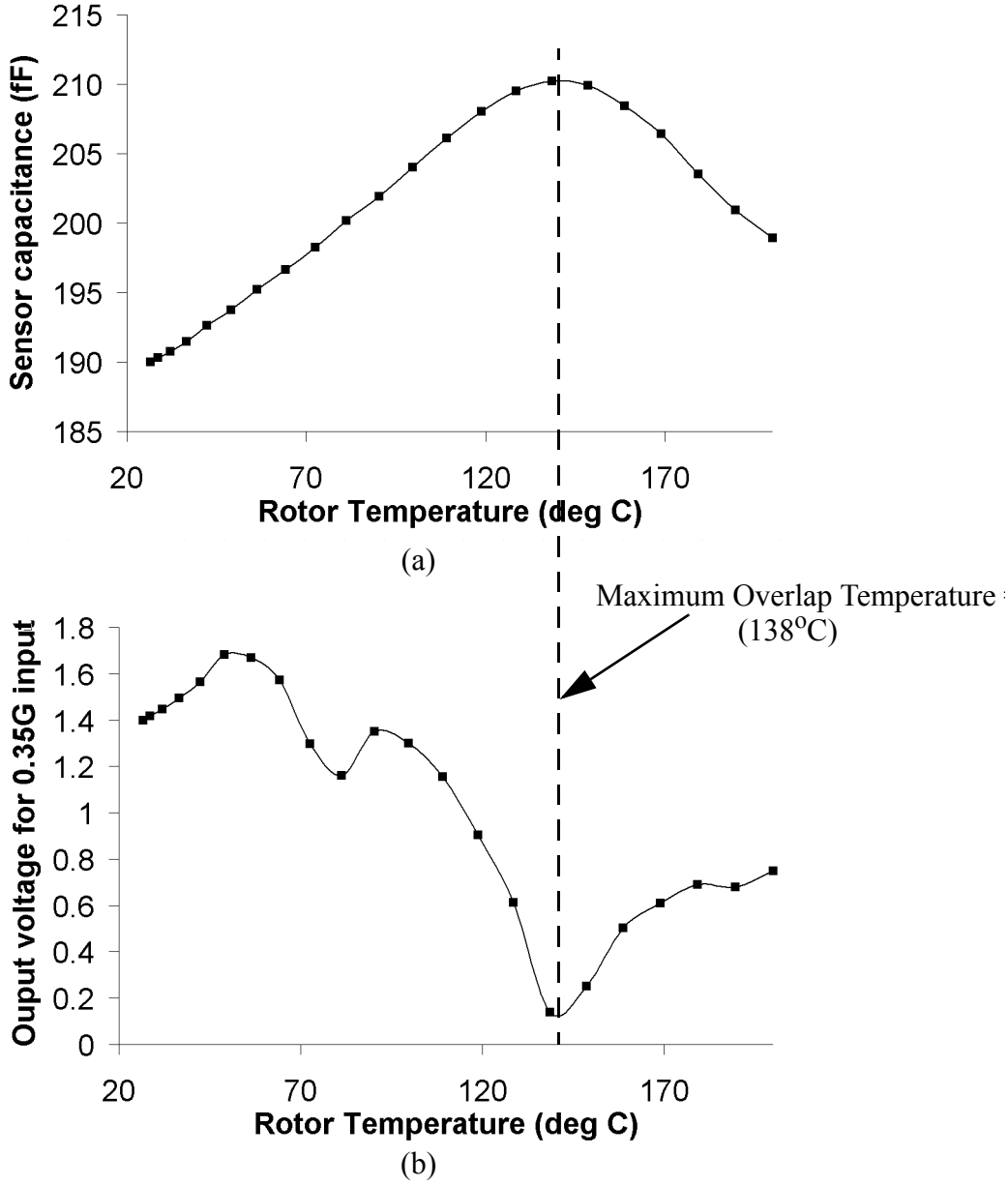


Figure 4.31 Measured variation of the (a) accelerometer D.C output voltage, and (b) sensitivity to external accelerations with rotor temperature. The offset between the rotor and the stator is a function of temperature.

Chapter 5. Temperature Stabilization of Z-axis Accelerometer

Residual stress gradients are an important consideration when designing microstructures made using the metal and the dielectric layers of CMOS process. Differences in stress produce internal bending moments that cause structures to curl in and out-of-plane. Design techniques have been proposed for design of mechanical structures that can compensate for structural curl, and improve device performance [7]. However, due to the large difference in thermal expansion coefficients of the aluminum (23μ/K) and the oxide (0.4μ/K) layers, the curl is a strong function of temperature. Therefore, the out-of-plane curl can cause variations over temperature in D.C. offset output and sensitivity of CMOS micromachined inertial devices. The situation is compounded by the dependence of in-plane curl on misalignments of the metal masks during the foundry CMOS fabrication. A temperature compensation scheme needs to be implemented to allow device operation over a wide ambient temperature range.

In this chapter, a temperature compensation technique that aims to keep the temperature of the device constant using integrated polysilicon resistors embedded in the device structure is described. Holding the device at a constant temperature rather than entire chip leads to lower power consumption and reduces packaging difficulties. A z-axis accelerometer sensitive to out-of-plane accelerations, described in Chapter 4, has been used as a testbed for demonstration of the temperature control scheme[85].

5.1 Temperature stabilization

There are several approaches to eliminate the temperature dependence of device performance. These include circuit compensation, dummy sensor compensation, and temperature stabilization. Temperature compensation using circuit techniques are based on look-up tables; the output voltage is calculated using predefined calibration coefficients and by the measurement of the

ambient temperature. If such a technique were to be used with CMOS micromachined sensors, then different calibration coefficients would have to be programmed for every device, as mask misalignment induced temperature dependency can vary from device to device. Temperature calibration and programming is expensive and can significantly increase the overall price of the sensor. In case of the sensor output in Figure 5.7, a fifth order fit would be required. The coefficients can also change with time and other environmental conditions, making the compensation less efficient.

Another common technique used in sensor design is the cancellation of temperature variations by use of a dummy sensor that does not respond to the measuring quantity, but responds identically to temperature variations. The schematic in Figure 5.1 illustrates the dummy sensor-based compensation scheme. This technique has been widely implemented in other z-accelerometer designs [84][86]. A reference z-axis accelerometer is designed to be identical to the main device, except that the motion between the rotor and the stator is restricted. Such a reference device cannot not track variations in z-offset changes between the rotor and the stator. This means that the use of a dummy device can only provide a limited cancellation of the temperature dependence.

Temperature stabilization schemes are based on the premise that effects of temperature on device performance can be eliminated if the device is held at a constant temperature. One method of maintaining a constant temperature is heating the device to a temperature greater than its maximum operating temperature. This approach is relatively low-cost as it can be implemented

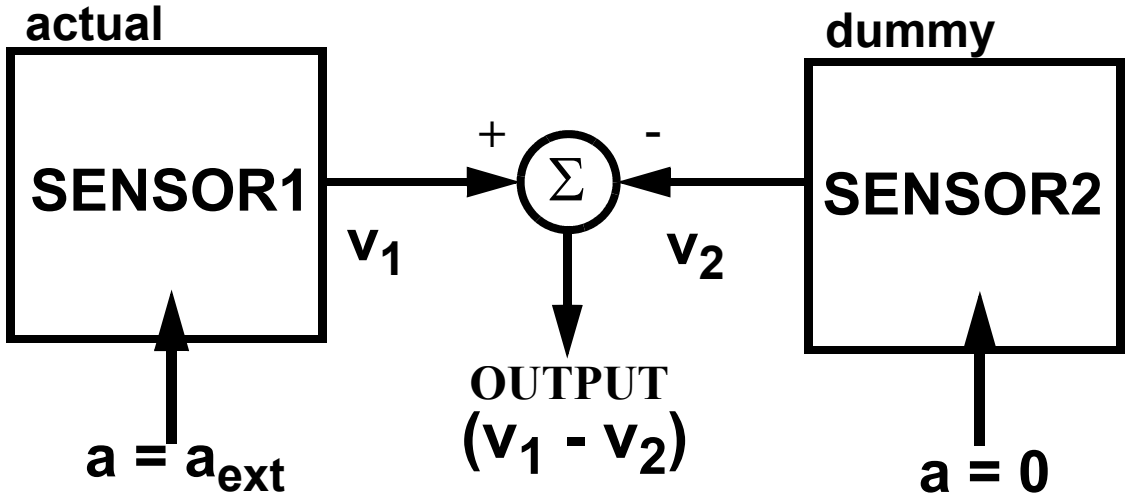


Figure 5.1 Cancelling temperature effects in sensor by use of a dummy sensor that is identical to the main sensor, except that is does not respond to the measuring quantity.

using resistive heaters. Heaters to control the frequency stability with temperature of devices have been used in commercial high quality quartz resonators and voltage references. In some cases the the device cannot be operated at an elevated temperature and must be controlled to the nominal operating temperature using a combination of heating and cooling. Thermo-electric coolers and heaters are used for temperature control of laser diodes for communication applications.

Temperature stabilization has also been applied to micro-devices. Integrated micro-heaters to stabilize temperature of surface acoustic wave (SAW) resonators were first proposed by White et al. [13]. Micro-heaters have been incorporated into film bulk acoustic resonators (FBAR) to improve the temperature performance [14]. Micro-heaters have also been integrated with silicon microprobes for thermal marking applications [15]. Researchers were able to raise the temperature of pig cortex by 50^{o}C using 6 mW of power for 2 minutes. Micro-oven temperature control has also been used to stabilize resonant frequency of polysilicon surface micromachined resonators placed in vacuum using less than 2 mW [16]. Thermal applications of polysilicon microbridges have been investigated by Mastrangelo [17] to design flow sensors, pressure sensors and as incandescent light sources.

5.1.1 Temperature Control using Micro-oven Control

Temperature control of many semiconductor devices is accomplished by setting the temperature of the entire chip to a constant higher temperature using a resistive heater integrated along with the package. This concept has been used for commercial voltage reference chips [87], in which the entire chip is packaged along with a resistive heater on a printed circuit board. This method has several disadvantages that preclude the use of this technique for low-cost sensor applications. The heated device has to be thermally isolated to minimize effects on other components placed on the printed circuit board. The power required for heating the chip and the package is high and often requires inclusion of high power driver transistors.

The solution presented here attempts to overcome some of the problems associated with chip-based temperature control schemes. We propose that by limiting the temperature control scheme to the sensor region, the power consumption and implementation difficulties can be over come. An integrated temperature control scheme transparent to the end user can be implemented. Integrated resistive heaters designed using the polysilicon of the CMOS are placed within the

device structure to stabilize its temperature. The resistivity change of polysilicon with temperature has been exploited for an *in situ* measurement of the device temperature. This localized heating of the microsensor region leads to simplification of control electronics. The control circuit, described in Section 5.3.3, is a simple constant resistance circuit that can be included on-chip, reducing the system cost.

5.1.2 Polysilicon as Heater and Temperature Sensor

Polysilicon is used as the gate material in CMOS processes, as well as for making on-chip resistors. There are two types of polysilicon in the Agilent 0.5 μm process [34]. The first is silicided polysilicon, which has a resistivity of 2.3 Ω/square, and the second is an unsilicided polysilicon with a resistivity of 130 Ω/square. For temperatures below 180^{o}C, the sensitivity of resistance as a function of temperature is linear and characterized by a temperature coefficient of resistance (TCR),

$$\alpha_p = \frac{R_T - R_{T_o}}{R_{T_o}(T - T_o)} \tag{5.1}$$

where, R_T is the is resistance at temperature T and R_{To} is the resistance at temperature T_o. Further details of the TCR measurement of polysilicon are presented in section Section 2.6. The TCR of the polysilicon is positive, enabling polysilicon heaters that can be driven by voltage sources without thermal run-away. Thermal run-away can occur in polysilicon resistors with negative TCR when they are driven by high voltage that produces a large temperature change due to joule heating in the resistor. The increased temperature causes the resistance to decrease, causing further heating as the current increases. The excessive V^2/R heating can eventually destroy the resistor. Resistors with positive coefficient of resistance can be heated by voltage sources, due to the inherent negative feedback.

To understand the heating effect due to polysilicon heaters embedded within CMOS micromachined structure, consider the cross-section in Figure 5.2. If the resistor, R_p, is heated by applying a constant voltage, V_h, per unit length, then the power dissipated due to Joule heating per unit length in the polysilicon layer of width w is

$$q = \frac{V_h^2}{R_p} = \frac{V_h^2 w}{R_{sq,p}} \tag{5.2}$$

where, $R_{sq,p}$ is the sheet resistance of the polysilicon in Ω/square. The thermal conductivity of the metal and the oxide layers is very large compared to that of the beam to the substrate though air (G_{air}). The temperature drop across the thickness of the beam the materials of the beam is therefore negligible. Therefore, the temperature of the beam cross-section is approximately the same as that of the polysilicon layer. The heat loss through radiation is neglected due to the low heating temperatures. The convection losses have been neglected as the air in the package is still, and therefore, cannot remove heat effectively. The energy balance equation is

$$C_{th}\frac{\mathrm{d}}{\mathrm{d}t}(T_p - T_s) + (T_p - T_s)G_{air} = \frac{V_h^2 w}{R_{sq,p0}(1+\alpha_p(T_p - T_s))} \quad , T_p = T_s \text{, at } t = 0 \tag{5.3}$$

where, C_{th} is the effective thermal heat capacity of the beam per unit length, obtained using (3.3), $R_{sq,p0}$ is the sheet resistance of the polysilicon at the initial or substrate temperature, T_s. An approximate solution of (5.3) for small temperature increase (T_p-$T_s << 1/\alpha_p$) is

$$T_p = T_s + \frac{V_h^2 w}{G_{air}R_{sq,p0}\left(1+\frac{\alpha_p V_h^2 w}{G_{air}R_{sq,p0}}\right)}\left(1 - e^{-\frac{G_{air}}{C_{th}}\left(1+\frac{\alpha_p V_h^2 w}{G_{air}R_{sq,p0}}\right)t}\right) \tag{5.4}$$

The thermal conductance of the beam, G_{air}, can be calculated analytically by solving the field problem for a heated beam placed at distance g_s above the substrate [88]. An approximate solution for just the bottom surface, is expressed as

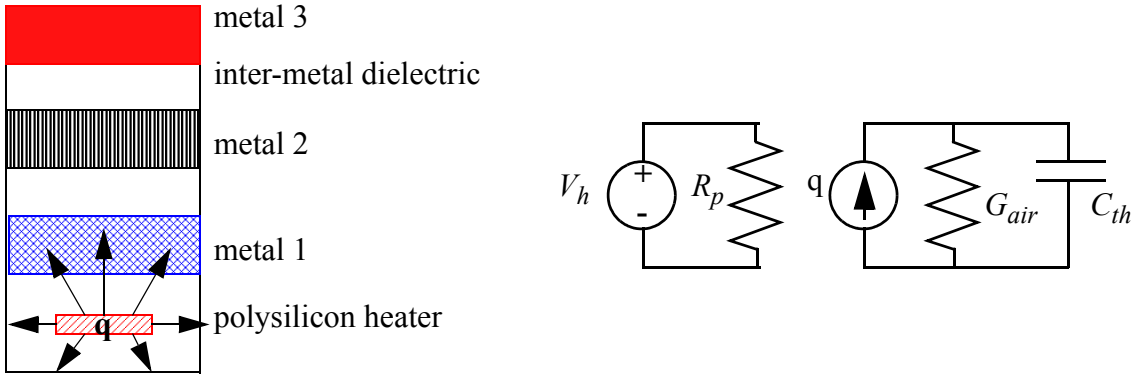


Figure 5.2 Cross-section of the beam and its electro-thermal equivalent circuit

$$G_{air} = \frac{2}{\pi k_{air}} \ln \frac{3}{1 + 2\cosh\left(1 + \frac{w\pi}{2t_i} + \pi 3^{-\frac{3}{2}}\right)} \tag{5.5}$$

The change in temperature of the beam is proportional to the square of the applied voltage. The expression in (5.4) stable for all positive values of α_p.

5.2 Integrated Temperature Stabilization CMOS Devices

A temperature control scheme for a CMOS micromachined device consists of a servo-circuit that keeps the average temperature of the heater constant. Heater resistance is a measure of the temperature of the beam. The heater is distributed within the device structure to maintain a uniform temperature distribution. Presence of temperature gradients makes the device curl dependent on the ambient temperature. If a uniform temperature is ensured, then the average temperature measured in the heaters is the true temperature of the device. To design a uniform temperature distribution, the heat conduction through the anchors must be minimized.

5.2.1 Temperature Control of CMOS Micromachined Beam

To illustrate the trade-off in temperature control design in CMOS micromachined devices, consider the temperature stabilization of a single beam fixed on both ends as shown in Figure 5.3. There are 3 distinct regions in the simple temperature controlled beam:

1. The substrate anchor region is made of high thermal conductivity silicon and is assumed to be the same temperature as that of the chip.

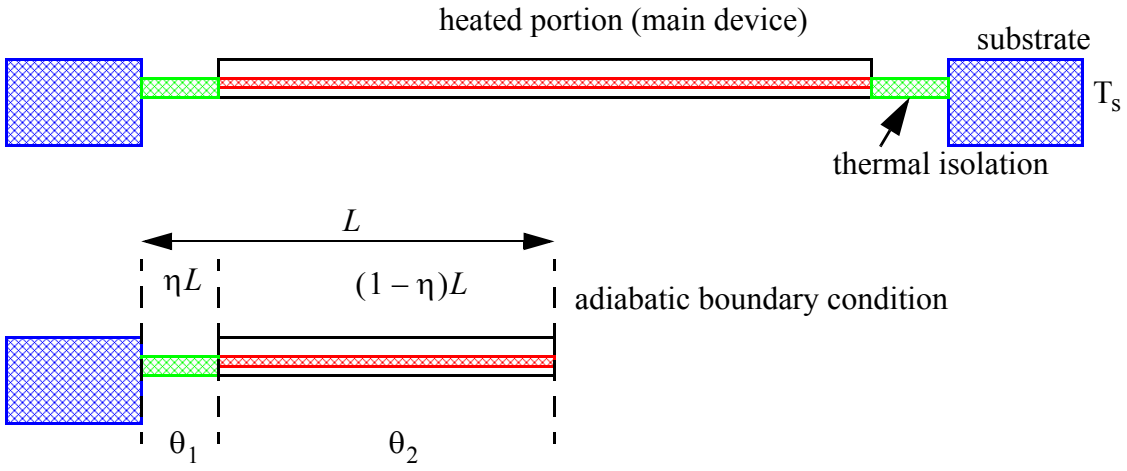


Figure 5.3 Illustration of a simple CMOS micromachined beam with a temperature controlled section, and with thermal isolation at the ends.

2. The thermal isolation regions of the beam are designed to minimize thermal losses to the substrate.

3. The central part of the beam with uniformly embedded polysilicon heaters.

Let *2L* be the length of the beam, with ηL being the length of the thermal isolation region. Heat loss in the thermal isolation region occurs due to conduction through air. Applying the energy balance equation, in a small length *dx*, we can write the differential equation for excess temperature, θ_1, at any point along the thermal isolation region as

$$\kappa_1 A_1 \frac{d^2}{dx^2}\theta_1(x) - G_{air1}\theta_1(x) = 0, \quad 0 < x < \eta L \quad \text{, and } \theta_1(x) = T_1(x) - T_s \tag{5.6}$$

where, κ_1 and A_1 are the thermal conductivities and cross-sectional area, respectively, of the thermal isolation region, and G_{air1} is the thermal conductance per unit length to the substrate through air. In the region with the embedded polysilicon heater, a heat source is added to (5.6). The heat dissipated per unit length, for a voltage V_h applied per unit length across the polysilicon resistor, is given by

$$q = \frac{w_{2p} V_h^2}{R_{sq,p0}(1 + \alpha_p \theta_2(x))} \tag{5.7}$$

where, w_{2p} is the width of the polysilicon heater, and θ_2 is the temperature of the central part of the beam. The differential equation for θ_2 is expressed as

$$k_2 A_2 \frac{d^2}{dx^2}\theta_2(x) - G_{air2}\theta_2(x) + \frac{w_{2p} V_h^2}{R_{sq,p0}(1 + \alpha_p \theta_2(x))} = 0, \text{ for } \eta L < x < L, \text{ and}$$
$$\theta_2(x) = T_2(x) - T_s \tag{5.8}$$

To solve the differential equations, the following boundary conditions are applied.

$$\theta_1(x) = 0 \quad \text{, at } x = 0 \tag{5.9}$$

$$\theta_1(x) = \theta_2(x), \text{ at } x = \eta L \tag{5.10}$$

$$\kappa_1 \frac{d}{dx}(\theta_1(x)) = \kappa_2 \frac{d}{dx}(\theta_2(x)), \text{ at } x = \eta L \tag{5.11}$$

$$\frac{d}{dx}\theta_2(x) = 0, \text{ at } x = L \tag{5.12}$$

Equation (5.12), is obtained by exploiting the symmetry, and recognizing that as the net heat flow is zero at the center. The solution of (5.8) for small temperature changes ($\theta_2 << 1/\alpha_p$) is given by

$$T_1(x) - T_s = \frac{\kappa_2 A_2 m_2}{\kappa_1 A_1 m_1}\left(\frac{C_o}{\delta}\right)\left(\frac{\sinh(m_1 x)}{\cosh(m_1 \eta L)}\right), \quad 0 < x < \eta L \tag{5.13}$$

$$T_2(x) - T_s = \left(\frac{C_o}{\delta}\right)\left(\frac{\cosh(m_2(L-x))}{\sinh(m_2 L(1-\eta))}\right) + C_o \tag{5.14}$$

where,

$$m_1 = \sqrt{\frac{G_{air1}}{\kappa_1 A_1}}, \; m_2 = \sqrt{\frac{G_{air2}}{\kappa_2 A_2}\left(1 + \frac{\alpha_p w_{2p} V_h^2}{R_{sq,p0} G_{air2}}\right)}, \; C_o = \frac{w_{2p} V_h^2}{m_2^2 R_{sq,p0} \kappa_2 A_2}, \text{ and} \tag{5.15}$$

$$\delta = \coth(m_2(1-\eta)L) + \frac{\kappa_2 A_2 m_2}{\kappa_1 A_1 m_1}\tanh(m_1 \eta L) \tag{5.16}$$

The resistance of the polysilicon embedded in the heated section of the beam is determined by the temperature distribution θ_2, and is calculated as

$$R_{poly} = \frac{R_{sq,p0}}{w_{2p}}\int_{\eta L}^{L}(1 + \alpha_p \theta_2(x))dx = \frac{R_{sq,p0}(1-\eta)L}{w_{2p}}(1 + \alpha_p \theta_{av}) \tag{5.17}$$

where the θ_{av} is the mean temperature of the heated section of the beam, given by

$$\theta_{av} = C_o\left(1 - \frac{1}{\delta m_2 L(1-\eta)}\right) + T_s \tag{5.18}$$

The measured resistance is the indicator of the average temperature of the heated region. The temperature controller works by maintaining the resistance of the beam constant. The controller can therefore only keep the average temperature of the heated section constant. The actual temperature distribution in the heated region is determined by the thermal properties of the beam. Proper design of the thermal isolation can have a significant effect on the temperature distribution in the heated region. The temperature profile is shown in Figure 5.4 of a 200 μm beam with a 20 μm metal-1 thermal isolation region with cross-section of 2 μm x 2 μm, and a heated M123-P section 160 μm long, 5 μm thick and 5 μm wide with a 2 μm wide embedded polysilicon heater. The profile is compared to that of a 200 μm-long, 5 μm-thick and 5 μm-wide beam made with

M123-P, embedded polysilicon heater without any thermal isolation. The case with thermal isolation yields better uniformity and lower power dissipation.

The variation in the temperature profile with changes in ambient temperature is seen in Figure 5.5. The presence of thermal isolation also reduces the dependence of temperature gradient on the ambient temperature. The ambient temperature dependence of the temperature profile can be minimized by decreasing the thermal conductivity of the isolation region. Design of isolation is a trade-off between achieving the lowest thermal conductivity, while maintaining good electrical connection between the sensor and the interface circuits. Thermal isolation can be designed in the CMOS process by minimizing the width, thickness and the overall metal content of the isolation beam section. Thin metal-1 beams provide good thermal isolation, while maintaining good electrical connection. A further discussion on design of thermal isolation in the CMOS process is presented in Section 3.3.1.

Another technique to improve the temperature distribution in the heated section is adjustment of the heat dissipation in different regions by varying the width of the heating resistors. The heating per unit length is given by (5.7), where w_{2p} can be function of position, x. By careful design, the widths of the heater resistors can create a heating profile that is the exact inverse of the

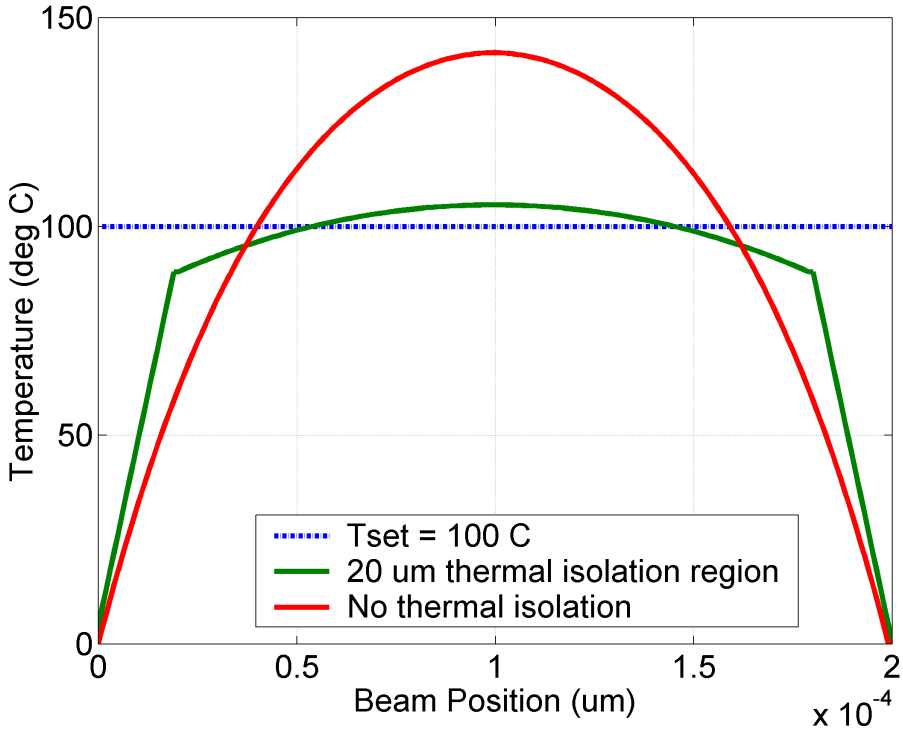


Figure 5.4 Temperature profile of a heated beam with and without thermal isolation is compared for temperature control of 100°C.

temperature distribution due to uniform heating. The calculation of the exact width distribution that would yield the most uniform temperature profile requires solving (5.8) with the heat generation per unit length as expressed in (5.7). This is accomplished by numerical optimization techniques discussed.

5.3 Temperature Stabilization of the Z-axis Accelerometer

The integrated temperature control scheme proposed was demonstrated on the z-axis accelerometer described in Chapter 4. The variation of z-axis accelerometer curl with change in temperature is illustrated by the measurement of the device at different rotor temperatures. The rotor was heated by joule heating of an embedded polysilicon heater. The curl was measured using a WYKO white-light interferometer [73]. The relative displacement between the rotor and stator fingers is seen to decrease with increase in temperature in Figure 5.6. The changes in overlap affects the D.C. offset of the measured acceleration, leading to large errors in D.C. measurements. The change in the D.C. offset with changes in ambient temperature is shown in Figure 5.7. The change in D.C. voltage corresponds to an acceleration input of 1.7 G/^{o}C, which underscores the need for temperature stabilization. Other in-plane sensing devices designed in the

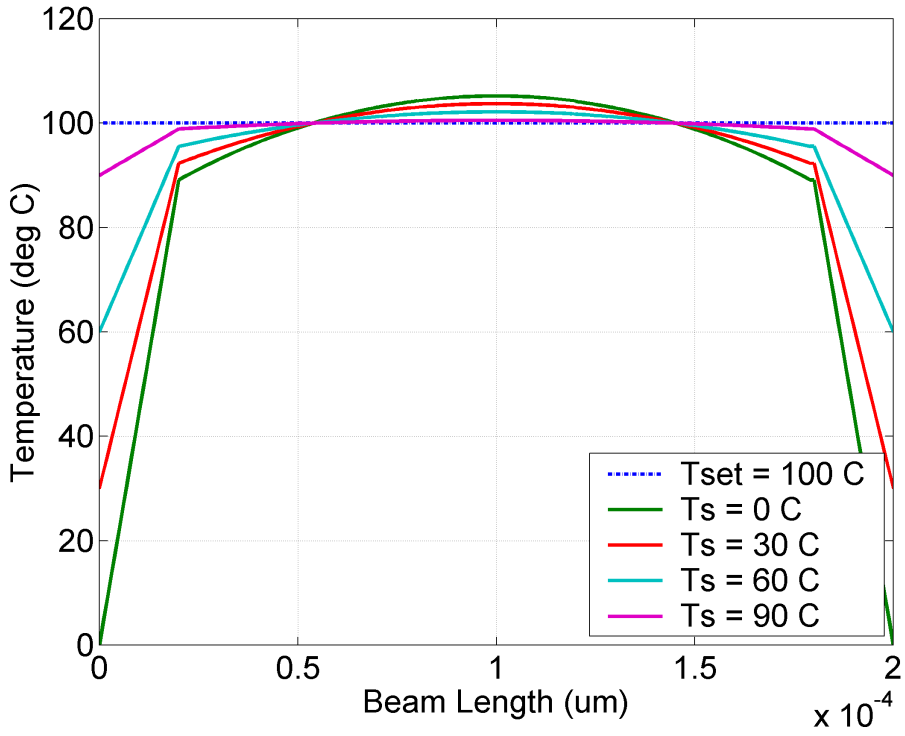


Figure 5.5 Performance of the temperature controller with changing ambient temperature. The temperature profile is depends upon the substrate temperature.

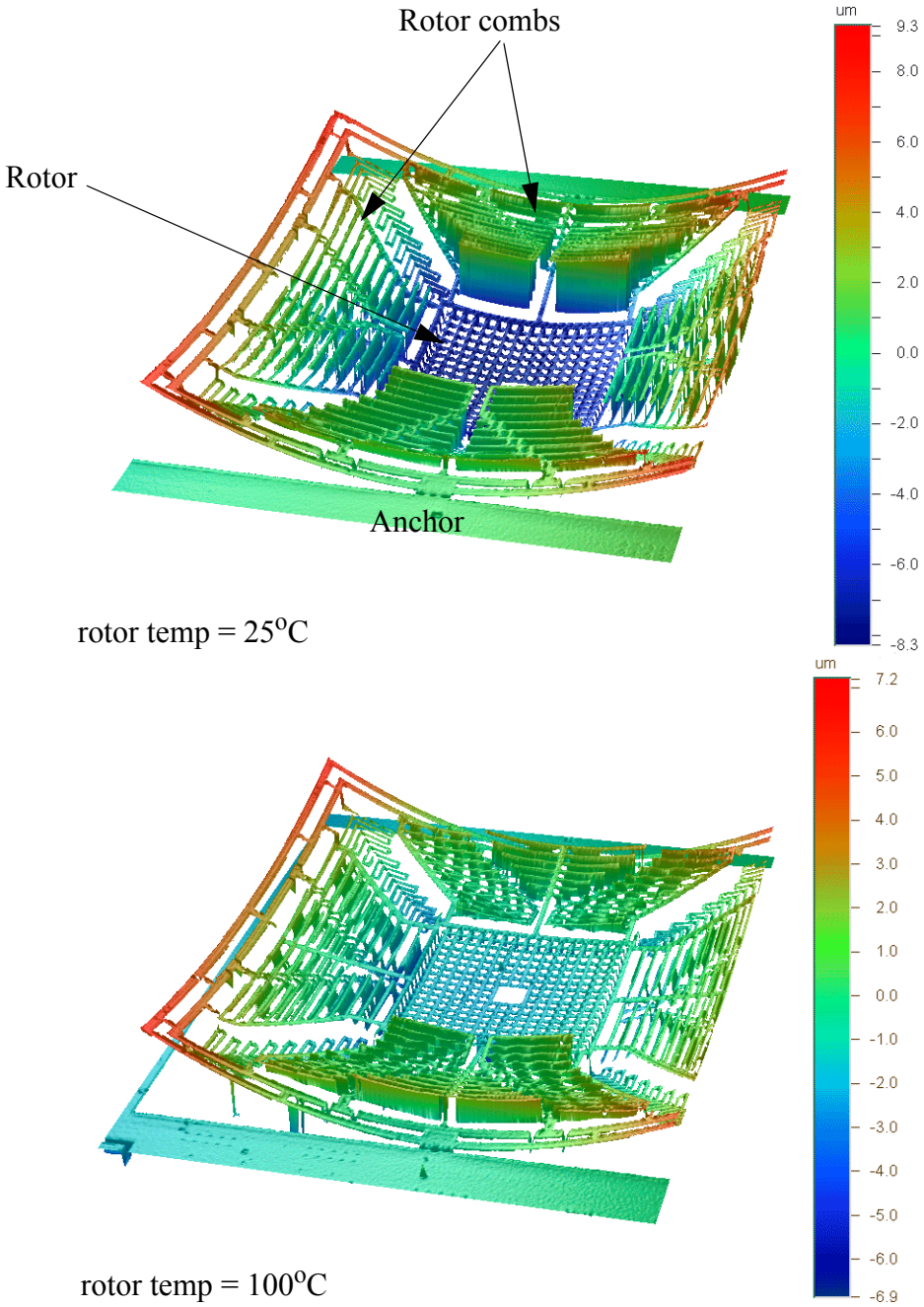


Figure 5.6 The change in structural curl due to a rotor temperature change from 25°C to 100°C. The rotor temperature was change by joule heating of the rotor resistor.

CMOS micromachining process do not have such large temperature dependency as they reject effects of temperature changes as a common-mode signal. For example, the lateral accelerometer described in [5], has a fully differential capacitance bridge sense element with a common centroid layout, in which all the capacitors are affected equally by device curl change with temperature. However, mask misalignment induced temperature-dependent lateral curl effect will not be cancelled.

5.3.1 Uniform Temperature Distribution

To obtain a uniform temperature distribution across the accelerometer, three independent heaters are embedded in the stator frame, rotor proof-mass and the rotor comb fingers. The placement of the heaters is shown in Figure 5.8 The average temperature in each of the heaters is set independently. The dissipation per unit volume of the device for a given voltage applied across the heater is set through feedback controls the heater resistance. The use of the independent heaters provides extra flexibility to achieve a uniform temperature distribution.

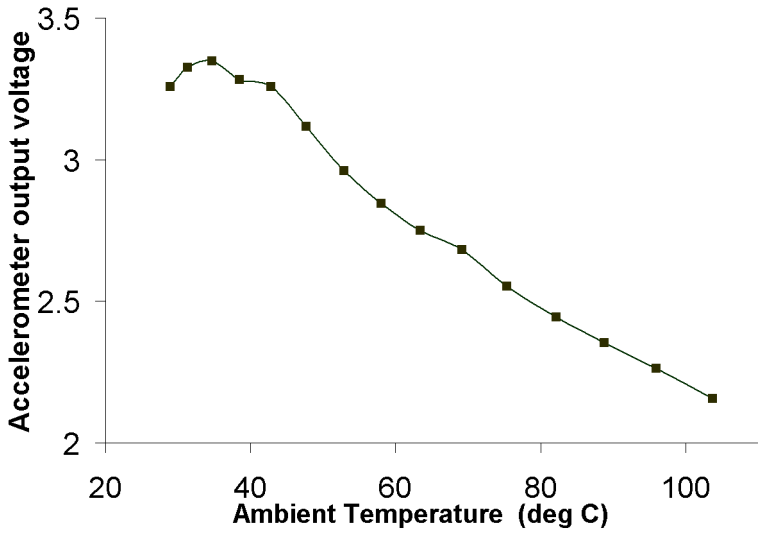


Figure 5.7 Variation of the output D.C. offset of the accelerometer with change in ambient temperature.

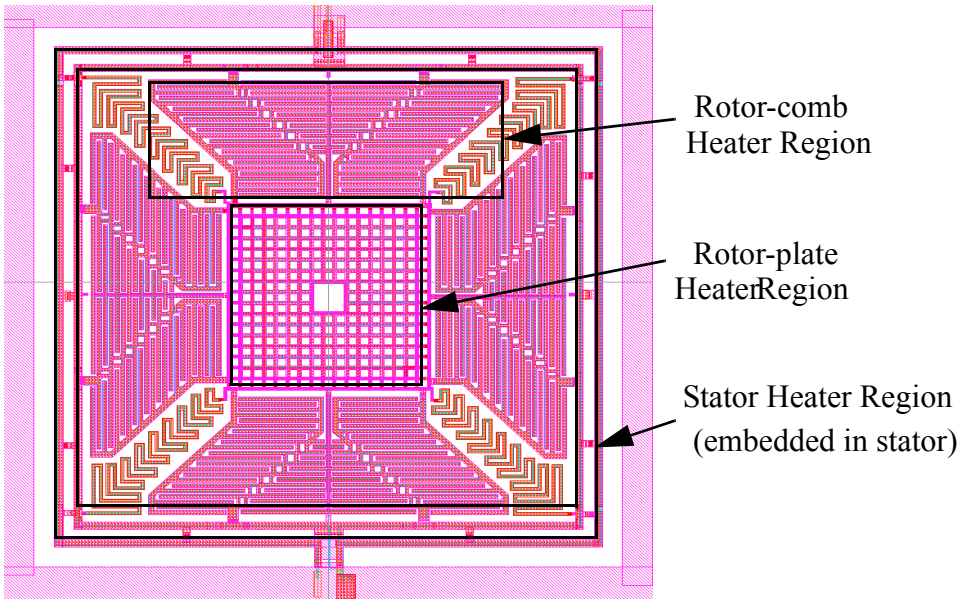


Figure 5.8 The layout of the accelerometer showing the rotor-plate, stator and the rotor-comb heater regions. The heater consists of embedded polysilicon resistors, designed to provide an uniform heat distribution.

Placement of Polysilicon heaters

The placement of the polysilicon heaters within the structure is difficult to optimize due to the the constraints placed by routing of wires to the heaters and electrical coupling concerns due to placement of polysilicon heaters very close to the high impedance sense nodes. To ensure that a surface is uniformly heated a regular placement of heaters is required. As mentioned previously, the heat loss through conduction through air dominates and the temperature profile is determined by this distributed heat loss mechanism. To develop an insight into the resistor placement, consider the two-dimensional temperature distribution of a plate with embedded strip heaters as illustrated in Figure 5.9. Such a uniform placement was used for heating the proof mass of a CMOS micromachined sensor. To maintain the most uniform temperature distribution in a plate, strip heaters are placed at regular intervals, $2x_o$ apart. The temperature of each heater is controlled to T_p by a temperature controller circuit. For simplicity we will assume that a large number of strip heaters are placed. Then, exploiting the symmetry of the structure, an adiabatic boundary condition occurs in one half, the steady-state heat conduction equation can be written as

$$\kappa_{m123} t_{m123} \frac{d^2}{dx^2} T(x) + \left(\frac{\kappa_{gap}}{t_{gap}}\right)(T(x) - T_s) = 0 \quad , 0 < x < x_o \tag{5.19}$$

with boundary conditions:

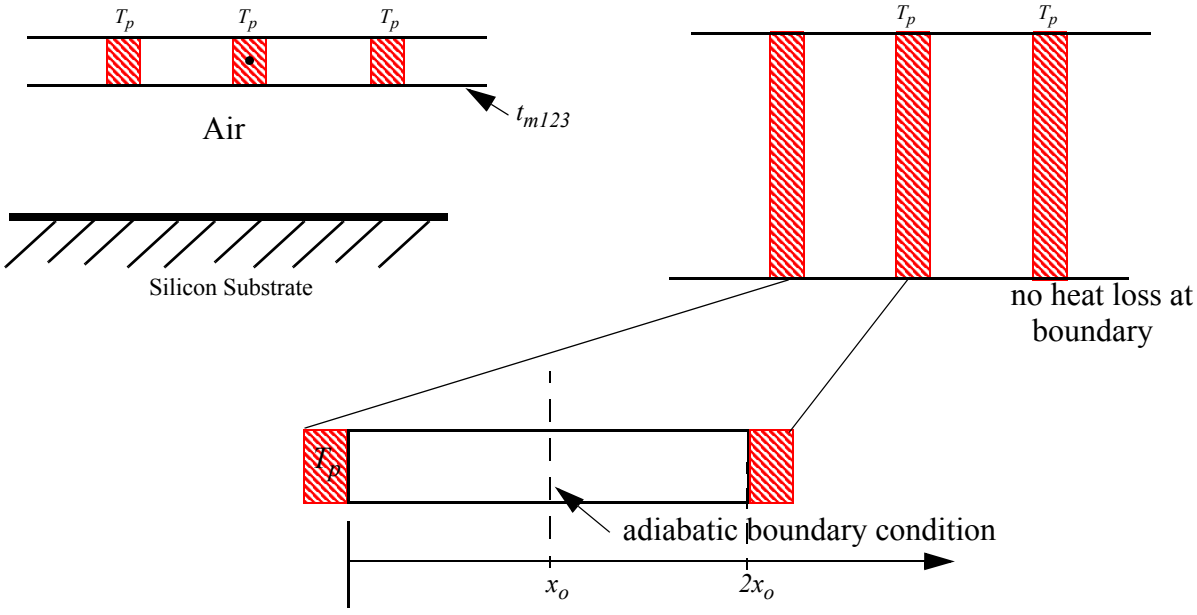


Figure 5.9 Temperature distribution for a infinite m123 plate heated by uniformly placed strip heaters. (a) Cross-sectional view, and (b) top view of the structure. (c) The simplification of the thermal equation using symmetry.

$$T(x) = T_p, \text{ at } x = 0, \tag{5.20}$$

$$\frac{\mathrm{d}}{\mathrm{d}x}T(x) = 0, \text{ at } x = x_o \tag{5.21}$$

The solution of (5.19) can be written as

$$T(x) = T_p - (T_p - T_s)\left(1 - \frac{\cosh\left(\frac{x - x_o}{L_h}\right)}{\cosh\left(\frac{x_o}{L_h}\right)}\right), \quad 0 < x < x_o \tag{5.22}$$

where t_g is the separation of the plate from the substrate

$$L_h = \sqrt{\frac{\kappa_{m123} t_{m123} t_g}{\kappa_{air}}} \tag{5.23}$$

and L_h is called the healing length. At a distance L_h away from the polysilicon heater, the heat conducted due to lateral conduction through the plate is equal to that lost to the substrate. This healing length is seen in solutions of the steady-state heat flow equation for various boundary conditions. The temperature profile between two heaters on the plate at 100°C, with a substrate

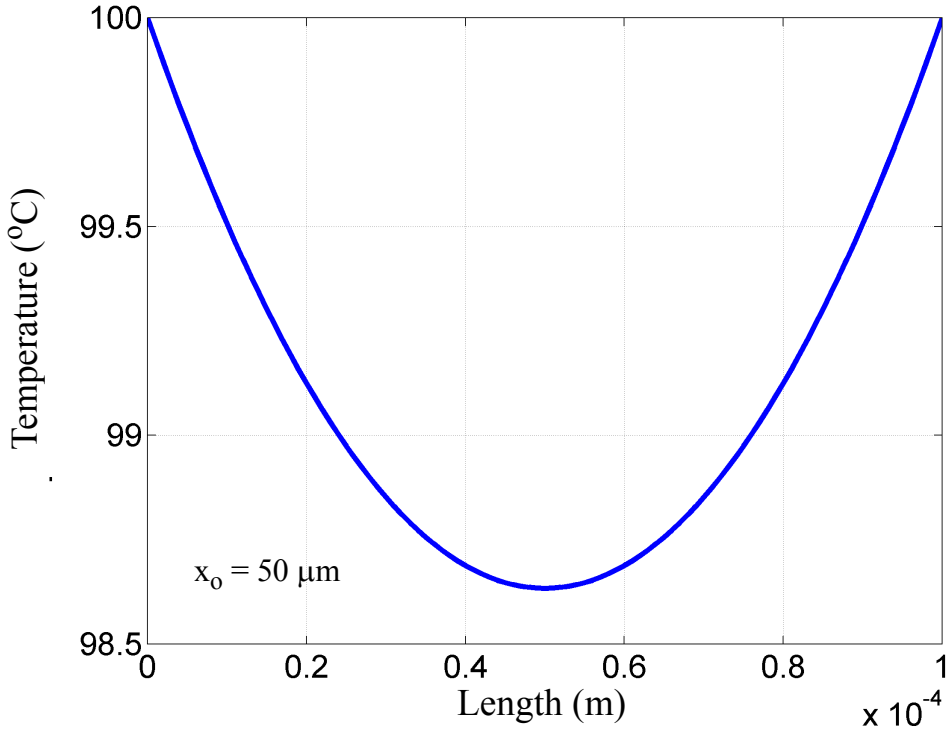


Figure 5.10 Temperature profile between two heaters placed 100 μm apart on a metal-123 plate. The healing length in this case is 270 μm.

temperature of 20°C, placed 100 μm apart on a metal 1,2, and 3 plate, 6 μm from the substrate, is shown in Figure 5.10. The healing length, L_h, for this case is 270 μm. The maximum temperature variation, ΔT_{max} across the plate for $x_o << L_h$ is

$$\frac{\Delta T_{max}}{T_p} = \frac{x_o^2 (T_p - T_s)}{2 L_h^2 T_p} \tag{5.24}$$

A distance of 100 μm between the polysilicon heaters ensures that the temperature profile is uniform to within 1.5%. Polysilicon heater placement for the three independent heaters in the accelerometer was guided by this concept of healing length. The heater resistors are placed on the edges of the rotor proof mass in the combs. The stator is thin, and therefore a heating resistor is placed in its entire length.

Optimization Of Heater Geometry

Once the placement of the heater was determined from the insights gained from analysis in the previous section, an optimization of the heater wire widths was performed. The width optimization using a commercial finite element simulation is time consuming and cannot be included in a practical iterative loop. The analysis of the temperature distribution within the loop of the optimization algorithm must be fast; therefore, a finite difference approximation was used for solution of conduction heat transfer problem. An equivalent electrical circuit representation of the thermal problem [89] was implemented and solved in SPICE.

To create an electrical equivalent circuit representation for the entire structure, the structure is divided into small elements. Consider an small volume of dimensions $2\Delta x$, $2\Delta y$, and $2\Delta z$, with a heat source q_v. The equivalent circuit representation for each element is shown in Figure 5.11, along with the dimensions of the element. To solve the temperature distribution, the energy generated within the element is equated to the energy lost, and the energy balance equation is

$$\kappa_{av}\frac{\partial^2 T}{\partial x^2} + \kappa_{av}\frac{\partial^2 T}{\partial y^2} + \kappa_{av}\frac{\partial^2 T}{\partial z^2} + \frac{q_v}{\Delta x \Delta y \Delta z} + G_{air}(T - T_s) = \rho_v c\left(\frac{\partial T}{\partial t}\right) \tag{5.25}$$

The solution of the above in all three dimensions with arbitrary boundary conditions yields the temperature distribution of the device, and can be found by a using a finite difference approximation technique. The second derivative in x can be expressed in term of thermal resistances, as

$$\kappa_{av}\frac{\partial^2 T}{\partial x^2} = \kappa_{av}\left(\frac{T_{x1}+T_{x2}-2T_c}{\left(\frac{\Delta x}{2}\right)\Delta x}\right) = \frac{1}{\Delta x\Delta y\Delta z}\left(\frac{T_{x1}-T_c}{R_x}-\frac{T_c-T_{x1}}{R_x}\right), \tag{5.26}$$

where $R_x = \dfrac{\Delta x}{2k_{av}\Delta y\Delta z}$. Similar expressions can be written for each of the dimension of the element, and (5.25) can then be rewritten in analogy to Kirchhoff's current equation as,

$$\left(\frac{T_{x1}-T_c}{R_x}-\frac{T_c-T_{x1}}{R_x}+\frac{T_{y1}-T_c}{R_y}-\frac{T_c-T_{y1}}{R_y}+\frac{T_{z1}-T_c}{R_z}-\frac{T_c-T_{z1}}{R_z}\right)+q_v+\frac{T_c-T_{z1}}{R_{air}} = C_e\frac{\mathrm{d}T_c}{\mathrm{d}t} \tag{5.27}$$

where,

$$R_y = \frac{\Delta y}{2\kappa_{av}\Delta x\Delta z}, \tag{5.28}$$

$$R_x = \frac{\Delta z}{2\kappa_{av}\Delta x\Delta y}, \tag{5.29}$$

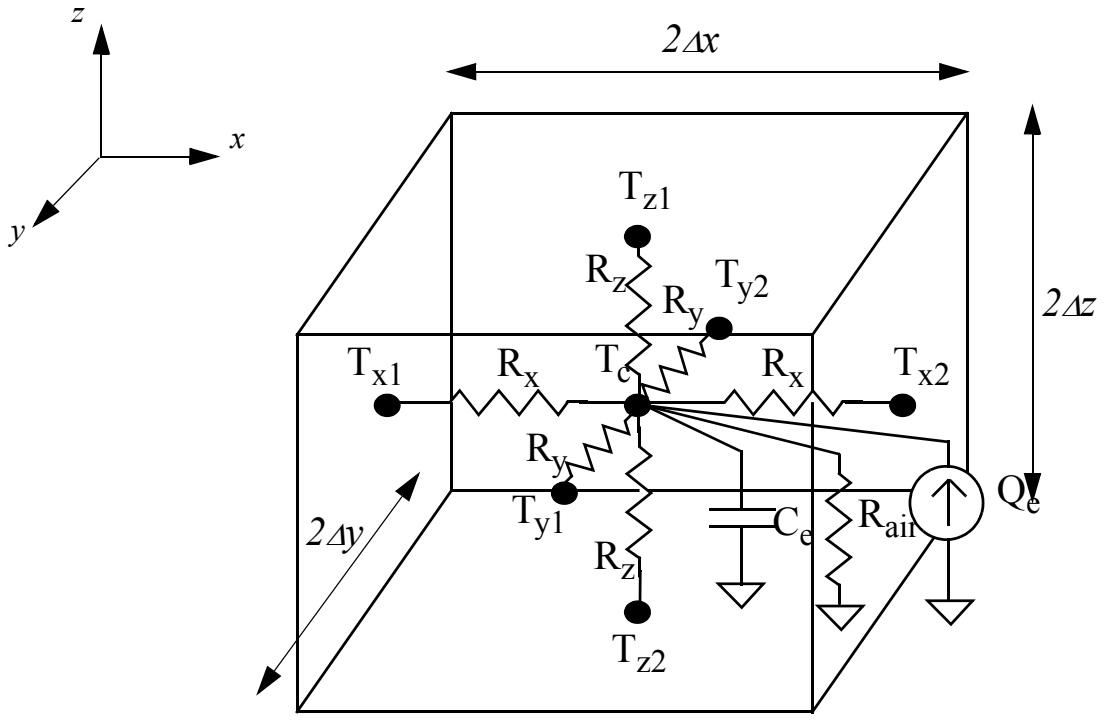


Figure 5.11 Equivalent circuit representation of a differential thermal element of the CMOS structure, with dimensions *2Δx*, *2Δy*, and *2Δz*, constructed using average values of thermal conductivity and thermal heat capacity.

$$R_{air} = \frac{t_g}{\kappa_{air}\Delta x\Delta y}, \tag{5.30}$$

$$\text{and } C_e = \rho_v(\Delta x\Delta y\Delta z)c \tag{5.31}$$

Drawing an analogy between temperature and voltage; and between heat flow and current, the equivalent electrical representation of the thermal element can be solved using the SPICE circuit simulator. The polysilicon heater power generation within the volume is represented by an equivalent current source in SPICE of value

$$Q_e = I^2 R_{sq,p}\frac{\Delta L_p}{\Delta w_p} \tag{5.32}$$

where ΔL_p is the length of the polysilicon wire embedded in the element (equal to Δx or Δy, depending on the direction of current flow in the polysilicon heater within the element) and Δw_p is the width of the polysilicon wire in that region. Heat generation is independent of the temperature, and the system is therefore linear. An equivalent representation can automatically be obtained from a layout representation of the structure using the auto-meshing technique described in Chapter 2. The values of the components of the equivalent circuits are computed from the average thermal properties of the type of beam material (such as m12 or m123 etc.) computed using the expressions in Chapter 3.

The optimization algorithm aims to achieve the most uniform temperature distribution across the device by minimizing the standard deviation of temperature at all nodes, for a current flow of 1 mA through the polysilicon heaters. The temperature distribution is determined by the heat dissipated by each heater element. The heat generation within each element is inversely proportional to the width of the polysilicon heater, as seen in (5.32). To speed up the optimization process, the algorithm uses the superposition principle. For a linear circuit, the final node voltages are the sum of node voltages calculated with only one source connected at a time. The temperature distribution due to each heater is obtained by setting all the other heater resistors to zero. Let $T_1(x,y)$, $T_2(x,y)$, ... $T_i(x,y)$, ... $T_n(x,y)$ be the temperature distributions calculated for each of the heater resistors: $R_{h1}, R_{h2}, \ldots R_{hi}, \ldots R_{hn}$, having their width set to $w_{h0} = 1\mu m$. The temperature distributions for the *i-th* resistor width, w_{hi}, can be calculated as

$$T_{i,w_{hi}}(x,y) = T_i(x,y)\left(\frac{w_{h0}}{w_{hi}}\right) \tag{5.33}$$

Using the superposition principle the temperature distribution for the entire structure, $T_{total}(x,y)$ can be calculated for heater resistor widths w_{h1}, ... w_{hi}, ... w_{hn} as

$$T_{total}(x,y) = \sum_{i=1}^{n} T_i(x,y)\left(\frac{w_{h0}}{w_{hi}}\right) \tag{5.34}$$

The entire temperature distribution can be pre-computed by a single SPICE computation for each heater resistor, and does not need to be run inside the optimization loop. This ensures that the simulation is very fast. The cost function to be minimized by the optimization algorithm is

$$CF = \left(T_{total}(x,y) - \overline{T_{total}}\right)^2 \tag{5.35}$$

The optimization is constrained by minimum and maximum widths of the polysilicon resistors that can be fabricated, which in the Agilent 0.5 μm process is 0.6 μm < w_h < (Beam width - 0.6 μm). The optimized values for w_{h1}, ... w_{hi}, ... w_{hn} are computed using the modified Levenberg algorithm [90]. The optimization of the rotor temperature distribution was carried out with a choice between eight different widths of resistors. The stator was assumed to be kept at a fixed temperature (20 ^{o}C). The placement of the rotor resistors is shown in Figure 5.12. The temperature distribution before optimization (all heaters with width = w_{h0} = 1μm) and after

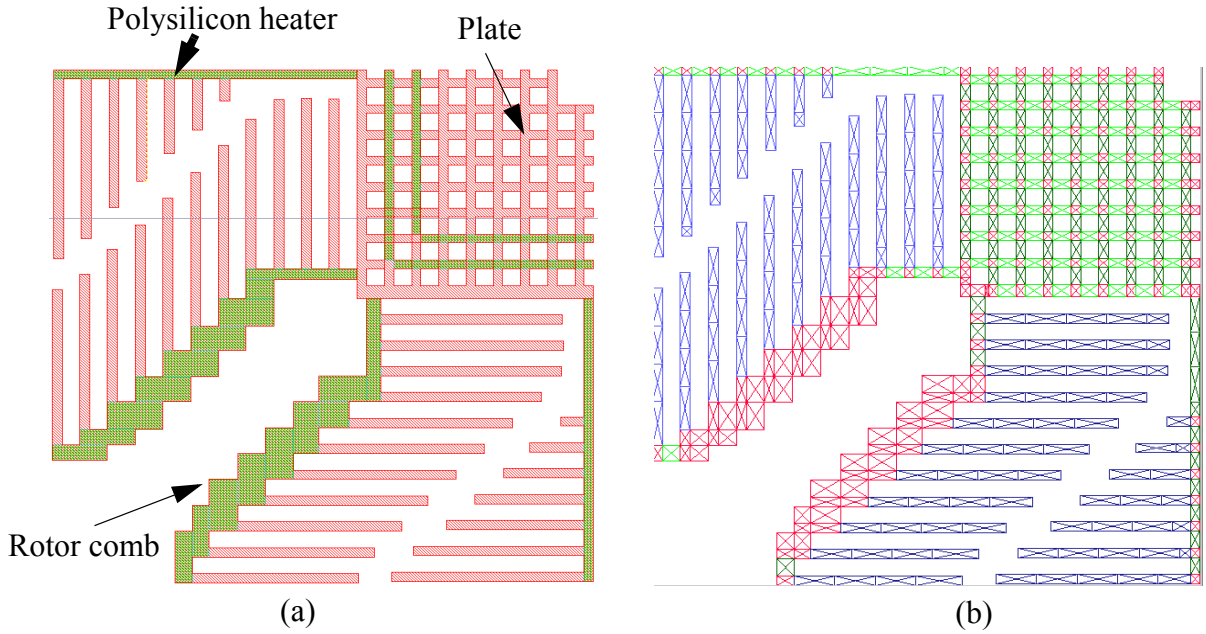


Figure 5.12 (a) Placement of the heaters within the rotor, and (b) the automatically generated mesh. Each element is replaced by the equivalent circuit representation of Figure 5.11

optimization is shown in Figure 5.13. The standard deviation before the optimization was 5.5 K, and was reduced to 0.9 K after the optimization.

The results of this optimization indicate it was possible to obtain a uniform rotor temperature distribution using a single heater on the rotor. However, due to routing limitations and the fact that conduction through air between the rotor and stator fingers was neglected in the optimization, a separate heater for the rotor comb fingers was included. The temperature distribution due to the proof mass heating was measured using a thermal imaging microscope is shown in Figure 5.14. The temperature drop due to the thermal conduction losses in the rotor comb fingers is seen, justifying the need for inclusion of rotor comb finger heaters.

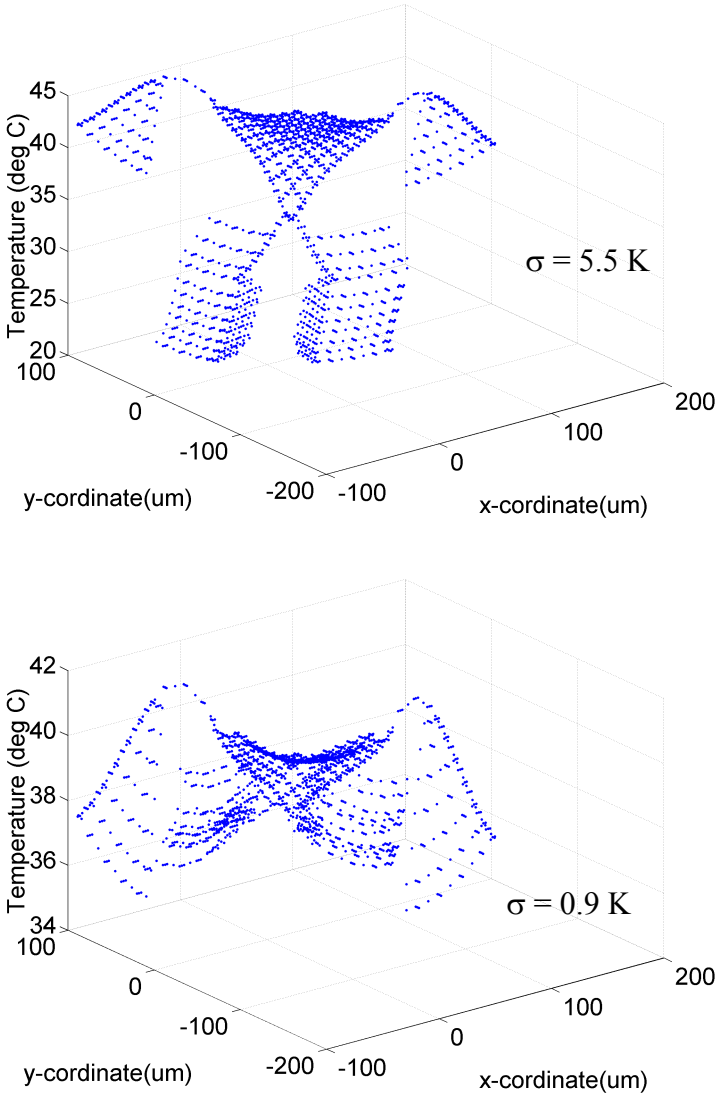


Figure 5.13 Temperature distribution due to rotor heating:. (a) Before optimization of the heater geometry (σ = 5.5 K), and (b) After optimization (σ = 0.9 K), for 1 mA of heater current.

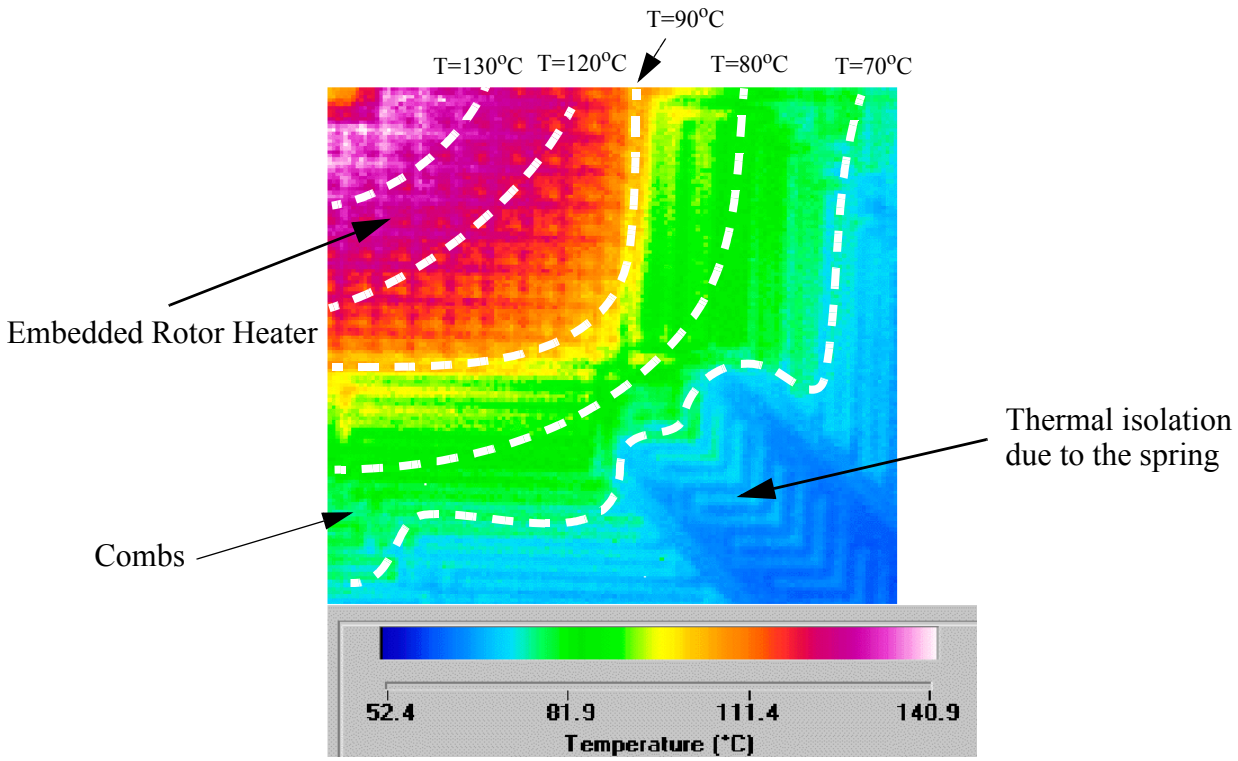


Figure 5.14 Measured temperature distribution due to rotor heating, measured by an infrared microscope.

5.3.2 Thermal Time Constant

The thermal time constant of the device is determined by the thermal conductance of the device to the substrate and the total heat capacity. Due to the close proximity of the substrate, conduction through air ensures that heat supplied to the device is quickly lost. The thermal heat capacity of the device is small, due to the small mass of the device. The knowledge of the thermal time constant is important in the design of a temperature controller. The thermal time constant of the device can be estimated using a thermal equivalent circuit, similar to that used in Section 3.2.1. The thermal equivalent circuit for the device is shown in Figure 5.15. A simplified one-dimensional model is used for the plate and each of the beams. The Norton equivalent circuit for the thermal circuit in Figure 5.15b is represented by a conductance, G_{eff} and heat capacity, C_{eff}. The G_{eff} is the sum of two conductances: G_{effair}, determined by heat conduction through air in to the substrate, and G_{effstr}, determined by heat conduction through the structure to the substrate. The solution of the electro-thermal circuit for a small voltage step input, is similar to (5.4), and is expressed as

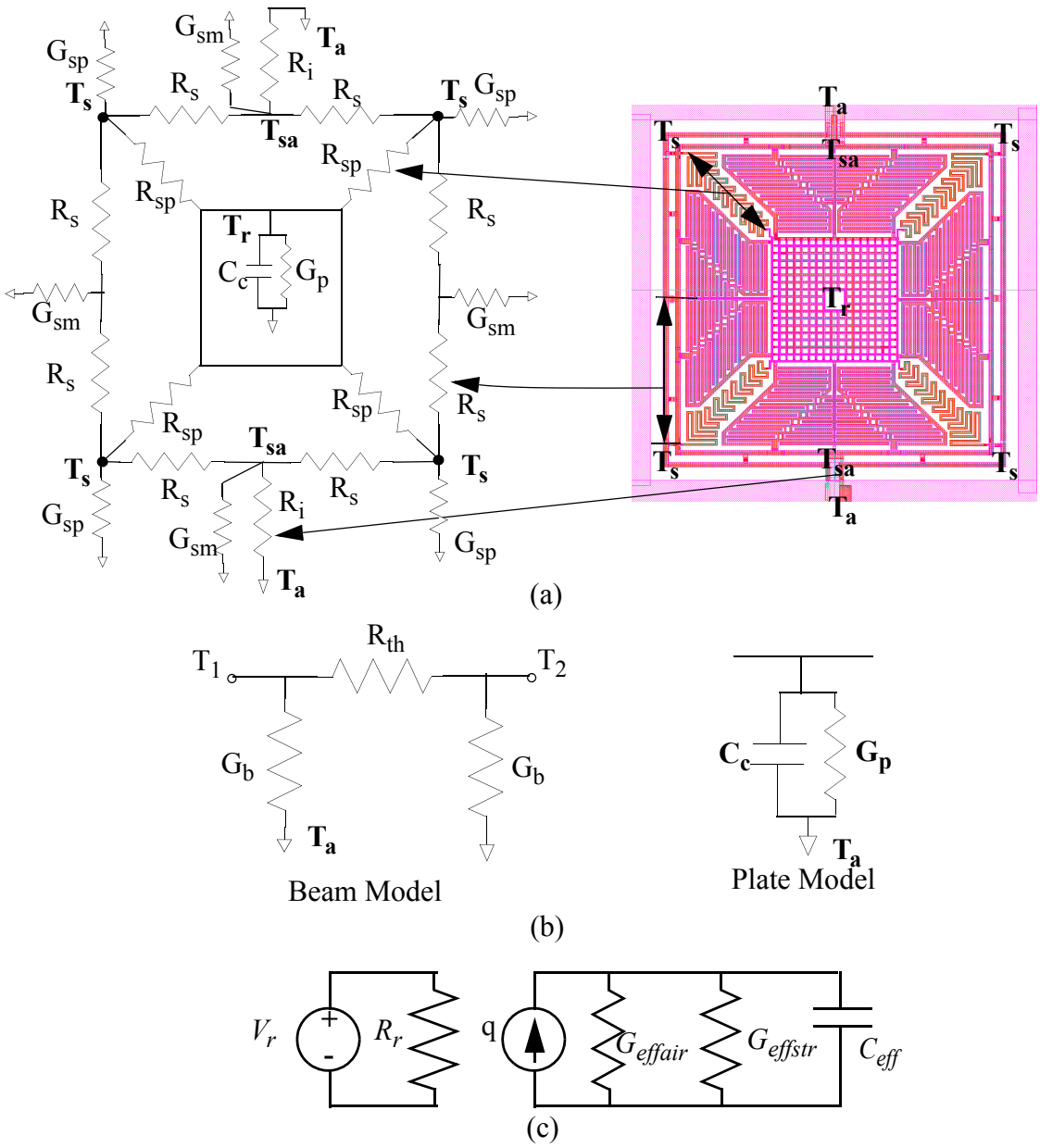


Figure 5.15 (a) Thermal equivalent circuit of the z-axis accelerometer, (b) Simplified beam and plate mass model. (c) The thermal Norton equivalent circuit, as seen by the rotor heater.

$$T_p = T_s + \frac{V_h^2}{G_{eff}R_r\left(1+\frac{\alpha_p V_r^2}{G_{eff}R_r}\right)}\left(1 - e^{-\frac{G_{eff}}{C_{eff}}\left(1+\frac{\alpha_p V_r^2}{G_{eff}R_r}\right)t}\right), \tag{5.36}$$

$$G_{eff} = G_{effstr} + G_{effair} \tag{5.37}$$

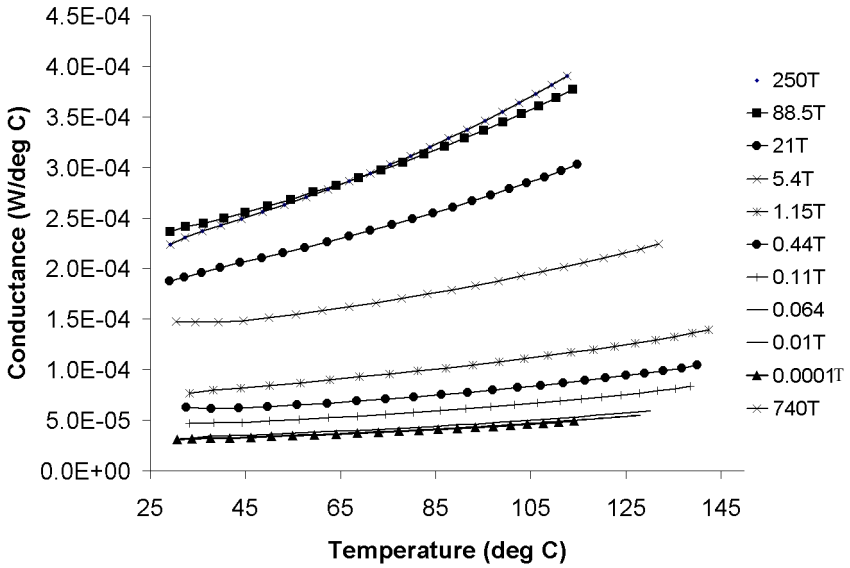


Figure 5.16 Variation of the device conductance as seen from the rotor heater, with rotor temperature and the pressure. In high vacuum the conductance is determined entirely by the heat loss through the thermal isolation.

where, R_r is the resistance of the rotor heater at ambient temperature, and V_r is the voltage applied to the heater. The thermal conductance, G_{eff}, is obtained by considering the steady state solution of (5.3), and evaluating

$$G_{eff} = \frac{V_r^2}{(T_p - T_s)R_{rf}} \tag{5.38}$$

where R_{rf} is the steady-state resistance of the heater after V_r is applied. This method was found to be accurate for temperature differences, T_p - T_s, greater that 4 ^{o}C, and significant error can occur for smaller values of T_p - T_s. To isolate the contribution from air conduction, measurements were made in different levels of vacuum. Devices that operate on this principle have been used by other researchers as vacuum sensors [74]. The plot of the thermal conductance of the device with different rotor temperatures and vacuum levels ranging from 740 Torr to about 10 mTorr is shown in Figure 5.16. The thermal conduction component due to heat conduction from the structure to the substrate is G_{effstr}=3.11x10^{-5} W/K, and due to air conductance is G_{effair}=2.05x10^{-4} W/K. Heat loss in the device is dominated by air conductance. The thermal conductance increases with temperature of the rotor, due to the increase in conductivity of air between the device and the substrate, and between the stator and the rotor comb fingers.

To determine the thermal time constant of the heater, two techniques were used. The first technique is based on (5.36). The step response of the temperature change in the rotor is measured by monitoring the resistance change of the heater. The resistance change is monitored using an active Wheatstone bridge circuit [91], the measured voltage is proportional to the temperature change. The time constant measured by this technique is a dependent upon the heater voltage, and is given by

$$\tau = \frac{C_{eff}}{G_{eff}\left(1 + \frac{\alpha_p V_r^2}{G_{eff} R_r}\right)} \tag{5.39}$$

The measured rotor heater time constant was 2.12 ms, for a heater voltage of = 2 V. This compares well with a time constant of 2.81 ms calculated based on analysis of the thermal circuit in Figure 5.15. The measured etch depth of 6 μm, was obtained using white light interferometry. The measured time constant is lower than calculated, as the thermal losses from the rotor comb fingers to the stator combs have not been taken into account in the analysis. The thermal time constant for the stator heater was measured as 1.9 ms and that for the rotor comb heater was 2.3 ms. The value of effective heat capacity of the rotor heater is obtained from (5.39) as C_{eff}= 5.5 x 10^{-7} J/K. Alternatively, the thermal time constant can be obtained by measuring the frequency response of the thermal heating signal. The details of the technique are described in reference [92][93]. The mechanical frequency response due to thermal heating can be obtained by measuring the proof-mass displacement optically at different frequencies using a MIT microvision system [27]. The displacements due to temperature were also be measured by the on-chip capacitance sense circuits. All three methods were investigated and they provide consistent results.

5.3.3 Temperature Control Circuits

Temperature changes in the device due to variations in ambient temperature are slow, on the order of minutes, mainly due to the large heat capacity of the package. The time constant of the temperature controller can easily be designed to be much faster than the overall package thermal time constant. The average temperature across the polysilicon heater can be kept constant by keeping the resistance constant. Several constant resistance circuits are proposed in the literature and are detailed in [17]. The time constant of the control circuit shown in Figure 5.17 can easily

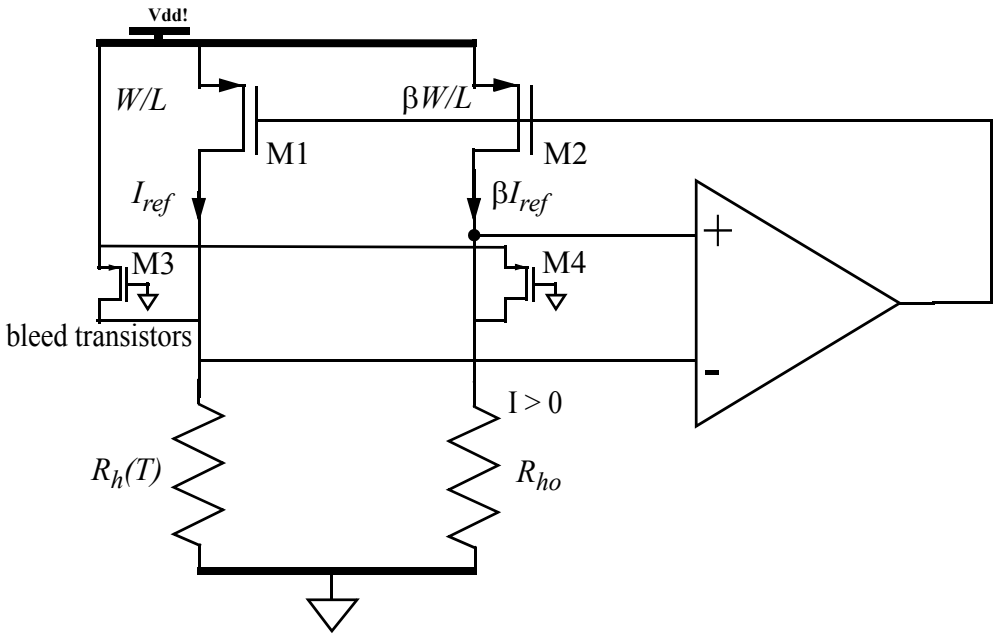


Figure 5.17 Schematic of a temperature control circuit, based on a constant resistance circuit

be made much smaller than the thermal time constant of the integrated heaters. $R_h(T)$ is temperature dependent polysilicon heater resistance. R_{ho} is a reference resistor with zero temperature coefficient of resistance, β is the ratio of the width of the transistor driving the reference resistor to the width of the transistor driving the heater resistor. The circuit controls the level of current to such that

$$I_{ref}R_h(T) = \beta I_{ref}R_{ho} \tag{5.40}$$

$$R_h(T) = \beta R_{ho} \tag{5.41}$$

If the value of the heater resistance is equal to R_{ho} at temperature T_o, The temperature of the polysilicon heater, from (5.1) is then

$$T = T_o + \frac{\beta - 1}{\alpha_p} \tag{5.42}$$

Equation (5.40) has an additional stable point, when the current in both branches is zero. This situation is reached when the drive to the current source transistors is reduced to zero, either at start-up or during operation. The current in both branches will become zero, when the ambient temperature exceeds the set temperature. To avoid this situation, additional bleed transistors, M3 and M4 are added to each branch to ensure that $I_h > 0$. If the ambient temperature becomes higher than the set temperature, the output of the opamp reaches the positive rail and the current sources

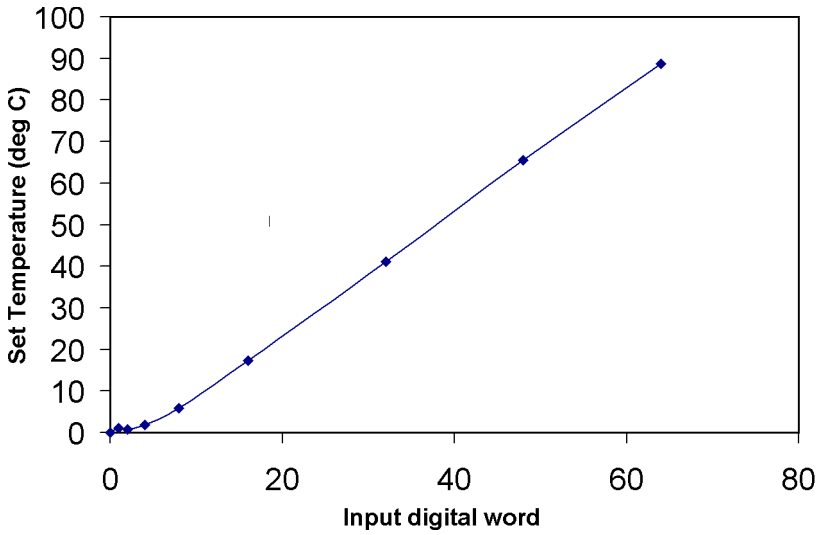


Figure 5.18 The measured variation of the average rotor control temperature with input digital word input to the DAC implementing M2.

shutoff. The bleeder transistors ensure that a small current flows through the heaters, so that the current sources can be turned on when the ambient temperature reduces and heating is required.

The heater in temperature increases is determined with β, as is evident from (5.41). β is changed digitally using a set of binary weighted transistors. A commercial digital to analog converter (DAC-08) integrated circuit (IC) includes an opamp and the digitally controlled binary weighted current sources, for the implementation of the temperature control. The details of the circuit implementation are included in Appendix II. Temperature control of the rotor polysilicon for different values of input digital word to M2 is shown in Figure 5.18. The characteristic has a small non-linearity due to the small bleeding current required to avoid the zero. The resolution of the controller is 1.4 ^{o}C per bit, which is sufficient for most control schemes.

5.4 Investigation of Temperature Control Schemes

The effect of temperature control to reduce the dependence of device characteristics on ambient temperature variations was demonstrated for various control conditions. Measurement were made by controlling each of the polysilicon heaters in the rotor-plate, rotor-comb and the stator, and the simultaneous control using all the heaters. In all cases identical heater voltages are maintained across the main device as the reference device. The accelerometer was packaged in a 40 pin DIP, and placed on the custom printed circuit board described in Section 4.4. The chip was heated by a strip heater taped to the back of the DIP to simulate ambient temperature change. The rotor, stator, and the rotor comb heater temperatures, for the main device and the dummy were set

by off-chip electronics. The complete board was mounted on the acceleration test shaker table, as described in Section 4.4.1. The sensitivity and the D.C. output voltage was measured at different chip temperatures under various temperature control schemes. Initial temperature control measurements were made using the circuit described in Section 5.3.3. However, to fully investigate all possible temperature conditions of the three heaters, a digital temperature control scheme, that allowed the heater temperatures to be controlled to within 0.3 ^{o}C, was implemented. The digital controller implemented using Labview [94] allowed completely automatic measurements over long periods of time. The temperature coefficient of resistance of each heater was measured during each measurement. Measurements were made on eight chips, with each measurement lasting about 40 hours. The heater voltage, current, chip temperature, ambient temperature were recorded for each control experiment. The heater voltage was set by a binary search algorithm that applied a voltage across the heater to maintain a constant resistance. If more than one heater temperature had to be set, the binary search iterates through all heaters till the set temperature is attained in each heater is obtained. The temperature coefficient of resistance ranged from 4.8 x 10^{-3} /K to 5.5 x 10^{-3}, with a nominal value of 5.23 x 10^{-3} /K for the resistors measured. The accurate determination of TCR is important for multi-heater control, as errors in the control temperature lead to temperature gradients between areas heated by different heaters. Temperature gradients are a function of the ambient temperature and can degrade the overall temperature coefficient of the accelerometer.

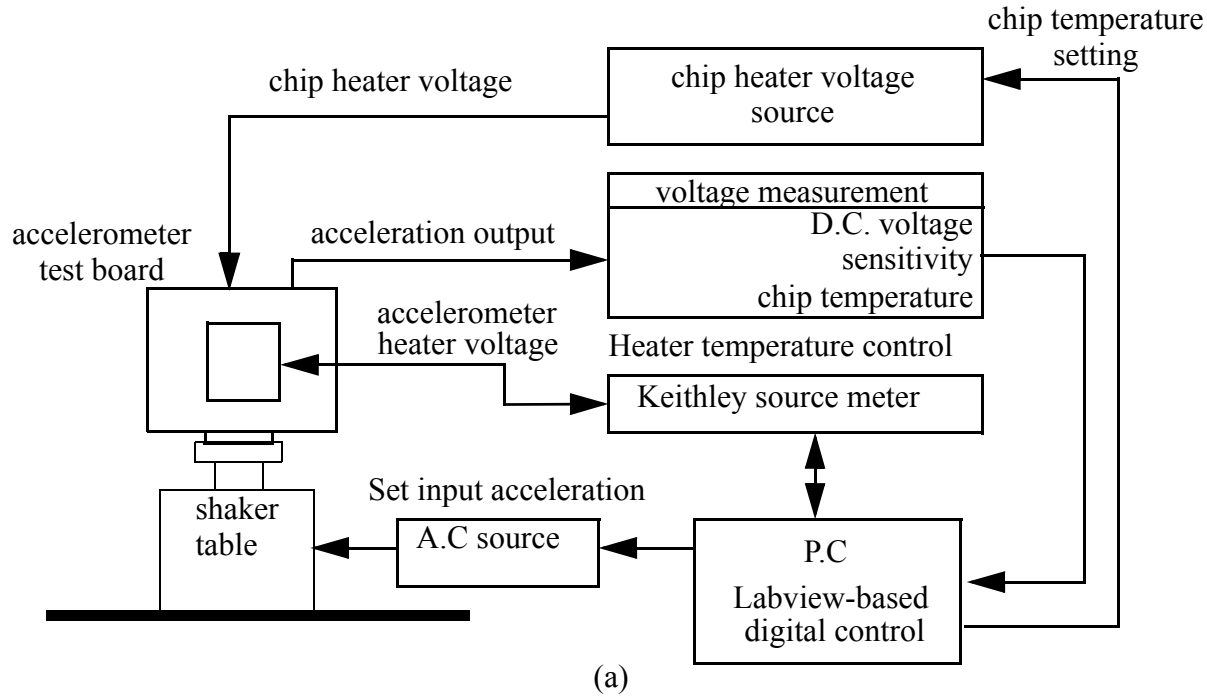
The chip temperature is measured by an on-chip temperature circuit that is based on the junction temperature of the diode. The temperature characteristic of the circuit was calibrated in a temperature controlled oven using a thermocouple attached to the DIP package. The schematic and the photograph of the measurement setup is shown in Figure 5.19. The personal computer (PC) control was implemented using Labview 5.1 by National Instruments [94] to control instruments linked by a GPIB bus.

The maximum safe temperature for heating is about 200 ^{o}C. Beyond this temperature the aluminum surface begins to appear grainy, and leads to device failure. The heater temperature was limited to about 160 ^{o}C, for best repeatability. To test the thermal reliability of thermal actuators measurements were made of simple thermally actuated beams described in [24], for a period of over 3 weeks, at a frequency of 6 kHz, with 10mW of heating power. The beam deflection per 100^{o}C decreased by 6%. Further measurements on thermal actuators have been reported by Xie et

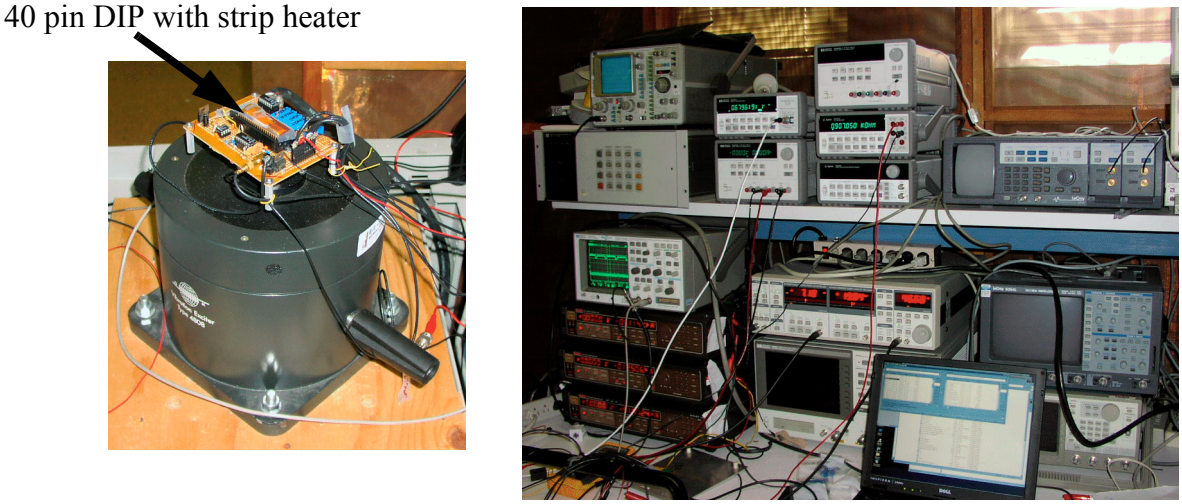
al. in [95]. A thermally actuated micro-mirror has been running in the MEMS lab display cabinet for almost a year without failure.

5.4.1 Rotor-plate Heater Control

The voltage output from the accelerometer test board, was measured with an acceleration input of 0.35 G (RMS) at 330 Hz. The rotor-plate heater was maintained at a constant temperature of 110 ^{o}C, the temperature of the accelerometer chip was varied from room temperature (30 ^{o}C)



(a)

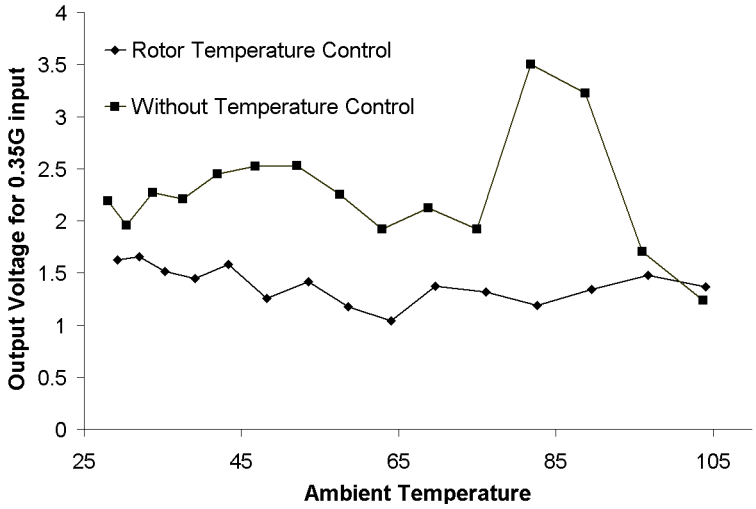


(b) (c)

Figure 5.19 Schematic of the setup for test of the temperature control scheme for the z-axis accelerometer. (b) The accelerometer packaged in a 40-pin DIP, with a strip heater and mounted on a shaker table. (c) Picture of the entire test setup.

to 104 ^{o}C. The A.C. RMS acceleration measured by the accelerometer is shown in Figure 5.20(a), and the D.C offset voltage variation with the ambient temperature is shown in Figure 5.20(b). When the rotor temperature is controlled, the stator-frame of the device is also heated, due to the heat loss through the connecting springs and air conduction from the rotor comb fingers. The average temperature of the stator is 53 ^{o}C, for an ambient temperature of 30 ^{o}C. This indicates that the heat conducted into the stator leaks away into the substrate. As the ambient temperature increases, the rotor heat loss reduces, changing the temperature distribution across the device. The changes in temperature distribution causes the dependence of the output voltage on the ambient temperature.

(a)



(b)

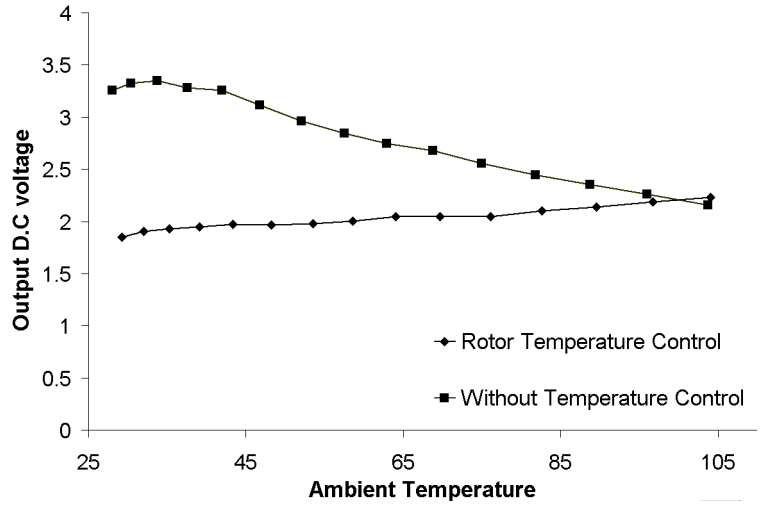
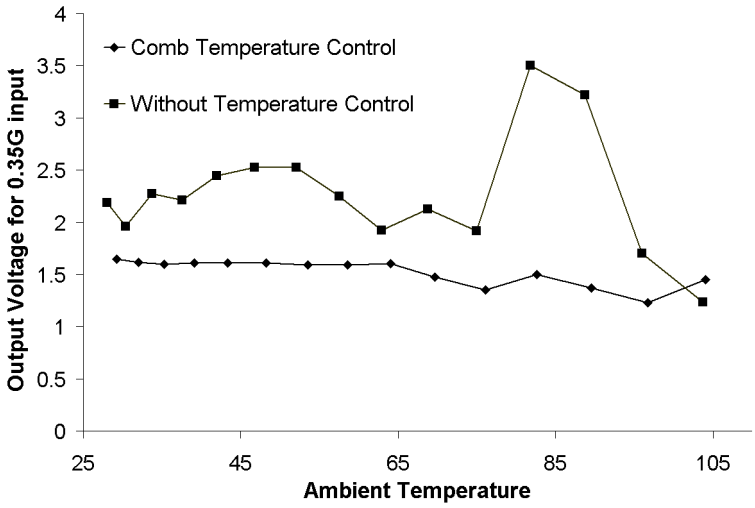


Figure 5.20 (a) Measured RMS voltage for a 0.35 G acceleration input at 330Hz, and (b) the output D.C voltage corresponding to a zero-G case, when the rotor heater is kept at 110 ^{o}C

5.4.2 Rotor-comb temperature control

A temperature control experiment with the only the rotor-comb heater maintained at 110 ^{o}C was performed using the same condition as in the rotor-plate temperature experiment. In this case, the heat is lost from the rotor comb fingers to the stator, due to air conduction. This results in temperature gradients and consequently degrades the temperature stability of this scheme. The A.C. RMS acceleration measured by the accelerometer is shown in Figure 5.21(a), and the D.C offset voltage variation with the ambient temperature is shown in Figure 5.21(b). The measure characteristic is very similar to that of the rotor-plate heater control, due to the close proximity of the heaters.

(a)



(b)

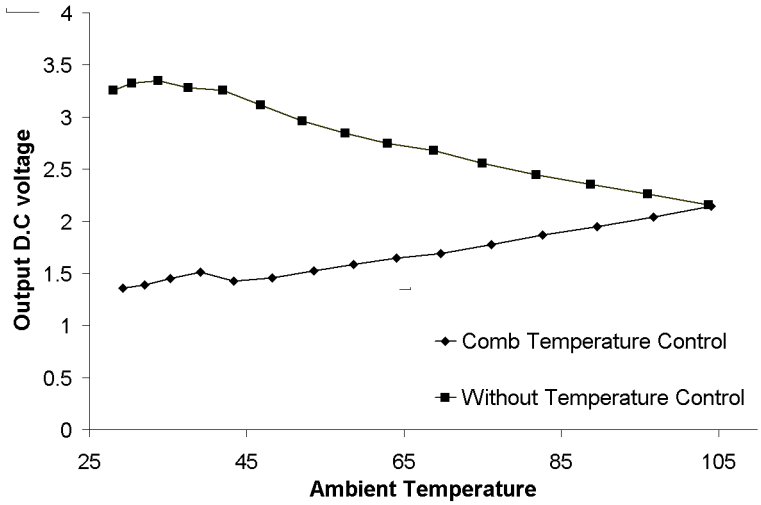
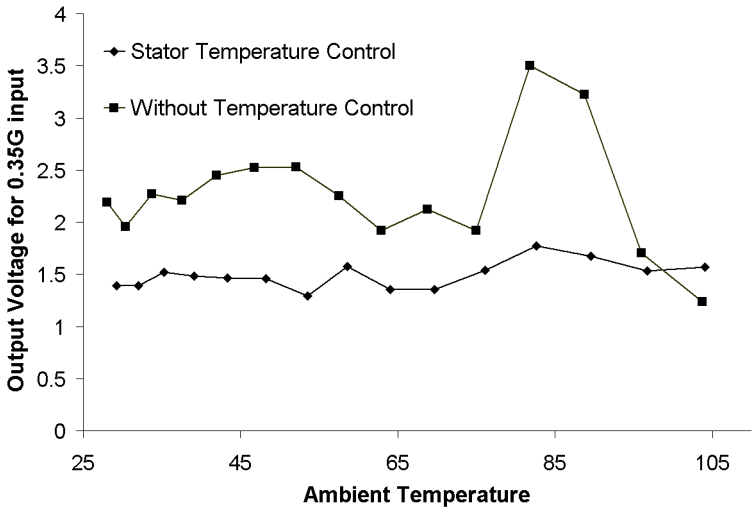


Figure 5.21 (a) Measured RMS voltage for a 0.35 G acceleration input at 330 Hz, and (b) the output D.C voltage corresponding to a zero-G case, when the rotor comb heater controlled at 110 ^{o}C

5.4.3 Stator heater temperature control

The stator heater, embedded in the outer stator of the accelerometer, was controlled at 110 ^{o}C, with the ambient temperature ranging from 30 ^{o}C to 104 ^{o}C. The heating of the outer frame causes the temperature of the rotor to rise due to heat conduction through the spring and the air gap between the rotor and the stator. This causes significant heating in the rotor is significantly, an average rotor temperature of almost 78 ^{o}C was measured at ambient temperature of 30 ^{o}C. At higher ambient temperatures the reduced heat losses to the substrate due to air conduction, increases the rotor temperature. The temperature gradient between the rotor and the stator is reduced with increasing temperature. Consequently, better performance is obtained with stator

(a)



(b)

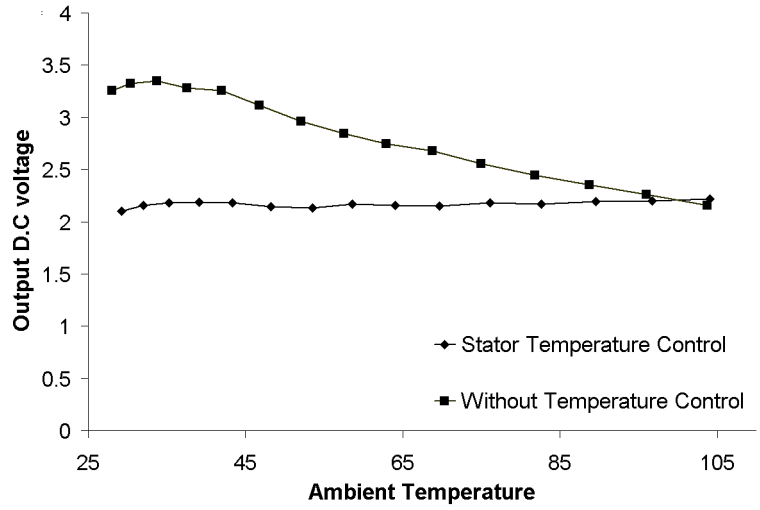


Figure 5.22 (a) Measured RMS voltage for a 0.35 G acceleration input at 330 Hz, and (b) the output D.C voltage corresponding to a zero-G case, when the stator heater controlled at 110 ^{o}C

heater control, than both the earlier cases. The A.C. RMS acceleration measured by the accelerometer is shown in Figure 5.22(a), and the D.C offset voltage variation with the ambient temperature is shown in Figure 5.22(b).

5.4.4 Temperature control using rotor-comb, rotor-comb and stator heaters

It is seen from the stator heater control experiment at 110 ^{o}C that the rotor heating is significant and that the temperature control is not satisfactory at lower ambient temperatures due to temperature gradients. The use of all the heaters within the device ensures that a uniform temperature distribution is generated across the rotor. Ideally the best performance would be expected when the rotor-plate, stator and the rotor-comb heaters are controlled to be at the same

(a)

(b)

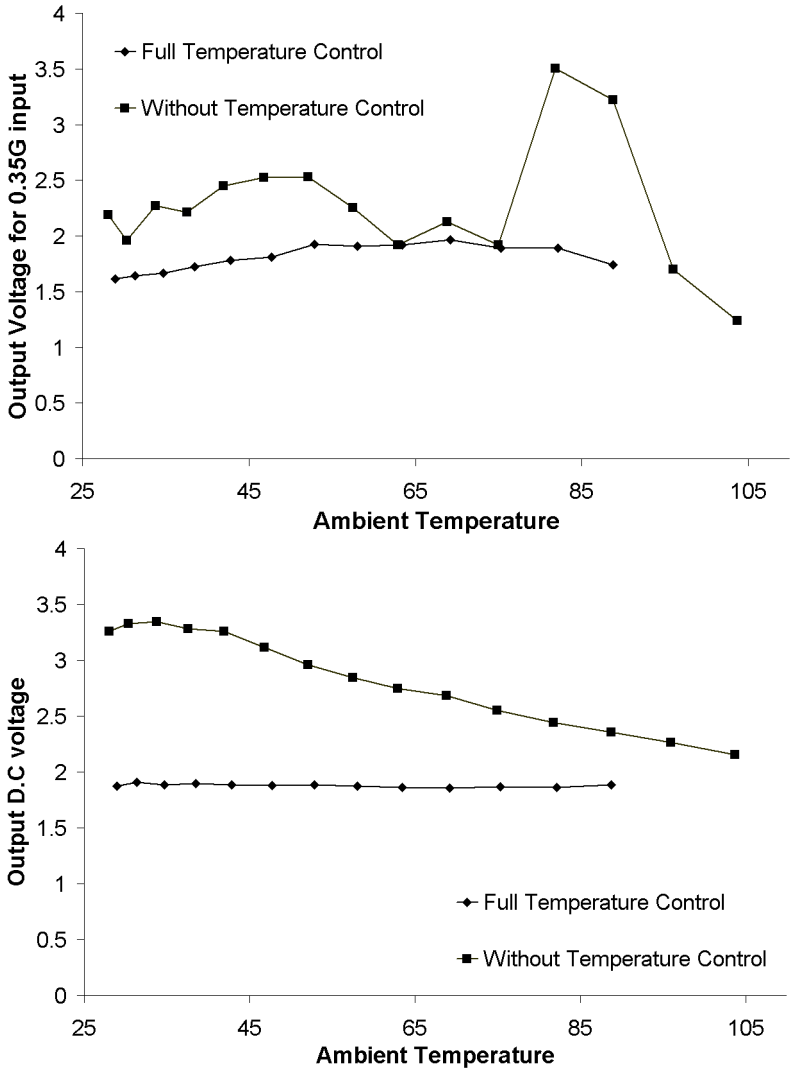


Figure 5.23 (a) Measured RMS voltage for a 0.35 G acceleration input at 330 Hz, and (b) the output D.C voltage corresponding to a zero-G case. The stator is controlled to 130 ^{o}C, and the rotor is controlled at 90 ^{o}C

Table 5.1: Summary of stator heater control performance

Parameter	Rotor-plate heater control only	Comb heater control only	Stator heater control only	All heater control
Nominal heater resistance	899 Ω	942 Ω	1470 Ω	n/a
Zero-G voltage temperature coefficient	4.29 mV/^{o}C	10.1 mV/^{o}C	711 μV/^{o}C	-416μ V/^{o}C
Percentage Sensitivity (30^{o}C-104^{o}C)	37.9 %	25.4 %	34.5 %	17.9 %
Heater input power @ T = 30^{o}C	29.4 mW	64.7 mW	80.7 mW	97.5 mW
Heater input power @ T = 104^{o}C	0.62 mW	3.7 mW	2.3 mW	41.3 mW

temperature. However, that was not found to be true. When all the heaters were kept at a constant temperature, a negative coefficient of temperature was seen for D.C. bias drift. This result can be explained by recognizing that the temperature controller can only set the average temperature of the heater resistor. It is observed from simulations and thermal imaging that the actual distribution is very different. The least temperature gradients are obtained for some combination of the heater temperatures. Measurements were made with different combinations of average temperatures of the stator and the rotor temperatures, with the rotor-comb heater set at the same temperature as the rotor-plate heater. The best performance was measured for a stator temperature of 130 ^{o}C, and a rotor temperature of 90 ^{o}C. The A.C. RMS acceleration measured by the accelerometer is shown in Figure 5.23(a), and the D.C offset voltage variation with the ambient temperature is shown in Figure 5.23(b). The performance is very similar to that obtained with stator heating only, except some improvements are seen at lower ambient temperatures. The D.C. bias or zero-G stability of the accelerometer improved from 1.9 G/^{o}C, to -42 mG/^{o}C, and the sensitivity stability improved from 60% to 18% over a temperature of 70 ^{o}C after temperature control.

5.4.5 Discussion on Temperature Stability Performance

A summary of the performance of the temperature control schemes is shown in Table 5.1. The nominal heater resistance was measured at an ambient temperature of 30 ^{o}C. The zero-G voltage temperature coefficient is the change in D.C bias output voltage per degree change in ambient temperature. The percentage sensitivity change is ratio of the maximum change in acceleration sensitivity of the accelerometer, over the range of ambient temperature, to the nominal sensitivity.

The performance of the temperature control scheme was limited by the ability to achieve a uniform temperature distribution across the device. The optimizations discussed in this chapter help to improve the temperature distribution across the device, but do not completely eliminated the effect of the temperature gradients. A non-uniform temperature gradients results in the device temperature distribution that is a function of ambient temperature.

It is also important to determine accurately the temperature coefficient of resistance of each of the heaters. An error in the measurement of the TCR results in different "set" temperature in the different heaters (rotor, rotor-comb and stator) leads to different temperatures being set in the device. This non uniform temperature setting leads to temperature gradients that degrade the temperature performance of the device

5.5 Conclusions

A temperature control scheme utilizing the polysilicon layer of the CMOS process improves the temperature performance of CMOS micromachined z-axis accelerometer. The best performance is obtained when the temperature of all the elements of the accelerometer are controlled. The methodology developed can be applied to any CMOS sensor to improve temperature stability and optimize the device curling.

Chapter 6. Modeling of CMOS Micromachined Inductors

6.1 Introduction

Advances in silicon technology, with decreasing feature sizes and application of novel materials, are pushing circuit performance to higher frequencies. State-of-the-art submicron gate CMOS with high f_t transistors is very attractive for RF design for mass-produced wireless communication products[96]. Interconnect resistance traditionally has not received attention in digital CMOS processes, but as modern digital designs have begun to be limited by interconnect delays, interest has been increasing[97]. Copper interconnect has been introduced to lower the interconnect resistance to reduce interconnect delay. This is an advantageous trend for RF circuit designers as better quality on-chip passives [98] can be designed with lower series resistance. High Q inductors can lead to improved power or figure of merit in low noise amplifiers (LNA), lower insertion loss in band pass filters and better phase noise and power in voltage controlled oscillators (VCO) [99].

Inductors are intended to store magnetic energy. However, the finite coil resistance and the substrate losses in silicon contribute to energy losses. Energy losses in the silicon substrate result from I^2R losses due to the currents flowing through the metal to substrate capacitance and to those currents generated due to magnetic fields induced by the inductor. These losses can be eliminated by either providing zero substrate resistance or making it very large.

Solid ground shields that help to reduce the substrate resistance induce opposite flowing loop currents due to Lenz's law. These currents produce a negative mutual coupling that reduces the magnetic field and decreases the overall inductance. One approach suggested by Yue and Wong [100] is the use of patterned ground shields that reduce the induced loop current by insertion of slots in the shield. The main drawback of this technique is that the parasitic capacitance to substrate is significantly increased. Pattern ground shields are effective for lower frequency applications where the parasitic capacitance can be absorbed in the LC tank. Increasing the

substrate resistance is another useful approach for eliminating substrate losses. The use of high resistivity silicon [101] and sapphire substrates has been used by researchers to demonstrate high Q planar inductors, achieving quality factors of 40 at 5.8 GHz for an 1.4nH inductor [102]. However, the use of high resistivity material is not common in a digital logic CMOS process and many submicron CMOS technologies use epitaxial silicon wafers. Substrate removal is a method of choice for large area inductors in which improvement in self resonant frequency extends the usable frequency range. Chang et al. [103] proposed elimination of substrate losses in large area inductors by removing the underlying silicon using front side etching of silicon in a post CMOS processing step. Silicon has been removed by wet etching or by using gaseous dry etching [104]. These techniques have inherent limitations as to how far circuits can be placed from the inductor, introducing I^2R losses in the interconnect resistance. The distance of the transistors from the inductor is determined by the dimensions of the inductor and the time of the etch. Other approaches to eliminate silicon from below the inductor have used back-side etching techniques [105]. Research has also aimed to integrate micromachined inductors using custom fabrication techniques on the bottom of the CMOS chip[106] and on GaAs substrates [107].

In this chapter, an approach is presented to improve the performance of inductors fabricated in a digital logic process with copper interconnect and low-k dielectric by use of maskless post-processing steps [108]. Removal of the underlying silicon and the inter-turn sidewall oxide helps reduce the substrate losses that dominate at higher frequencies, increase the self resonant frequency and also reduce substrate noise coupling into the inductor. This technique leverages the ever increasing number of interconnect layers used in modern processes for passive designs [109] for lower series resistance without severe high frequency performance penalties. Section 6.2 describes the processing steps and its impact on circuit design and layout. The mechanical stability of a suspended inductor to external shock and temperature changes has been investigated using finite element modeling. Section 6.3 describes a physical model of the inductors that was developed to understand the performance gains due to micromachining. Measurement results compare the performance of the micromachined inductor to conventional on-chip inductors, with and without the sidewall oxide. Section 6.4 presents a discussion of the results and Section 6.5 draws some conclusions based on this work.

6.2 Design Considerations

A 0.18 μm minimum feature size CMOS process with copper interconnect and low-K dielectrics was used to fabricate the inductors. [8][110] Circuits can be placed about 30 μm away from the edge of the silicon pit and this design rule is independent of the depth of the silicon pit. The circuits are protected by the top metal of the CMOS process. This is a disadvantage as top metal cannot be used for arbitrary interconnect and is grounded. The maximum width of a metal masked microstructure is about 30 μm. The smallest width is limited by the processing conditions to about 1.5 μm.

The electrical performance of the circuits is not affected by the etching steps. Inverter test structures were tested before and after the micromachining process. A 2.2 GHz single LC tank oscillator was tested to verify the operation of the transistors after the post process step. The oscillator used a 3 nH single suspended inductor. The circuit consumed 10.2 mA with a supply voltage of 1.7 V.

6.2.1 Inductor Structure

Scanning electron microscope image of a suspended inductor with a single sided mechanical connection is shown in Figure 6.1. The inductor coil is designed with four 20 μm-wide turns using metal 5 and metal 6 layers, which are the thickest (0.5μm) layers available in the process. The two layers are shunted together to reduce the series resistance of the coil. The return conductor consists of the metal 4,3,2,1 layers shunted together, with a total thickness of about 1 μm. Inductor geometries were optimized for maximum inductance, and lowest D.C resistance using FASTHENRY [111] with a parametric inductor layout and input deck generator.

6.2.2 Mechanical Stability of the Suspended Inductor

The variation of inductor performance with temperature has been studied by researchers [112] for conventional on-chip inductors. One concern in design of mechanical suspended inductors is that external shocks and mechanical deformations of the inductor structure from external shock or temperature change the inductance, hence affecting the circuit performance. Residual stress differences in various films used in the interconnect fabrication cause the inductors to curl out-of-plane, so that the highest point of the inductor is above the plane of the chip. This out-of-plane curl is a function of the dimensions of the inductor and temperature. Finite element simulations were carried out to verify the mechanical stability of the suspended inductors and curling due to residual stress and temperature. The details of the analysis are in

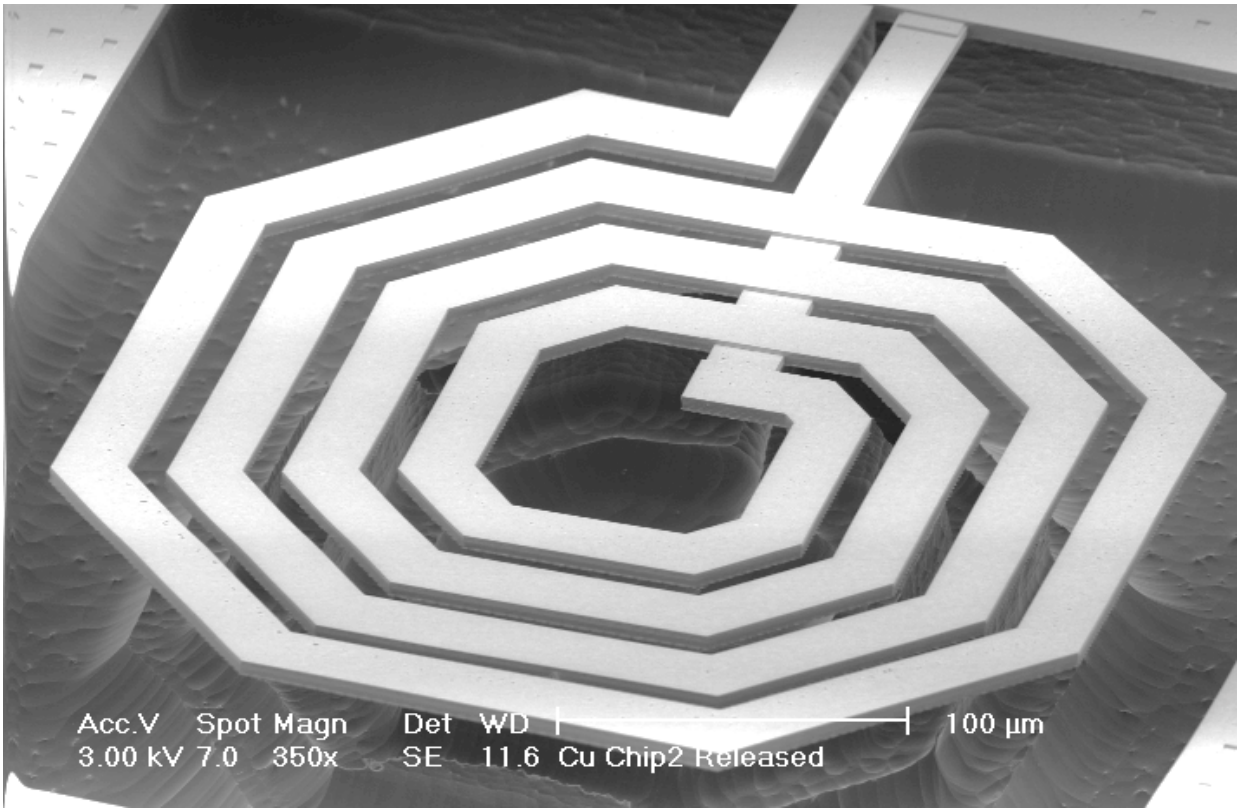


Figure 6.1 Scanning electron micrograph of a micromachined inductor anchored on one side.

Chapter 2. Two square (400 µm by 400 µm) inductors with single-sided and double-sided suspension and five turns were analyzed. Thermomechanical simulations [35] were followed by FASTHENRY simulations to compute the inductance after deformation. Table 6.1 summarizes the results of the mechanical simulation. External shock to the inductor was simulated by subjecting the inductor structure to a static 9810 m/s^2 (100G) of acceleration and calculating the inductance change. Motion due to external shock is very small (~ 0.5µm) due to the extremely small mass of the inductor, on the order of 1 µgram. The natural mechanical frequencies, which potentially can amplify the displacement from a shock, and can frequency modulate the center frequency of a VCO were simulated. The results of the finite element analysis for structural curl and mechanical modes is summarized in Figure 6.2. The first three mechanical vibration modes of the device are low frequency (8-23kHz). The effect of these modes can be compensated in the design of the Phase Lock Loop (PLL) by a large loop gain. The higher frequency mechanical modes are difficult to excite in a packaged inductor due to the mechanical damping of the package. These resonances can be moved to higher frequencies by increasing the number of

anchors. The suspended inductors have a low mechanical dependence on inductance with temperature change because the relative displacement between adjacent turns is very small compared to the dimensions of the structure. The relative displacement between the turns is smaller in a single-suspended cantilever inductor, compared to the double-suspended inductor, even though the former has larger overall curl. This results in a lower inductance reduction for the single-sided inductor after release.

6.3 Device Modeling and Characterization

To understand the improvement due to substrate and the sidewall oxide removal, an equivalent circuit model based on physical principles is proposed. The schematic of the model for a four-turn inductor is shown in Figure 6.3 and is an extension of models proposed earlier[113].

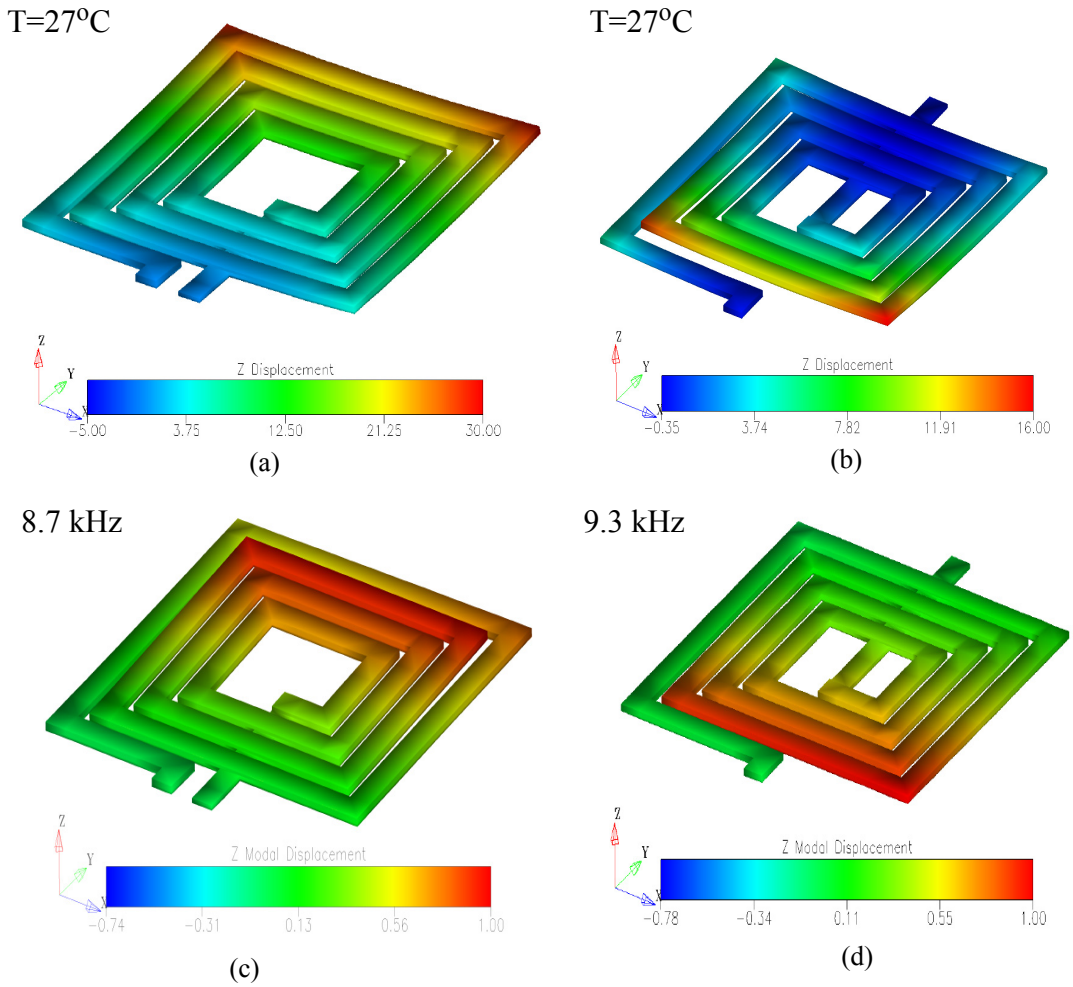


Figure 6.2 Inductor out-of-plane curl after oxide removal and silicon release. (a) Single suspended inductor, (b) Double-sided suspended inductor. The shape of the first mechanical mode for (c) Mechanical mode of single suspended inductor at 8.7 kHz, (d) Mechanical mode of double-sided suspended inductor at 9.3 kHz.

Table 6.1: Summary of mechanical effects in suspended inductors

Simulation result	Single anchored inductor	Double anchored inductor	
Nominal Inductance	4.824	4.918	nH
Inductor dimensions	400μm by 400μm	400μm by 400μm	μm^2
Maximum out of plane curl	25.10	15.94	μm
% Inductance change due to curl	-0.0070	-0.1036	%
1st Mechanical mode	8.71	9.31	kHz
2nd Mechanical mode	16.27	21.71	kHz
3rd Mechanical mode	22.07	22.22	kHz
Temperature coefficient of inductance	0.757	11.139	ppm/^oC
Inductance change due to 100G shock	-0.0162	-0.0173	%
Maximum deflection due to 100G shock	0.5011	0.4543	μm

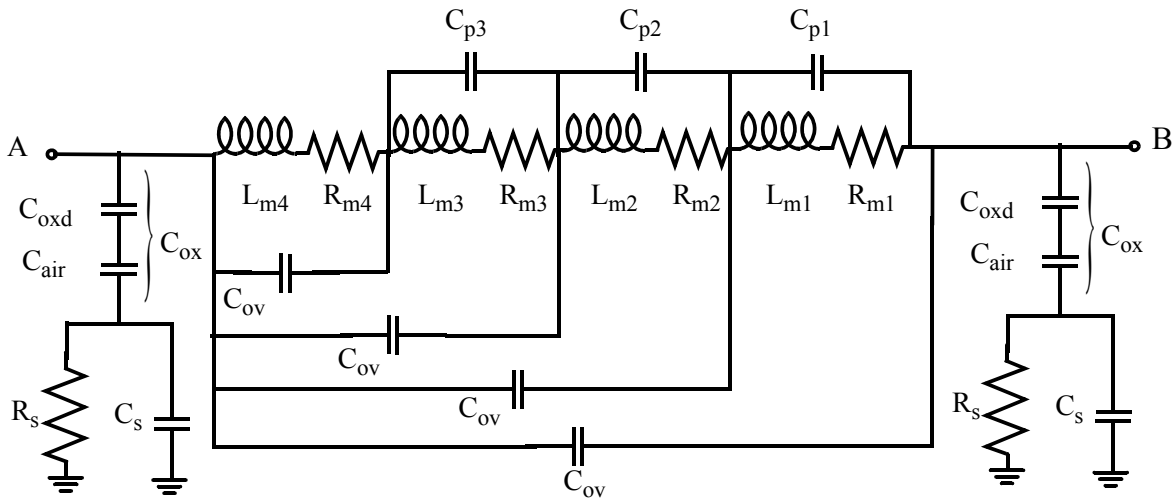


Figure 6.3 The lumped parameter equivalent circuit for the inductor, which for includes parasitic sidewall capacitance and substrate loss.

Each turn of the inductor has been modeled as a separate LCR segment to account for the contribution of inter-turn capacitances to the resonant frequency. Contribution of the inter-turn capacitance has been considered insignificant in the modeling of non-micromachined inductors.

6.3.1 Inductor Model

To accommodate the effects of inter-turn capacitance, the inductance (L_{mn}) and the series (R_{mn}) resistance due to each turn are modeled separately [114] and are expressed as

$$L_{mn} = L_m\left(\frac{l_n}{l_m}\right), \tag{6.1}$$

$$R_{mn}(f) = R_m(f)\left(\frac{l_n}{l_m}\right) \tag{6.2}$$

where, L_{mn} is the inductance of the nth turn of the inductor, L_m is the total inductance, l_m is the total length of conductors, l_n is the length of the n-th turn, and $R_m(f)$ is the series resistance of the inductor. The total inductance value was estimated from finite element simulations using FASTHENRY. A constant inductance per unit length was assumed for all the spirals.

D.C resistance is computed from the dimensions of the coil and conductivity of the interconnect material. However, at higher frequencies the series resistance of the inductor is dependent on frequency due to skin effects, and current crowding issues due to magnetic effects [115]. The situation is further complicated by the use of two parallel conductors electrically shunted together to form the inductor spiral. The application of an analytical expression derived in [113] and [116], has been used to model the series resistance. The series resistance of each segment is modeled as

$$R_m(f) = R_{dc}\left(\frac{l_n}{l_m}\right)\frac{\frac{t_c}{\delta}}{1-e^{-\frac{t_c}{\delta}}} = R_{dc}\left(\frac{l_n}{l_m}\right)\left(\frac{\sqrt{\frac{f}{f_c}}}{1-e^{-\sqrt{\frac{f}{f_c}}}}\right) \tag{6.3}$$

where f_c models the frequency at which skin effect begins to dominate in copper for the thickness of the conductor used in the design, t_c is the combined thickness of the copper conductor used in the spiral, and ρ is the resistivity of copper. The skin depth (δ) at any frequency [117], and the critical frequency f_c are given by

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}}, \tag{6.4}$$

$$f_c = \frac{\rho^2}{\pi^2\mu^2 t_c^2} \tag{6.5}$$

The expression in (6.5) indicates that the use of thicker metals in the spiral will reduce the frequency at which skin effects begin to dominate. Improvements in Q factor at higher frequencies reduce with increasing coil thickness.

The capacitance due to the cross-over of the return conductor under the coil is denoted by C_{pov}. This is computed as the parallel-plate capacitance between the spiral and the return conductor.

$$C_{pov} = \frac{\varepsilon_d w^2}{d_s} \tag{6.6}$$

where, ε_d is the permittivity of the low-K dielectric material, w is the width of the inductor turn and d_s is the dielectric thickness between the spiral and the return path.

The sidewall inter-turn capacitor has been neglected in the modeling of non-micromachined inductors. Since the potential difference between adjacent turns is small, that small capacitance is absorbed in the capacitance to the substrate. The inclusion of this term is important for understanding the effects of sidewall oxide removal on the performance of the micromachined inductors. The sidewall term consists of two parts, namely the parallel plate component (C_{p1n}) directly between the conductors and the fringing fields between the two conductors (C_{p2n}). The fringing field between the inductor turns is a function of the ratio of inductor turn width and the gap between the turns and can be expressed as [118]

$$C_{pn} = C_{p1n} + C_{p2n}$$

$$C_{pn} = \frac{\varepsilon_{gap}(l_{n+1} + l_n)}{2}\left(\frac{t}{P-w} + \frac{1}{2\pi}\ln\left(\left(\frac{w}{P-w}+1\right)^2 - 1\right)\left(1 + 2\left(\frac{P-w}{w}\right)\right)^{\left(1+\frac{w}{P-w}\right)}\right) \tag{6.7}$$

where, ε_{gap} is the electrical permittivity of the medium between the turns (air or dielectric), and P is the pitch of the spiral. The fringing capacitance due to the sidewalls can only be neglected for narrow conductors with large spacing between them. The fringe term expression assumes that the conductors are in a medium with the same dielectric constant. The micromachined inductors are surrounded by air, so this assumption is appropriate. The effect of the silicon under the coil has been neglected.

The substrate losses are modeled using the model proposed in [113] and [101]. The capacitance between the inductor and the substrate, C_{ox} is expressed as

$$\frac{1}{C_{ox}} = \frac{1}{C_{oxd}} + \frac{1}{C_{air}} = \frac{2d_{sub}}{\varepsilon_d w l_m} + \frac{2d_{etch}}{\varepsilon_o w l_m} \tag{6.8}$$

where, C_{oxd} is the capacitance between the bottom metal of the spiral and the silicon substrate, that is separated by a distance, d_{sub}, C_{air} is the capacitance between the bottom of the oxide to the etched silicon, and d_{etch} is the etch depth of the silicon pit. The value of d_{sub} for the inductors in this process is 3.2μm. The slight asymmetry between the two ports due to the presence of the return conductor has been neglected. The expression has been corrected for fringing using the expression in [119].

The dissipative mechanisms in the inductor include losses in the silicon substrate below the inductor and in the surrounding metal frame. Due to processing constraints, the top metal layer is used as a mask and it defines the etch pit around the inductor. A fill pattern is also introduced by the foundry to control metal density for more uniform thickness during the chemical mechanical polishing of the metal. The empty area in the inductor hollow and the area around the inductor and in the area below the unused inductor coil is an exception to the metal fill rule. The eddy currents produced in the silicon dominate the substrate losses in the non-micromachined inductor case. However, the effects from the surrounding metal frame dominate the losses in the micromachined inductor. A lumped R_s-C_s substrate model accounts for these dissipative mechanisms.

$$C_s = \frac{wl_m}{2} C_{sub} \quad \text{and} \tag{6.9}$$

$$R_s = \frac{2}{wl_m G_{sub}} \tag{6.10}$$

where, C_{sub} is the capacitance and G_{sub} is the conductance per unit area of the substrate. The values of G_{sub} and C_{sub} are extracted from measured results and are a function of the inductor geometry. The etch depth of the silicon directly below is a function of the metal mask. Small openings in the metal mask experience etch lag. d_{etch} is thus a function of the geometry and the layout. Considering these difficulties d_{etch} is fitted from experimental data.

This model accounts for the changes in inductor performance due to the post process. The effects of oxide removal can be explained by reduction of the C_{pn} term to increase the self resonant frequency of the inductor. The increase in d_{etch} due to silicon etch lowers the substrate capacitance C_{ox}, thus reducing substrate losses.

6.3.2 Definition of Quality Factor

Several definitions of Q have been used to define the quality factor of inductors in literature depending on their intended applications. [109][100][120] The quality factor defined for inductor used for on-chip planar inductor applications and in this paper is defined as

$$Q(f) = \frac{X_m(f)}{R_m(f)} \tag{6.11}$$

For application of the inductor in an LC tank circuit, the quality factor definition at the resonant frequency is important. The Q at resonance of an LC tank (Q_{LC}) is calculated by assuming that the capacitive contribution to the impedance is equal to the inductive contribution and is expressed as

$$Q_{LC} = \frac{f}{2R_m(f)} \frac{\mathrm{d}}{\mathrm{d}f}(X_m(f))\Big|_{f=f_{res}} \quad , \quad f_{res} = f|_{X_m = 0} \tag{6.12}$$

where, f is the frequency of the LC tank, $R_m(f)$ is the real part and $X_m(f)$ is the imaginary part of the inductor impedance. This expression is evaluated at the resonant frequency of the LC tank,

Table 6.2: Summary of inductor measurement data

Property	L1			L2			L3			L4		
	set A	set B	set C	set A	set B	set C	set A	set B	set C	set A	set B	set C
L_m (nH)	3.16	3.32	3.19	3.89	3.95	3.91	4.12	4.20	4.15	4.61	4.71	4.69
Q_{max} conv.	4.39	5.32	12.5	4.02	4.60	11.2	3.76	4.25	10.46	3.64	4.09	7.61
@ f (GHz)	1.75	2.25	7.75	1.45	1.85	6.50	1.35	1.75	5.72	1.25	1.75	4.75
R_{dc} (ohms)	3.45	3.27	3.32	4.26	4.39	4.16	4.70	4.89	4.65	5.28	5.52	5.21
Q_{max} LC	4.43	5.28	25.7	3.87	4.52	17.0	3.52	4.19	16.0	3.50	4.04	10.3
@ f (GHz)	2.05	2.65	13.7	2.15	2.25	8.62	1.55	2.15	7.65	1.45	2.15	6.80
f_{res} (GHz)	10.1	11.5	14.0	8.35	9.85	12.9	7.15	9.45	12.0	6.65	8.85	11.38
diameter(μm)	300			336			350			365		
width(μm)	20			20			20			20		
turns	4			4			4			4		
pitch (μm)	30			30			30			30		

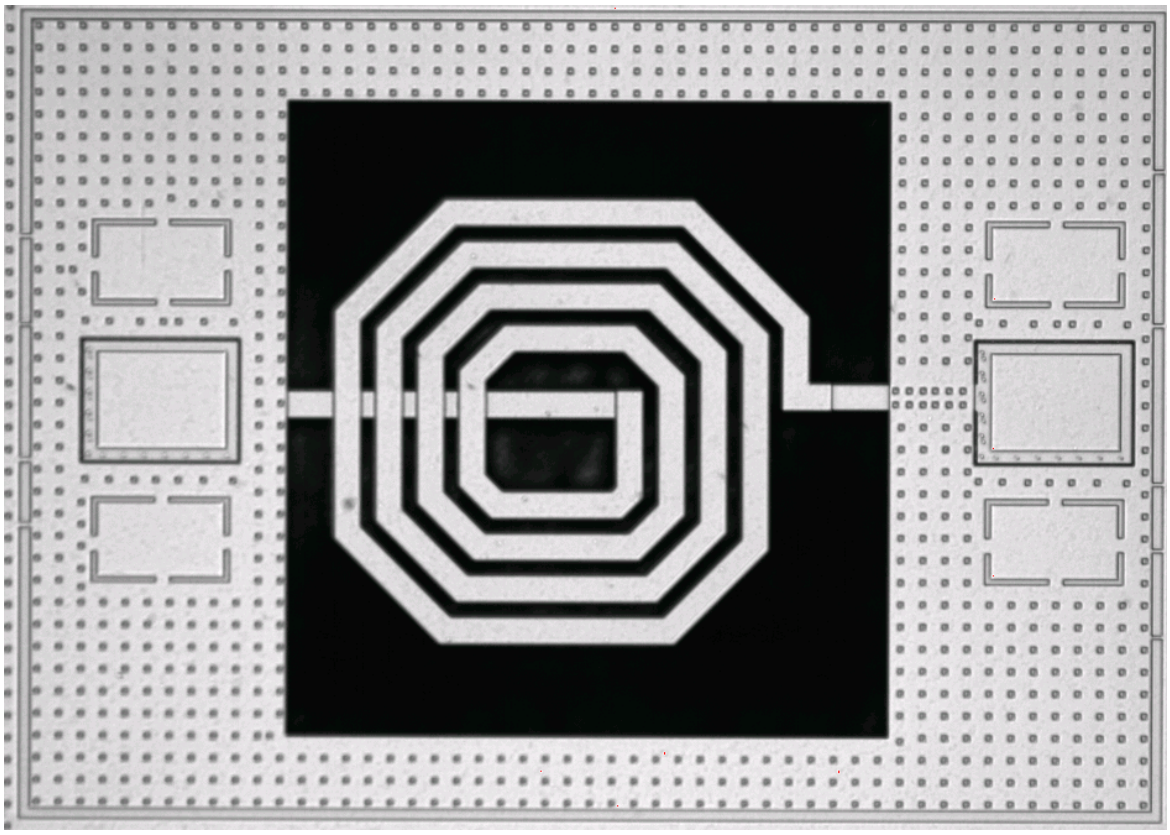


Figure 6.4 Microphotograph of a micromachined inductor test structure showing the mask metal layer surrounding the double side anchored inductor along with 2 port test pads. The dimensions of the cavity are 400μm by 450μm.

f_{res}, which is defined as the frequency at which the imaginary part of the impedance is zero. Niknejad et al. [120] proposed a Q calculation at any frequency by addition of a perfect capacitor to bring the resonance to that frequency. This definition of Q measurement leads to much higher values for micromachined inductors.

6.3.3 Experiment Design and Measurements

Four octagonal inductors with different sizes, L1-4, and values ranging from 3.0nH to 4.5nH, were designed. The metal mask around the inductor was 400 μm x 450 μm. Inductor, L1, along with the two-port probe pads is shown in Figure 6.4 The surrounding mask metal has been grounded and is tied to the substrate. To investigate the effect of the micromachining on the performance of the inductors, measurements were made on unprocessed inductors, after the first step of sidewall oxide removal and after the complete processing. All these chips were from the same wafer batch and were post-processed at the same time. This set of measurements quantifies the improvement due to micromachining, including oxide removal and silicon etching.

The inductors were measured by making two-port measurements by on-chip probing using 100 μm pitch ground-signal-ground (GSG) microwave probes connected to a HP8510C network analyzer with frequencies ranging from 50 MHz to 20 GHz. Probe calibration was done using a Cascade CS-5 calibration substrate. The probe pads were de-embedded by making measurements on dummy open and short test structures connected to test pad structures.

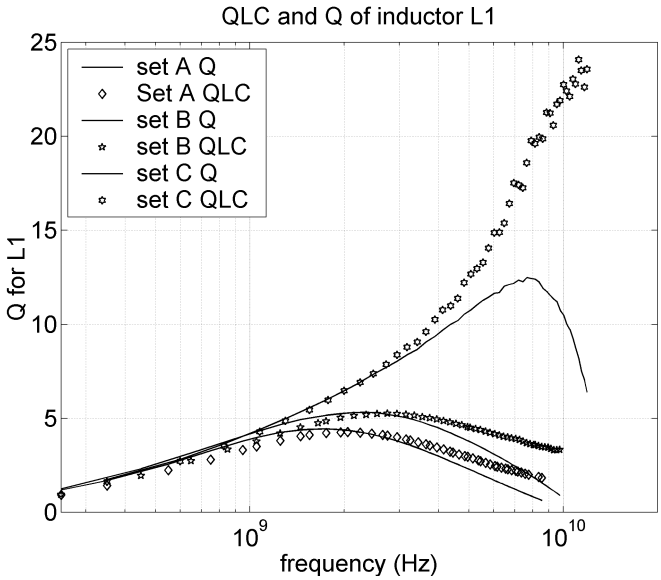
The performance of four inductors L1-4 was compared with measurements made on three chips. The three sets of measurements are:

1. Set A: Conventional inductors without micromachining obtained from the foundry.
2. Set B: Low-k sidewall oxide removed between turns.
3. Set C: Low-k sidewall oxide removed between turns and silicon undercut below turns.

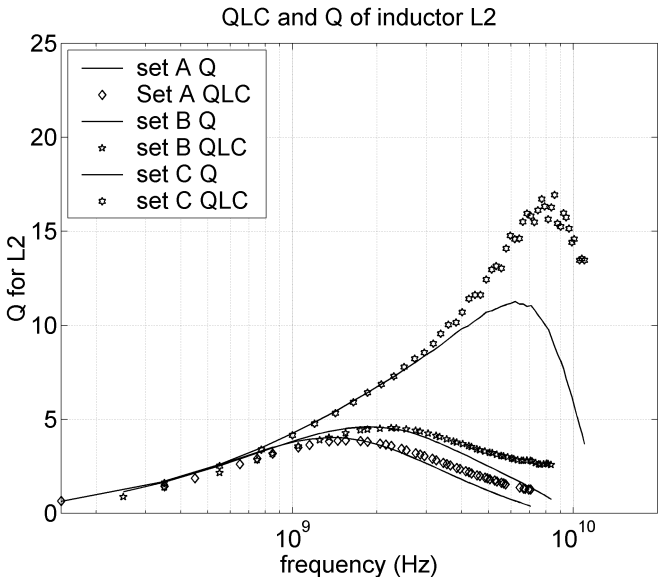
A comparison of the Q of the micromachined inductors calculated by the conventional method and by the LC tank definition is shown in Figure 6.5 and Figure 6.6. Table 6.2 summarizes the measurement results obtained from the inductors. All the values of Q were measured by grounding port 2. The self-resonant frequency after sidewall oxide removal in set B, increases by 14%-33%. The reduction of the sidewall oxide capacitance is larger for the bigger inductor, causing a greater increase in self-resonant frequency. A small increase in the maximum Q was also observed due to the increase in the self resonance frequency.

The silicon removal process step increases the maximum Q by about 100%-180%. A smaller increase is observed in L4, the biggest inductor, due to the smaller distance of the inductor from the surrounding mask and the fill metal. This suggests that the separation distance from the sidewall to the inductor should be made large enough to minimize eddy current losses in the mask metal. The self-resonance frequency increased by about 38% to 70% over set A, depending on the size of the inductor. The bigger inductors have a larger increase due to a greater reduction in capacitance to substrate (C_{ox}). The frequency at which maximum Q occurs is moved to the 5-8 GHz range (set C) from the 1-2 GHz range (set A), an increase of 280%-350%. Inductor L1 in set C achieves a maximum Q of 12.5 at 7.8 GHz, a 14-fold increase compared to set A. At 5.5 GHz a 5 fold improvement can be seen.

The measured quality factors are compared to the model, described previously, in Figure 6.7 and Figure 6.8. The differences from the modeled behavior in set A and set B result from a reduction in the sidewall capacitance and a slight increase in G_{sub} due to the over-etching of the



(a)



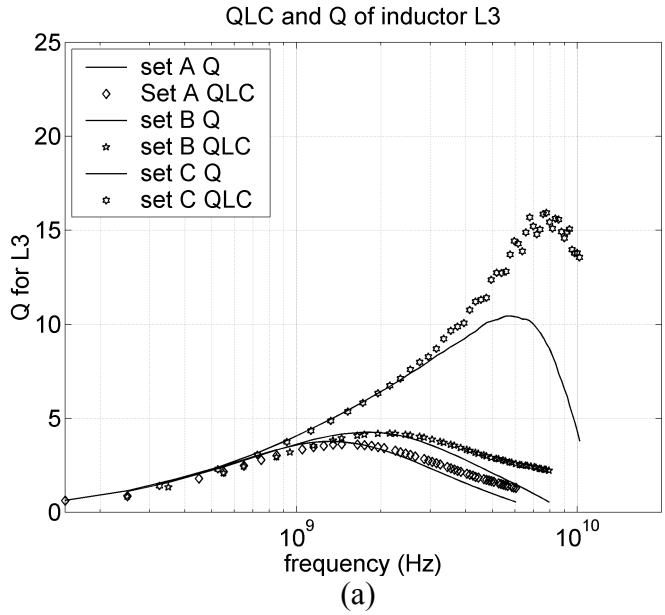
(b)

Figure 6.5 Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), Set C (micromachined) measured by conventional (Q) and LC tank definitions (QLC) of Q for inductors (a) L1, (b) L2

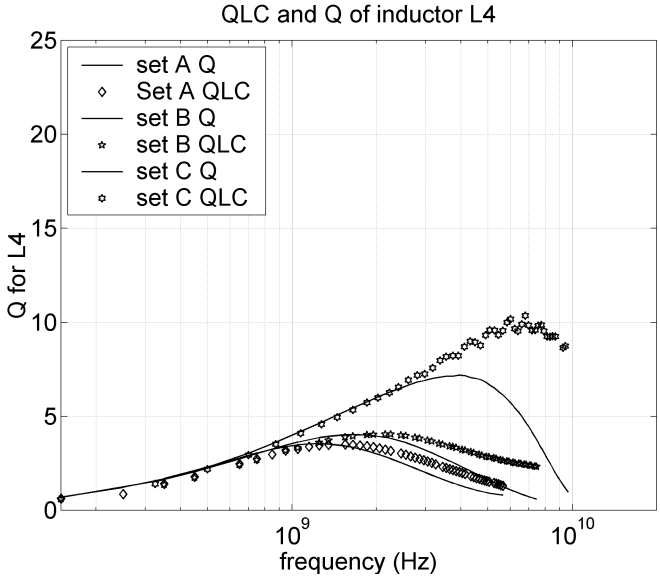
silicon during the etching of the oxide. The model for set C is accounted for by the increase in the effective etch depth (d_{etch}) and the increased substrate conductivity (G_{sub}).

6.4 Discussion

At lower frequencies, the quality factor of the inductors is not significantly improved by micromachining, as the series resistance losses dominate the energy loss mechanism. However, at higher frequencies, substrate losses begin to dominate and an improvement in Q is observed. The



(a)

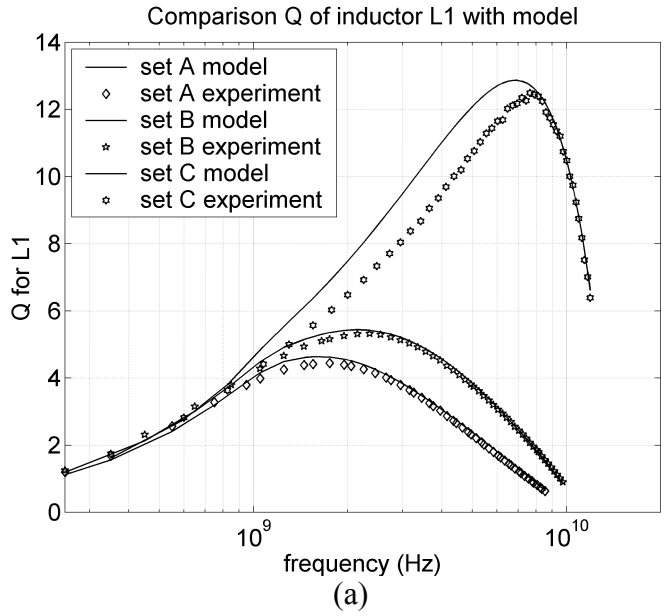


(b)

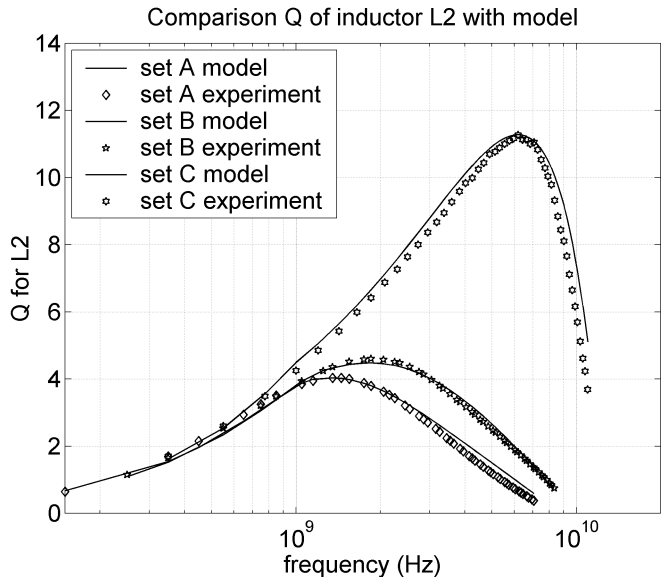
Figure 6.6 Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), Set C (micromachined) measured by conventional (Q) and LC tank definitions (QLC) of *Q* for inductors (a) L3, (b) L4

inductor design was made in the standard digital logic process and the total thickness of the inductor metal was 1 μm, and yet quality factors of greater than 10 have been achieved.

Post-CMOS micromachining represents a solution that reduces both the capacitance to substrate and the inter-turn capacitance. The addition of closely-spaced copper layers with interleaved low-K dielectric offers a high mutual inductance between the parallel layers [121].



(a)

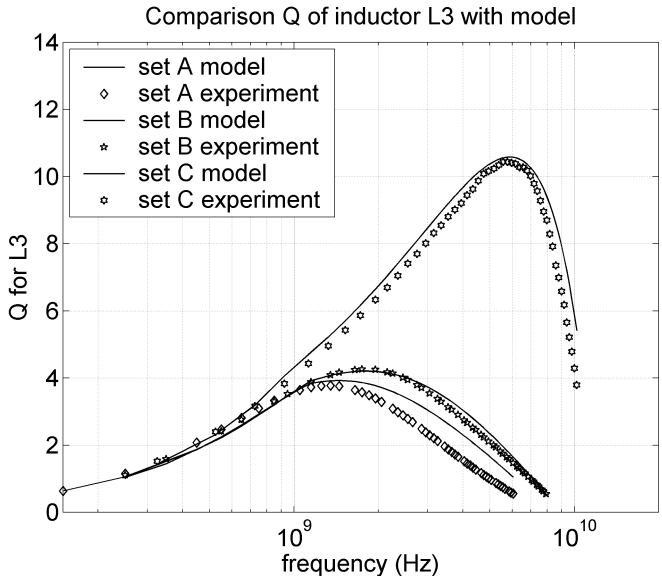


(b)

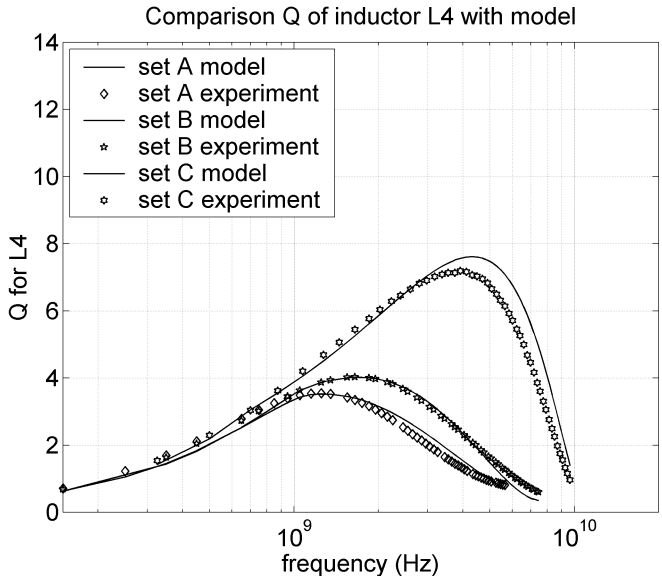
Figure 6.7 Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), Set C (micromachined) with the model predictions, for inductors L1-L4, for inductors (a) L1, and (b) L2

This means that use of multi-level layers with CMOS micromachining will reduce series resistance without significant reduction in inductance, improving overall performance.

Design of high quality passives for circuits in the 5-6 GHz band [122] is possible with micromachining on a standard CMOS process. The model developed for micromachined inductor can be used to evaluate the improvement in Q factor obtained by increasing the metal thickness. For example, Figure 6.9 shows the improvement in Q by increasing metal thickness with and



(a)



(b)

Figure 6.8 Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), Set C (micromachined) with the model predictions, for inductors L1-L4, for inductors (a) L4, and (b) L4

without micromachining for the L1 inductor. Without micromachining, the change is significant at 1 GHz, but at 5.5 GHz no improvement is gained, as substrate losses dominate the Q degradation. However, with the additional micromachining, the Q does improve at both frequencies. The improvement in Q at 5.5 GHz is lower than that at 1 GHz, as the skin depth limits the improvement of Q with increasing frequency. The quality factor of the micromachined inductor is predicted to be limited by the D.C. series resistance for metal thicknesses below 6μm.

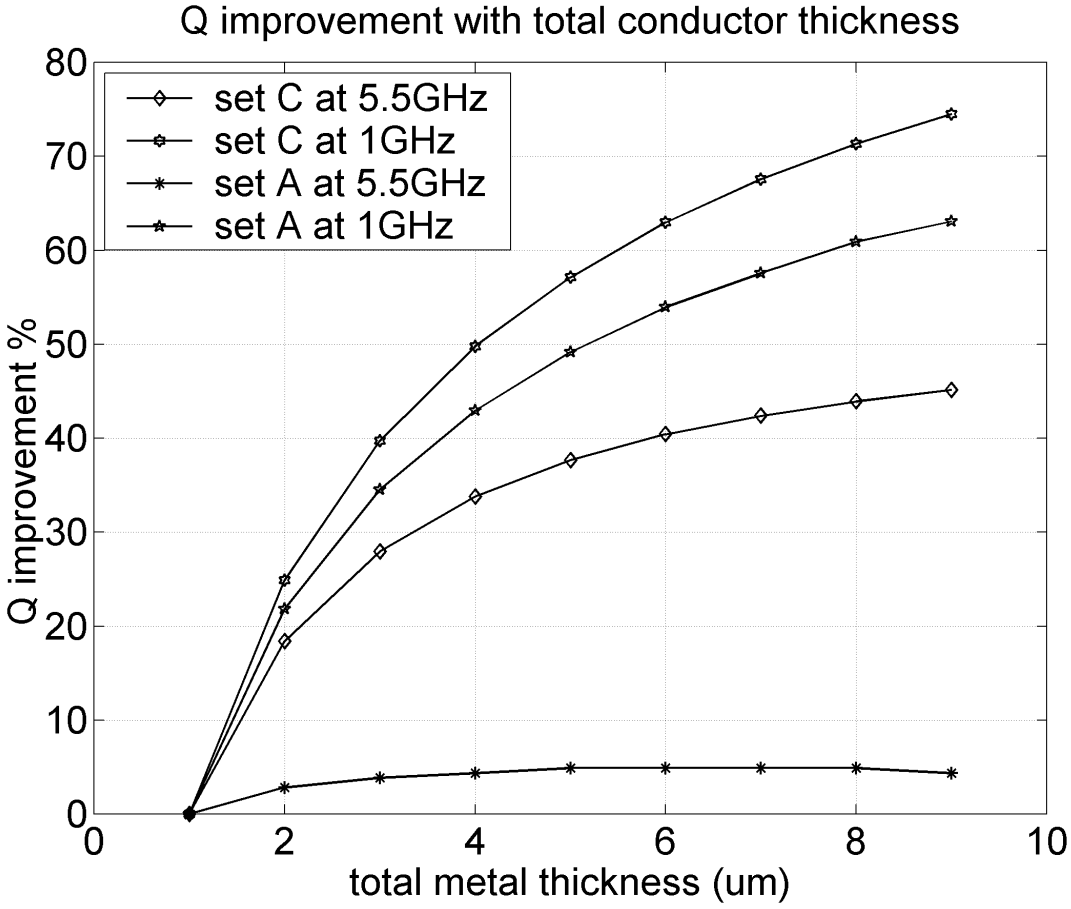


Figure 6.9 The percentage improvement in *Q* with increase in metal thickness at 1 GHz and 5.5 GHz for inductor L1, with and without post-process micromachining.

Above this thickness, the inductance change with thickness must be included for best accuracy. Qualitatively, for thicker metal layers, the series resistance becomes limited by skin effects, the inter-turn capacitance increases and the self-resonance is lowered. All of these effects conspire to limit the Q. From Figure 6.9, the thickness limit is estimated at about 10 μm, and conservatively at 6 μm.

Substrate coupling is an important consideration in design of RF analog circuits placed close to digital circuits. Design of deep trenches in the silicon separating the analog block from the digital block is an interesting application of this technology to reduce substrate coupling. This is easily implemented by designing a moat around critical circuit blocks. The removal of substrate also improves the performance of metal-insulator-metal (MIM) capacitors as the parasitic capacitance to substrate is reduced. The use of multiple metal layers shunted together can help reduce the resistance of the MIM structure.

The use of top metal as a mask is not very convenient, as this layer cannot be used freely for circuit interconnect. The top metal also introduces increased interconnect parasitics. An extra non-critical masking step to protect the circuits from post-CMOS micromachining can be included to free the top metal for interconnects. However, this step was not feasible to implement on the die-level prototype.

6.5 Conclusions

Post-CMOS micromachining improves the performance of CMOS inductors, as validated through experimental measurements. A physics-based model based on earlier literature predicts the improvement in performance obtained by micromachining. The quality factor of conventional on-chip inductors at higher frequencies is limited by substrate losses and removal of silicon reduces these losses by 100% to 180%. Reduction of the inter-turn capacitance through dielectric removal and of the capacitance to substrate through silicon undercut increases the self-resonance by 40% to 70%. Micromachined inductor Q is limited by series resistance up to thicknesses of about 6 μm. Post-CMOS micromachining is an option to leverage the ever-increasing performance of active components with high quality passives in higher frequency wireless communications.

Chapter 7. Conclusions

An understanding of structural curl in CMOS micromachined devices, along with its temperature variation is important in design. A methodology for characterization of stress, using test structures, for any CMOS process was developed during the course of this research. Simulation of complicated devices using experimentally extracted mechanical properties yields an accurate estimate of the device curl with temperature. Tools developed for automatically meshing structures helps designers simulate large devices. The tools allow for an iterative design of micromachined structures to attain the desired specifications.

The in-plane curl in CMOS micromachined process was exploited in the design of a compact IR imaging pixel. Results indicate that this structure has the potential to yield low-cost imaging arrays applicable to various personal safety, security, and law-enforcement applications.

A z-axis CMOS micromachined accelerometer was designed using an iterative finite element simulation methodology. This device exploits the differences in structural curl of beams with different metal and oxide composition, to create a vertical comb drive. The z-offset between the rotor and stator combs is a function of temperature, and hence the D.C. offset and the sensitivity of the device are temperature-dependent. Such a sensor needs a temperature compensation scheme, for operation over a large temperature change. This device was used as a test bed for an integrated micro-oven temperature control scheme.

The main focus of this research was the demonstration of a temperature compensation scheme for CMOS micromachined sensors that maintains a constant device temperature using integrated heaters. This is the first time that a integrated temperature control has been implemented for a micromachined sensor. This technique exploits the available polysilicon layer to enable an integrated single-chip solution. The technique can be applied to any CMOS micromachined sensor, as the polysilicon layer is not used as a structural layer.

In a separate effort, CMOS-micromachined inductors for RF applications on a copper interconnect 0.18 μm CMOS process with low-k dielectrics were designed, modeled and tested. The verified model predicts Q enhancement for micromachined inductors with thickness. The demonstration of the CMOS micromachining technology for a process with newer materials and applications, is proof of the versatility of the CMOS micromachining technology.

7.1 Future Work

To design iteratively the temperature distribution in CMOS micromachined devices, finite element simulation presents a time consuming approach. This approach becomes increasingly more difficult as MEMS design becomes mature, and more complicated devices are designed. NODAS, developed at CMU, is a behavioral simulator based tool that can accurately model mechanical and electrical effects in MEMS structures like beams, plates and comb drives [18][31]. The finite difference based approach demonstrated in this thesis, can be incorporated directly within the NODAS framework to enable simulation of temperature distribution. The inclusion of thermomechanical stress effects discussed in Chapter 2 can be included in NODAS for the simulation of stress and temperature variation. The possibility of combining thermomechanical simulation within the NODAS framework would enable design of microstructure whose performance meets specifications for residual stress effects and temperature variation.

The nominal or room temperature curl in CMOS micromachined structures can be reduced by deposition of a stress compensating layer. The choice of the material must be such that all layers used in the design have reduced curl. The knowledge of the extracted stress values of each layer can help in the choice of the material, and its thickness.

Embedding polysilicon resistors on CMOS micromachined plates can serve as interesting circuit elements. Their resistance can be controlled by current flow through another polysilicon heater resistor on the same plate. This produces an electrically tunable resistor element that can be used in the design of the band-gap references and automatic gain control circuits.

References

1. Low Cost 2g/10 g Dual Axis iMEMS® Accelerometers with Digital Output (Datasheet, Rev. B - 4/99) http://www.analog.com.
2. Sherman, S. J, Tsang, W.K.; Core, T.A., Payne, R.S., Quinn, D.E., Chau, K.H.-L, "A low cost monolithic accelerometer; product/technology update", *International Electron Device Meeting*, San Francisco, CA, Dec 1992.
3. H. Xie, G. K. Fedder, "A CMOS-MEMS Lateral-axis Gyroscope", in *14th IEEE International Conference on Micro Electro Mechanical Systems*, Interlaken, Switzerland, January 21-25, 2001.
4. H. Luo, G. K. Fedder, L. R. Carley, "An Elastically Gimbaled Z-Axis CMOS-MEMS Gyroscope", in *International Symposium on Smart Structures and Microsystems 2000*, Hong Kong, Oct. 19-21, 2000.
5. H. Luo, G. K. Fedder*, L. R. Carley, "A 1 mG Lateral CMOS-MEMS Accelerometer", in *13th Annual International Conference on Micro Electro Mechanical Systems*, Miyazaki, Japan, Jan 23-27, 2000
6. H, Xie, G. K. Fedder, "A CMOS Z-axis Capacitive Accelerometer With Comb-finger Sensing", in *13th Annual International Conference on Micro Electro Mechanical Systems*, Miyazaki, Japan, Jan 23-27, 2000.
7. G. Zhang, H. Xie, L. DeRosset, G. K. Fedder, "A Lateral Capacitive CMOS Accelerometer with Structural Curl Compensation", *MEMS `99* Orlando, FL, Jan 17-21, 1999.
8. G. K. Fedder, S. Santhanam, M. L. Reed, S.C. Eagle, D. F. Guillou, M. S-C. Lu, L. R. Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process," *Sensors and Actuators*, A-57, pp 103-110, 1996.
9. X. Zhu, "Bulk and surface micromachined CMOS", Ph.D thesis, Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh PA, April 2002 <fix>
10. X. Zhu, D. W. Greve, G. K. Fedder., "Characterization of Silicon Isotropic Etch by Inductively Coupled Plasma Etch in Post-CMOS Processing", in *13th Annual International Conference on Micro Electro Mechanical Systems*, Miyazaki, Japan, Jan 23-27, 2000.

11. X. Zhu, D. W. Greve, R. Lawton, N. Presser, G. K. Fedder, “Factorial Experiment on CMOS-MEMS RIE Post Processing”, in *194th Meeting of Electrochemical Society*, Boston, Massachusetts, November 1-6th, 1998
12. H. Lakdawala and G. K. Fedder, “Analysis of temperature-dependent residual stress gradients in CMOS Micromachined Structures”, *The 10th International Conference on Solid State Sensors and Actuators*, Sendai Japan, pp 526 -9, June 1999
13. R. M. White, R. C. Goyal “Stabilizing surface-wave devices against temperature variations” *Electronics Letters*, vol.8, no.6, p. 142-3 March 1972.
14. R. Ruby, P Merchant, “Micromachined thin film bulk acoustic resonators”, *Proc. 1994 IEEE International Frequency Control.* Boston, MA, June 1994.
15. J. Chen, K.D. Wise, “A silicon probe with integrated microheaters for thermal marking and monitoring of neural tissue” *IEEE Trans BME,* vol.44, no.8, pp. 770-4, August 1997.
16. C. T. C Nguyen, “Micromechanical resonators for oscillators and filters”, *Proc. 1995 IEEE International Frequency Control*. Seattle WA, Nov 1995.
17. C. H. Mastrangelo, “Thermal Applications of Microbridges”, Ph.D. Thesis, EECS, U. C. Berkeley, 1991.
18. G. K. Fedder., Qi Jing, “A Hierarchical circuit-Level design methodology microelectromechanical systems”, in *Transactions on Circuits & Systems II (TCAS), Special Issue on Behavioral Modeling and Simulation of Mixed Signal/Mixed Technology Systems*
19. S. Iyer, H. Lakdawala, G. K. Fedder and T. Mukherjee, “Macromodeling Temperature-Dependent Curl in CMOS Micromachined Beams”, in *Fourth International Conference on Modeling and Simulation of Microsystems*, Hilton Head Island, South Carolina, March 19-21, 2000.
20. S. Timoshenko, “Analysis of Bi-metal Thermostats”, *J. Optical Society of America*, 11, pp 233-255, 1925
21. M, Judy, “Micromechanisms Using Sidewall Beams”, Ph.D. Thesis, EECS, U. C. Berkeley, April 1994.
22. O. Paul, M. Von Arx, H. Baltes, “Process-dependent thermophysical properties of CMOS IC thin films” *Transducers 95,* Stockholm, Sweden, 1995, vol 1, pp 528-531.
23. M. S. Lu, X. Zhu, G. K. Fedder, “Mechanical Property Measurement of 0.5 μm CMOS Microstructures”, in *MRS 1998 Spring Meeting., Symposium: Microelectromechanical Structures for Materials Research*, April 13-17, 1998. San Francisco, CA.

24. S. Eagle, H. Lakdawala and G. K. Fedder, “Design and simulation of thermal actuators for STM applications in a standard CMOS process”, *Proc. SPIE - Int. Soc. Opt. Eng*. v3875 pp 32-9.
25. J. Buhler, “Deformable Micromirror Arrays by CMOS Technology”, Ph.D. Thesis No. 12139 ETH Zurich, Zurich Switzerland, 1997.
26. G. Zhang, “Design and Simulation of A CMOS-MEMS Accelerometer”, *M.S. Thesis*, Carnegie Mellon University, 1998
27. D. Freeman, A. Aranyosi, M. Gordon, S. Hong, “Multidimensional Motion Analysis of MEMS Using Computer Microvision”, *Solid State Sensor & Actuators Workshop*, Hilton Head Is., SC, 1998, p. 150-155.
28. Y. Gianchandani, K. Najafi, “Bent beam strain sensors” J. Microelectromechanical Systems, v5, issue1, March 1996, pp 52 -58
29. G. K. Fedder, “Structured Design of Integrated MEMS”, in *Twelfth IEEE International Micro Electro Mechanical Systems Conference*, Orlando, Florida, January 17-21 1999.
30. Q. Jing, G. K. Fedder, “NODAS 1.3 - Nodal Design Of Actuators And Sensors”, in *IEEE/ VIUF Int. Workshop on Behavioral Modeling and Simulation*, Orlando, FL, October 27-28, 1998.
31. T. Mukherjee, G. K. Fedder, “Hierarchical Mixed-Domain Circuit Simulation, Synthesis and Extraction Methodology for MEMS”, in *Journal of VLSI Signal Processing-Systems for Signal, Image and Video Technology*, pp. 233-249, July 1999.
32. S.A. Smee, M. Gaitan, D.B. Novotny, Y. Joshi, and D.L. Blackburn, “IC Test Structures for Multilayer Interconnect Stress Determination,” *IEEE Electron Device Letters*, Vol. 21, pp. 12-14, 2000.
33. MathWorks, Inc., Natick, MA, MATLAB Users Guide, 2000
34. MOSIS IC fabrication service, http://www.mosis.com
35. Coventorware User’s Manual, Coventor, Inc., Cary, NC 27513, http: //www.coventor.com.
36. L. Latorre, Y. Bertrand, and P. Nouet, “On the use of test structures for the electro-mechanical characterization of a CMOS compatible MEMS technology”, *Proc. IEEE 1998 Int. Conf. on Microelectronic Test Structures*, vol 11, March 1998
37. H. Lakdawala, B. Baidya, T. Mukherjee, Gary K. Fedder, “Intelligent Automatic Meshing Of Multilayer CMOS Micromachined Structures For Finite Element Analysis”, in *International*

Conference on Modeling and Simulation of Microsystems, San Juan Marriott Resort & Stellaris Casino, San Juan, Puerto Rico, April 19-21, 1999

38. D. Ramaswamy, N.R. Aluru, J. White, "A Mixed Rigid/Elastic Formulation for an Efficient Analysis of Electromechanical Systems", *Proc of MSM '98*, pp. 304-307.
39. B. Baidya, "MEMS Extraction", *M.S. Thesis*, Carnegie Mellon University, 1999
40. B. Baidya, S.K. Gupta and T. Mukherjee, "MEMS Component Extraction", in *International Conference on Modeling and Simulation of Microsystems*, San Juan Marriott Resort & Stellaris Casino, San Juan, Puerto Rico, April 19-21, 1999
41. B. Baidya, S. K. Gupta, T. Mukherjee, "Feature-Recognition For Mems Extraction", in 1*998 ASME Design Engineering Technical Conferences*, Atlanta, Georgia, September 13-16, 1998
42. T. Mukherjee, G. K. Fedder, "Structured Design Of Microelectromechanical Systems", in *Proceedings of 34th Design Automation Conference*, Anaheim, CA, June 1997, pp. 680-685.
43. T. Mukherjee, Gary K. Fedder, "Design Methodology for Mixed-Domain Systems-on-a-Chip", in *IEEE Computer Society Workshop on VLSI*, Orlando, FL, April 16-17, 1998.
44. J. E. Vandemeer, "Nodal Design of Actuators and Sensors (NODAS)", *M.S. Thesis*, Carnegie Mellon University, 1998
45. G. K. Fedder, "Top-Down Design of MEMS", in C*onference on Modeling and Simulation of Microsystems Semiconductors, Sensors and Actuators*, San Diego, CA, March 27-29, 2000
46. MEMS material database. http://mems.isi.edu/
47. D. R. Lide, "CRC Handbook of Chemistry and Physics", 77th Edition CRC Press, Boca
48. R. Flannery, and J. E. Miller, "Status of uncooled infrared imagers", *SPIE conference on Infrared Technology and Applications,* Vol 1689, 1992, pp 379-395
49. B.E. Cole, R. E. Higashi, and R. A. Wood, "Monolithic Two-Dimensional Arrays of Micromachined Microstructures for Infrared Applications" *Proceedings of the IEEE*, Vol 86, no. 8 pp1679-1686.
50. R. A. Wood, C. J. Han, and P.W. Kruse, "Monolithic arrays of micromachined pixels for infrared applications", in *IEDM*, 1998 pp 459-462.
51. P. Kruse, R. Dodson, S. Anderson, L. Kantor, M. Knipfer, and T. McManus, "Infrared imager employing 160x120 pixel uncooled bolometer array", *SPIE conference on Infrared Technology and Applications, XX1V*, San Diego, CA, July 1998, vol. 3436, pp 572-577
52. C. Hanson, "Uncooled thermal imaging at Texas Instruments, SPIE vol 2020" Infrared Technology XIX (1993)

53. W. Lang, K. Kuhl and H. Sandmaier, “Absorbing layers for thermal infrared detectors”, Sensors and Actuators, vol. A, No. 34, pp. 243-248, 1992

54. C-C Lui and C. Mastrangelo “CMOS Uncooled Heat-Balancing Infrared Imager,” *IEEE Journal of Solid State Circuits*, v. 35, no. 4, April 2000.

55. W. Baer, T. Hull, K.D. Wise, K. Najafi and K.D. Wise, “A Multiplexed Silicon Infrared Thermal Imager,” *Transducers 1991*, June 1991, pp. 631-634.

56. A. Schaufelbuhl, N. Schneeberger, U. Munch, O. Paul, H. Baltes, “Uncooled low-cost thermal imager using micromachined CMOS integrated sensor array”, *Technical Digest of the IEEE International Conference on Solid-State Sensors and Actuators*, Sendai, Japan, Transducers 1999

57. R. Lenggenhager, “CMOS thermoelectric infrared sensor”, *Ph.D thesis*, ETH no.10744, ETH Zurich, 1994

58. T.D. Binnie; H.J. Weller, Z. He; D. Setiadi, “An integrated 16x16 PVDF pyroelectric sensor array“, *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, Volume: 47 Issue: 6, Nov. 2000 pp 1413 -1420

59. R. Amantes, C. M. Knoedler, F. P. Pantuso, V. K. Patel, D. J. Sauer, and J. R. Tower, “An uncooled IR imager with 5mK NEDT” *SPIE conference on Infrared Technology and Applications* Vol 3061 pp 210-22 1997

60. R. Amantes, L. A. Goodman, F. Pantuso, D. J. Sauer, M. Varghese, T. S. Villani, and L. K. White, “Progress towards an uncooled IR imager with 5mK NEDT”, *SPIE conference on Infrared Technology and Applications, XX1V*, San Diego, CA, July 1998, vol. 3436, pp 647-659

61. H. Lakdawala and G. K. Fedder, “CMOS Micromachined Infrared Imager Pixel”, in *Technical Digest of the IEEE International Conference on Solid-State Sensors and Actuators*, Munich, Germany, June 10-14, 2001, pp. 1548-1551.

62. D. Moser, R. Lenggenhager, H. Baltes “Silicon gas flow sensors using industrial CMOS and bipolar IC technology” *Sensors and Actuators* A. vol 25/27 pp 577-581, 1991

63. H. Baltes, O. Paul, O Brand, “Micromachined Thermally Based CMOS Microsensors”, *Proc. IEEE*, vol 86, no. 8, August 1998.

64. M. Von Arx, O. Paul, H. Baltes, “Determination of the heat capacity of CMOS layers for optimal CMOS sensor design”, *Sensors and Actuators* A. vol 46/47 pp 428-431, 1995

65. A. S. Jensen, “Temperature limitations to infrared detectors”, *SPIE conference on Infrared Technology and Applications,* vol. 1308, 1990, pp 284-292

66. A. S. Jensen, “Limitations to room temperature IR imaging systems”, *SPIE conference on Infrared Technology and Applications*, *XIX*, 1993, vol. 2020, pp 340-350

67. C. Nguyen, “Micromechanical signal processors”, Ph.D. Thesis, EECS, U. C. Berkeley, Dec 1994.

68. M. Andrews, I. Harris, G. Turner, “A comparison of squeeze-film theory with measurements on a microstructure”, *Sensors and Actuators A*, vol. A36, pp 79-87, March 1993.

69. G. K. Fedder, “Simulation of Microelectromechanical Systems”, Ph.D. Thesis, EECS, U. C. Berkeley, 1994.

70. W.C. Tang, T.-C.H. Nguyen, and R. T. Howe, “Laterally driven polysilicon resonant microstructures”, *Sensors and Actuators*, vol 20, pp25-32, 1989.

71. W. C. Tang, T.-C.H. Nguyen, M. W. Judy, and R. T. Howe “Electrostatic comb drive of lateral polysilicon resonators”, *Sensors and Actuators*, vol 21-23, pp328-331, 1990.

72. S. Iyer, “Layout Synthesis of Microresonators”, *M.S. Thesis*, Carnegie Mellon University, 1998

73. Wyko white light interferometer, NT3300 user manual, http://www.veeco.com/

74. O. Paul and H. Baltes, “Novel fully CMOS compatible vacuum sensor” *Sensors and Actuators* A. vol 46/47 pp 428-431, 1995.

75. *Rapheal* Interconnect Analysis Software user manual, http://www.avanticorp.com

76. *S-PLUS* User Manual, http://www.insightful.com/products/

77. T. B. Gabrielson, “Mechanical-thermal noise in micromachined acoustic and vibration sensors”, *IEEE Trans on Electron Device*, ED-40(5), pp178-195

78. X. Zhang, W. C. Tang, “Viscous air damping in laterally driver microresonators”, *IEEE Micro-Electro-Mechanical Systems Conference,* 1994, pp. 199 - 205.

79. Cadence Electronic Design Automation Software, http://www.cadence.com

80. A. Burstein and W. J. Kaiser, “Mixed analog-digital highly sensitive sensor interface circuit for low-cost microsensors,” *Sensors Actuators A,* vol. 52, pp. 193–197, 1996.

81. D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, New York, 1997

82. R. Brederlow, W. Weber, C. Dahl, D. Schmitt-Landsiedel, and R. Thewes, "Low-Frequency Noise of Integrated Poly-Silicon Resistors", *IEEE Trans. Electron Devices*, vol. vol-48, no.6, pp. 1180–1187, June 2001.
83. Bruel and Kjaer Model Type 4394, accelerometer, http://www.bkhome.com
84. B. E. Boser and R. T. Howe, "Surface micromachined accelerometers," *J. Solid-State Circuits,* vol. 31, pp. 366–375, 1996.
85. H. Lakdawala, G. K. Fedder, "Temperature Control of CMOS Micromachined Sensors", in *15th IEEE International Conference on Micro Electro Mechanical Systems*, Las Vegas, Nevada, January 22-26, 2002, pp 324-327.
86. M. A. Lemkins, "Micro Accelerometer Design with Digital Feedback Control", Ph.D. Thesis, EECS, U. C. Berkeley, Fall 1997
87. LM199/ LM299/ LM399/ LM3999 precision voltage reference integrated circuit available from National Semiconductor, http://www.national.com
88. D. Harmon, J. Gill, T. Sullivan, "Thermal Conductance of IC Interconnects Embedded in Dielectrics", IRW Final Report, pp 1-9, 1998.
89. Holman, J. P., "Heat Transfer", McGraw-Hill Higher Education, 1996 ISBN: 00784478526
90. IMSL C library, http://www.vni.com/products/imsl/
91. A. S. Sedra, K. C. Smith, "Microelectronic circuits", Oxford University Press, July 1997
92. M. Ou-Yang, C-S Sheen, and J-S. Shie, "Parameter extraction of resistive thermal microsensors by A.C. electrical method", I*EEE Transactions on Instrumentation and Measurement*, vol 47, no. 2, April 1998
93. Y-M. Chen, T. Hwang, and C-S Sheen, "Parameter extraction of resistive thermal sensors", *Sensors and Actuators* A 55 (1996) pp 43-47
94. LabVIEW reference manual, http://www.natinst.com/labview/
95. H. Xie, Y. Pan, G. K. Fedder, "A SCS CMOS micromirror for optical coherence tomographic imaging", *15th IEEE International Conference on Micro Electro Mechanical Systems*, Las Vegas, Nevada, January 22-26, 2002, pp 495-498.
96. J. N. Burghartz, M. Hargrove, C. S. Webster, R. A. Groves, M. Keene, K. A. Jenkins, R. Logan, E. Nowak, "RF Potential of a 0.18μm CMOS Logic Device Technology", *IEEE Trans Electron Devices*, vol-47, no. 4, pp 864-870, April 2000.

97. A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. V. Surovic, B. L. Krauter, D. C. Edelstein, P. J. Restle, "On-chip Wiring Design Challenges for Gigahertz Operation", *Proc. IEEE*, vol-89, no. 4, April 2001

98. N. H. Nguyen, R. G. Meyer, "Si IC-Compatible Inductors and Passive Filters", *IEEE J. Solid-State Circuits*, vol-25, no. 4, Aug. 1990.

99. J. N. Burghartz, D.C. Edelstein, M. Soyuer, H. A. Ainspan and K. A. Jenkins, "RF Circuit Design Aspects of Spiral Inductors on Silicon", *J. Solid State Circuits*, vol-33, no. 12, pp 2028-2034, Dec. 1998.

100. C. P. Yue, and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's", *J. Solid State Circuits*, vol-33, no. 5, pp 743-751, May 1998.

101. K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek and S. Moinian, "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process", *J. Solid State Circuits*, vol-31, no. 1, pp 4-9, Jan 1996.

102. J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, and Y. H. Kwark, "Spiral Inductors and Transmission Lines in Silicon Technology Using Copper-Damascene Interconnects and Low-Loss Substrates", *IEEE Trans Microwave Theory Tech.*, vol-45, no. 10, pp 1961-1968, Oct 1997.

103. J. Y. C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2 μm CMOS RF amplifier," *IEEE Electron Device Letters*, Vol. 14, No. 5, May 1993, pp 246-248.

104. A. Rofougaran, J. Y-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct Conversion Wireless Receiver", *IEEE J. Solid-State Circuits*, vol-31, no.7, July 1996.

105. M. Ozgur, M. E. Zaghloul, M. Gaitan, "Optimization of Backside Micromachined CMOS Inductors for RF applications", IEEE International Symposium on Circuits and Systems, May 28-31, Geneva, Switzerland, pp V-185-188.

106. K Ng, N. Pham, L. Sarro, B. Rejaei, J. Burghartz "Characterization of a Bulk-Micromachined Post-Process Module for Silicon RF Technology", 2000 Topical Meetings on Silicon Monolithic Integrated Circuits in RF Systems, pp 99-102, April 2000.

107. R. P. Rabbis, J. Lescot, J-L Leclercq, J. M. Karam, F. Ndagijimana, "Micromachined Microwave Planar Spiral Inductors and Transformer", *IEEE Trans Microwave Theory Tech.*, vol-42, no. 9, pp 1750-1758, Jan 1996.

108. H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, G. K. Fedder, "Micromachined High Q inductors in 0.18 μm Cu interconnect Low-K CMOS", in Proc. IEEE Custom Integrated Circuits Conf., San Diego, May 2001, pp 579-82.

109. A. Zolfaghari, A. Chan, B. Razavi, "Stacked Inductors and Transformers in CMOS Technology", *J. Solid State Circuits*, vol-36, no. 4, pp 620-628, April 2001.

110. X. Zhu, H. Lakdawala, H. Luo, S. Santhanam, D. W. Greve, G. K. Fedder, "Copper Interconnect Low-K Dielectric Post-CMOS Micromachining", in *Technical Digest of the IEEE Int. Conf. on Solid-State Sensors and Actuators*, Munich, Germany, June 10-14, 2001, pp. 1548-1551.

111. M. Kamon, J. Ttsuk, and J. K. White, "FASTHENRY: a multipole-accelerated 3-D inductance extraction program", *IEEE Trans Microwave Theory Tech.*, vol-42, no. 9, pp 1750-1758, Jan 1996.

112. R. Groves, D. L. Harame, and D. Jadus, "Temperature Dependence of Q and Inductance in Spiral Inductors Fabricated in a Silicon-Germanium/BiCMOS Technology" *J. Solid State Circuits*, vol-32, no. 9, pp 1455-1459, Sept 1997.

113. C. P. Yue, and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon", *IEEE Trans Electron Devices*, vol-47, no. 3, pp 560-568, Mar 2000.

114. J. R. Long, and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's", *J. Solid State Circuits*, vol-32, no. 3, pp 4-9, March 1997.

115. W. B. Kuhn, and N. M Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors", *IEEE Trans Microwave Theory Tech.*, vol-49, no. 1, pp 31-38, Jan 2001.

116. Y. Eo, and W. R. Eisenstadt, "High Speed VLSI Interconnnect Modeling Based on S-Parameter Measurements", *IEEE Trans. Comp., Hybrids, Manufact., Techol.* vol-5 no. 16, pp 555-562, June 1990.

117. S. E. Schwarz, "Electromagnetics for Engineers", Philadelphia, Saunders College Publishing, 1990

118. W. A. Johnson and L. K. Warne, "Electrophysics of Mechanical Comb Actuators", *J. Microelectromechanical Systems*, vol-4, no. 1, pp 49-59, Mar 1995.

119. J. Yuan, W. R. Eisenstadt, J. J. Liou, "A Novel Lossy and Dispersive Interconnnect Model for Integrated Circuit Simulation", *IEEE Trans. Comp., Hybrids, Manufact., Techol.* vol-13 no. 2, pp 275-280, June 1990.

120. A. M. Niknejad, and R. G. Meyer, “Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC’s”, *IEEE J. Solid-State Circuits*, vol-33, no. 9, Oct 1998.

121. J. N. Burghartz, M. Soyuer, and K. A. Jenkins, “Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology”, *IEEE Trans Microwave Theory Tech.*, vol-44, no. 1, pp 100-104, Jan 1996.

122. T. H. Lee, and S. S. Wong, “CMOS RF Integrated Circuits at 5 GHz and Beyond”, *Proc. IEEE*, vol-88, no. 10, Oct 2000

123. D. C. Ghiglia, M. D. Pritt, “Two-Dimensional Phase Unwrapping: Theory, Algorithms, and Software”, Wiley Publishing, 1998

Appendix I. A Method for Dynamic Microstructure Profiling for Large and Displacement using Light Emitting Diodes

I.1 Introduction

Dynamic shape measurement is an important tool for MicroElectroMechanical devices (MEMS). Present systems allow for only single point measurement of deflections. Commercial optical profilers cannot measure dynamic microstructures. Phase unwrapping techniques based on phase measurement are limited by their inability to resolve height difference between disconnected portions that are very common in MEMS devices. The phase unwrapping techniques also rely on laser illumination that produces speckling and spurious fringe data that is difficult to unwrap.

The techniques described in this appendix combine the phase unwrapping technique and white light interferometer concepts to enable systems that can measure large displacements with very good relative accuracy (< 5nm) and good absolute accuracy. The proposed measurement technique allows for accurate measurement of dynamic microstructures.

I.2 System Implementation

The main characteristics of the system are:

1. Use of a Mirau microscope objective in place of a normal microscope objective to create an interferometer.
2. Use of a light emitting diode as a monochromatic light source.
3. A piezoelectric stage objective stage for accurate objective motion.
4. Use of strobing to capture dynamic images.
5. Modified phase unwrapping algorithm to reconstruct device shape using image stitching and LED coherence property.

The base system is a retrofitted Zeiss microscope provided along with the MIT microvision that is used for single point dynamic measurements. Our work has been to modify the system for dynamic shape measurement using a Mirau interferometer (Figure II.1).

A Mirau objective is used to generate an interferometeric pattern on the microstructure. Several interferometeric images are taken with different piezoelectric objective stage motions. An example of an device with interference fringes is shown in Figure II.2.

Each of the measurements is synchronized in phase to the displacement. The above set of images have to be taken for every phase of the sinosoidal input waveform. The same algorithm as the microvision system is used to make these dynamic measurements. The five local images are used to compute the phase and envelope of the illumination. Five images are used, rather than the minimum three to reduce effects of non-linearity of the camera and z displacement error. The LED illumination is assumed to fit the following function

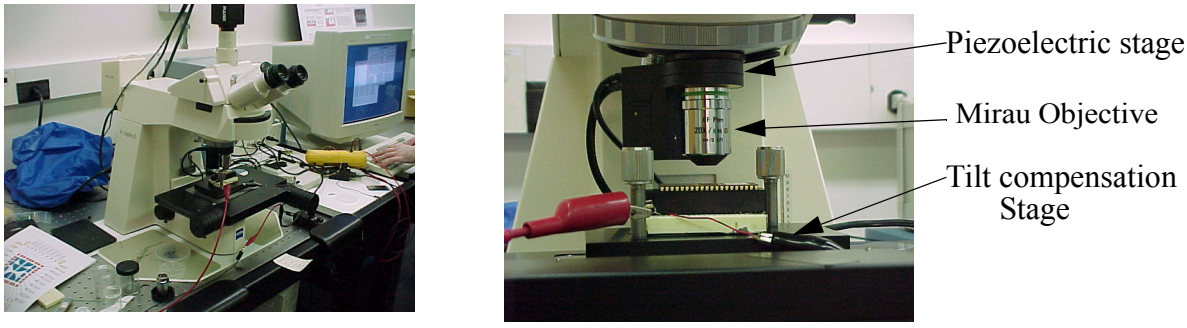


Figure II.1 (a) Photograph of the modifications to the MIT microvision system. (b). The Mirau objective along with the tilt compensation stage.

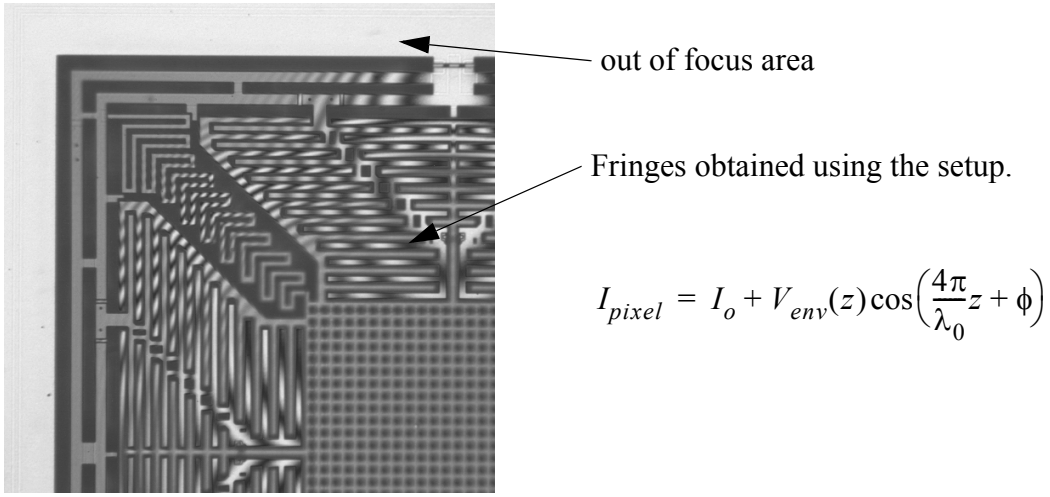


Figure II.2 A single measurement of a MEMS device with the setup.

$$I_{pixel} = I_o + V_{env}(z)\cos\left(\frac{4\pi}{\lambda_0}z + \phi\right) \tag{6.13}$$

where, I_{pixel} is the intensity of each pixel, I_o is the pixel intensity without presence of fringes, V_{env} is the intensity of the envelope, z is the motion of the objective and ϕ is the phase of the pixel. The 5 images are used to solve for I_o, V_{env} and ϕ using a discrete Fourier series expansion technique.

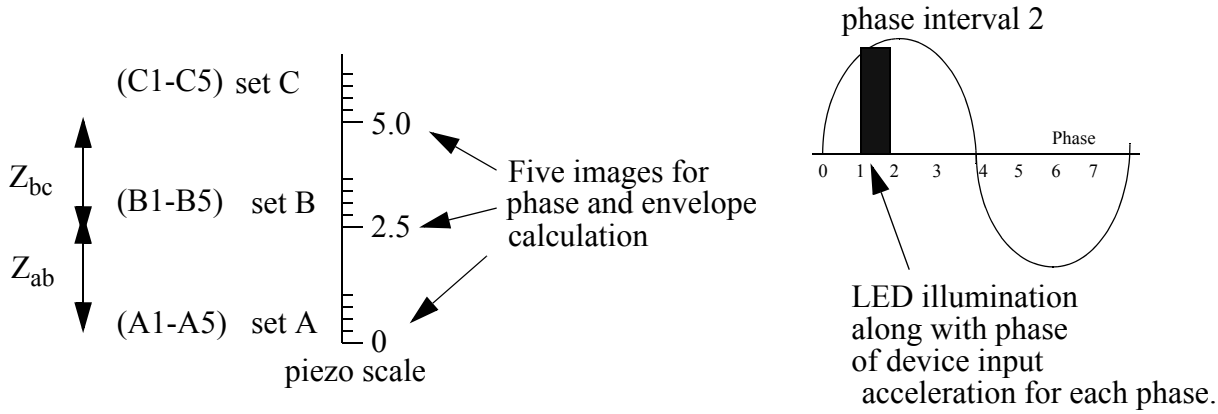


Figure II.3 The z displacements of the piezoelectric stage (optical path difference) for each LED illumination stroboscopically synchronized with the device excitation input. The same stroboscopic illumination concept as the MIT microvision system are used.

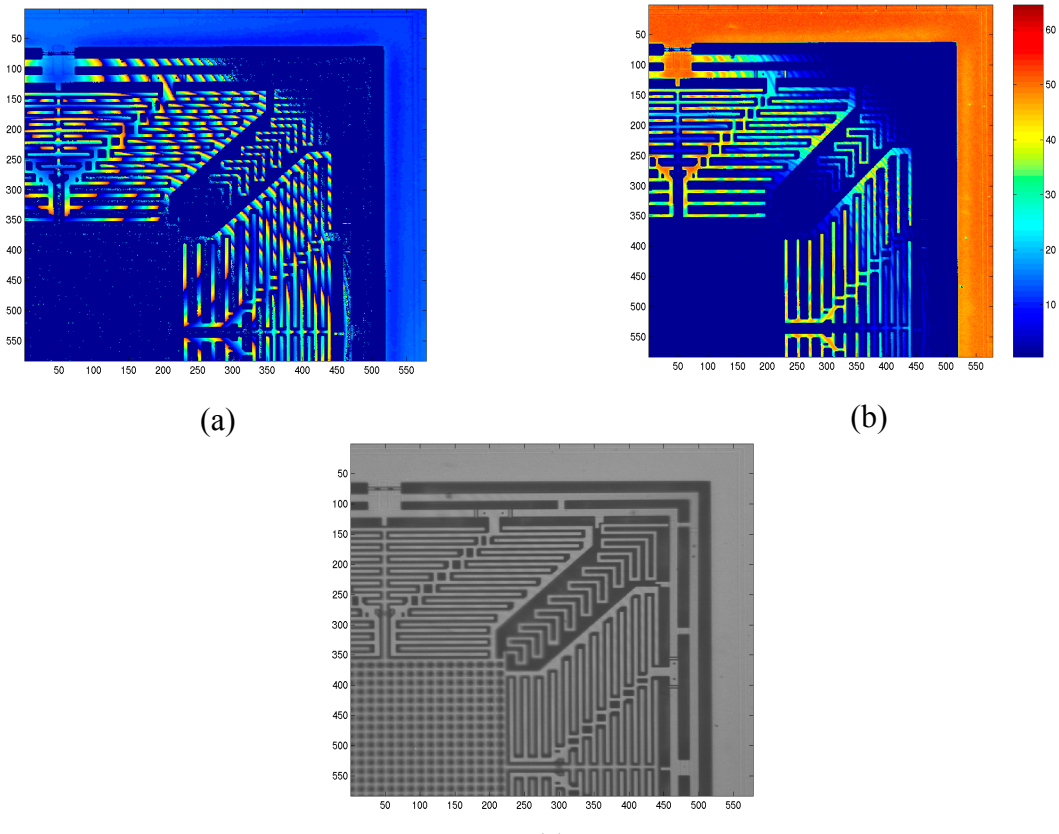


Figure II.4 (a) The phase map ϕ, (b) intensity map of V_{env} (c) and fringe-less image, I_o.

The image, I_o, does not have fringes and may be used for normal Microvision data analysis for x and y motion. ϕ is the phase of the pixel that is used to construct the phase map of the image.

The phase map of a typical measurement is shown in Figure II.4 (a). The intensity envelope of the image is shown in Figure II.4 (b). The fringeless image derived from the interferometeric images is shown in Figure II.4 (c). Similar intensity, phase and image maps are calculated for the other groups of interferometeric images (Denoted by set A, B and C see Figure II.3)

The four operations essential to the stitching process are

a. Phase Stitching

This process involves extracting the common portion in two successive sets and combining them to a common phase map. This process involves the computation of an average phase difference between the two common portions. ϕ_a and ϕ_b are the phase maps of set A and set B. The phase difference between set A and set B is expressed as

$$\Delta\phi_{ab} = \text{median}(\text{nonzeros}(\text{mod}(\phi_a - \phi_b + 2\pi, 2\pi))) \tag{6.14}$$

This computation is done only in regions covered by both ϕ_a and ϕ_b. The phase difference can also be used as a correction factor to calculated the actual motion of the piezoelectric actuator. The actual displacement of piezoelectric stage can be computed by

$$Z_{ab} = \text{mod}\,(Z_{set}, \lambda_0/2) + \lambda_0\Delta\phi_{ab}/4\pi \tag{6.15}$$

where, λ_0 is the wavelength of the LED. λ_0 is a constant and can be calculated using a separate calibration procedure, that needs a reference step. The phase of the common region between set A and B is

$$\phi_{ab} = \phi_b + \Delta\phi_{ab} \tag{6.16}$$

This computation is only made in areas defined by both set a and set b. All the phase values are set to zero. Similarly, the phase of the common region between set B and set C is computed as

$$\phi_{bc} = \phi_b \tag{6.17}$$

This computation is only made in areas defined by both set B and set C. The phase of the entire image is then calculated as

$$\phi_{all} = \phi_{ab} + \phi_{bc} \tag{6.18}$$

This expression is calculated in area (bc -ab). The illustration of the calculation of ϕ_{ab} and ϕ_{bc} to get the phase of the entire image is illustrated in Figure II.5.

b. Z-displacement Calculation And Data Merge

The z deflection of each pixel (z_p) is calculated from the knowledge of the intensity of the LED fringe pattern. The fringe pattern as function of optical path difference, z_p is expressed as

$$I_{pixel} = I_o + V_o \exp\left(-\frac{z_p^2}{2\sigma}\right)\cos\left(\frac{4\pi}{\lambda_0} z_p\right) \tag{6.19}$$

V_{env}, the envelope of the fringe intensity is expressed as a function of the optical path difference as

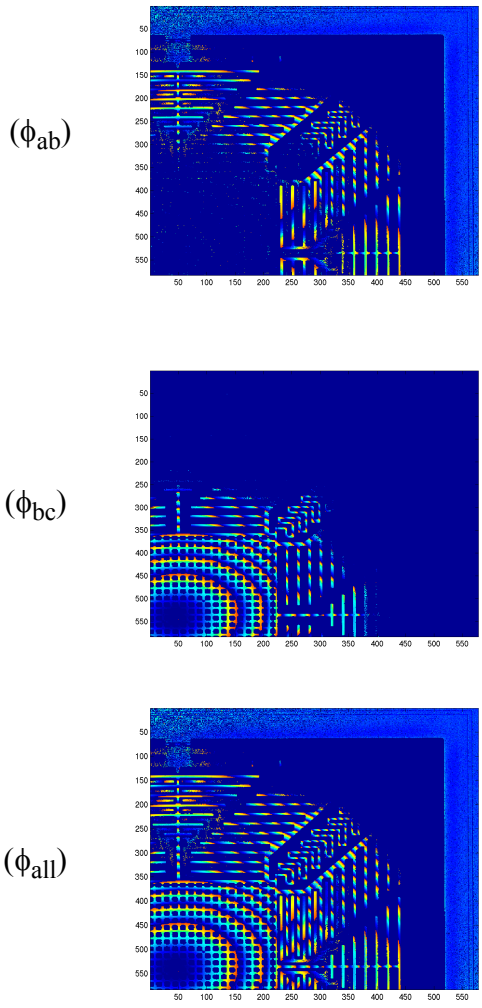


Figure II.5 Combination of phase maps of set AB (ϕ_{ab}) and set BC (ϕ_{bc}) to produce phase map of ABC (ϕ_{abc}).

$$V_{env} = V_o \exp\left(-\frac{z_p^2}{2\sigma}\right) \tag{6.20}$$

where V_o is the maximum value of the pixel envelope intensity. The σ is the property of the LED and can be characterized experimentally. The envelope value for the pixel in set A, V_a, and set B, V_b, are

$$V_a = V_o \exp\left(-\frac{(z_p - z_o)^2}{2\sigma}\right) \tag{6.21}$$

$$V_b = V_o \exp\left(-\frac{(z_p - z_o - Z_{ab})^2}{2\sigma}\right) \tag{6.22}$$

where z_o is some arbitrary z reference value. The reference value is nominally taken to be zero. The actual z value of the pixel is calculated solving (6.21) and (6.22) as

$$z_{pab} = z_0 + \frac{1}{Z_{ab}}\left(Z_{bc}^2 - \frac{4\sigma^2}{Z_{ab}} \operatorname{atanh}\left(\frac{V_b - V_a}{V_b + V_a}\right)\right) \tag{6.23}$$

This function is calculated in the common region between set A and set B. Similarly the pixel values for the region defined by set B and set C are computed as

$$z_{pbc} = Z_{ab} + z_0 + \frac{1}{Z_{ab}}\left(Z_{bc}^2 - \frac{4\sigma^2}{Z_{ab}} \operatorname{atanh}\left(\frac{V_b - V_a}{V_b + V_a}\right)\right) \tag{6.24}$$

The pixel z values are computed for all images by

$$z_{all} = z_{ab} + z_{bc} \text{ (in area bc -ab)} + z_{cd} \text{ (in area cd-bc)} + ... \tag{6.25}$$

In this manner, the entire z distribution of the image can be computed. An illustration of the z calculation to obtain the final z displacement map is shown in Figure II.6

c. Definition of the Active Measurement Region.

MEMS structures have narrow gaps and therefore normal phase unwrapping tends to produce erroneous results. The phase-unwrapping algorithm is guided by removing all regions that are not focussed. The identification of the focussed regions combined with thresholding of the I_o image data is used to derive regions where phase unwrapping can proceed. The focussed area is obtained

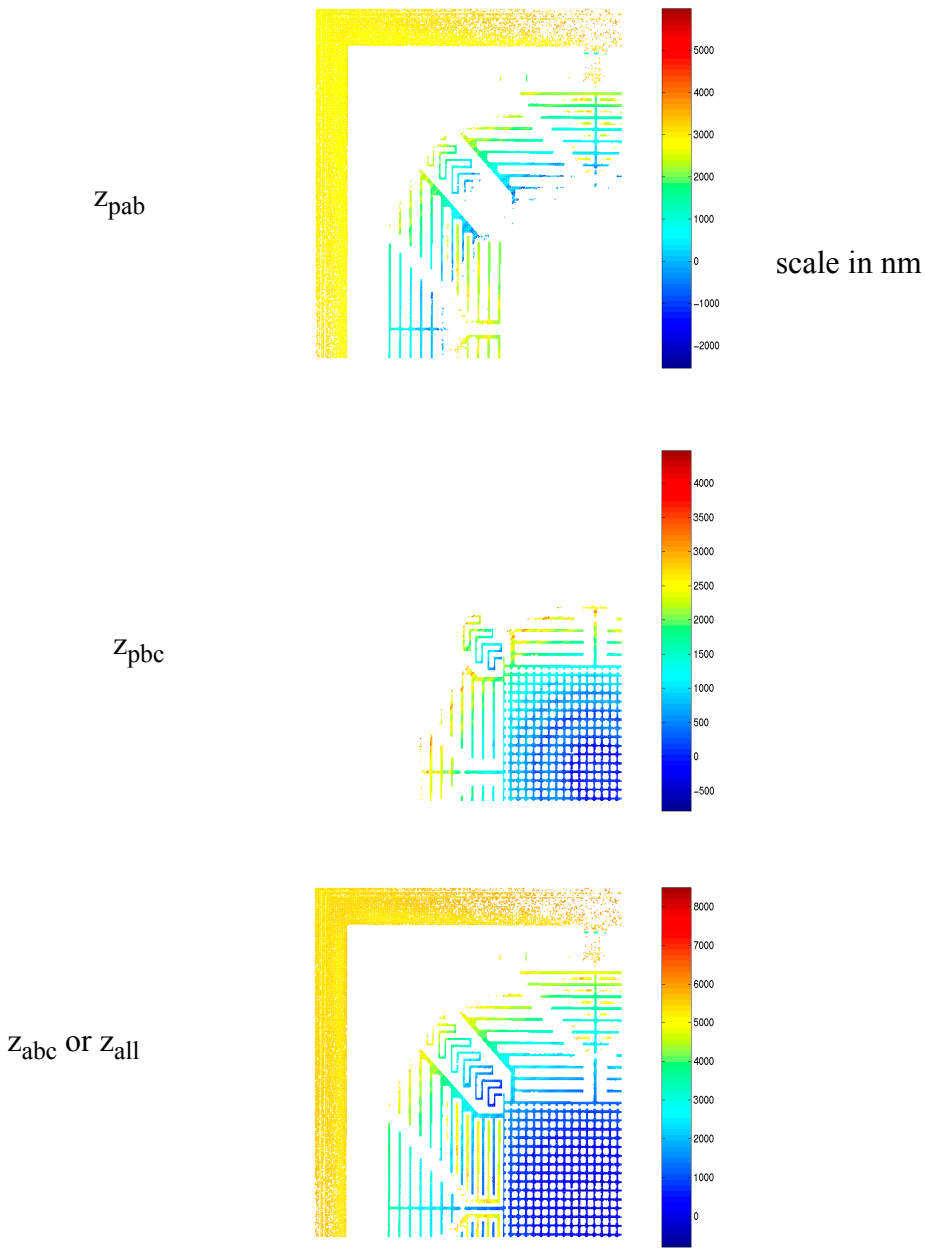


Figure II.6 Illustration of the pixel z displacement computation and merged z data

by thresholding the variance of the pixel values of the 5 images in set A. The threshold number has to be set by heuristics. The focussed image mask for set A is described as

$$M_a = (\text{Threshold } (\text{variance}(A1,A2,A3,A4,A5))) \text{ AND } ((\text{Threshold } (I_0)) \quad (6.26)$$

where A1-A5 are individual phase shifted images of set A. This method extracts a mask that contains only the best focussed points. This ensures that small gaps between the comb fingers are

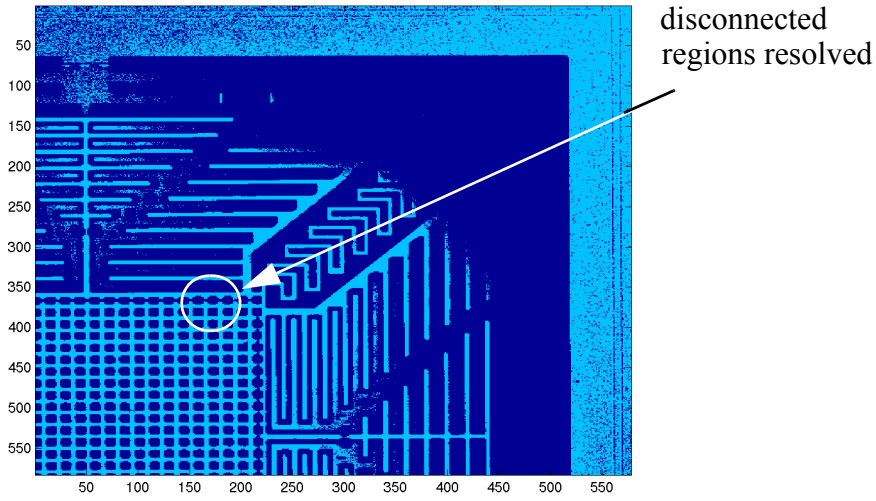


Figure II.7 The mask for feature-guided Goldsteins phase unwrapping algorithm derived from best focussed images.

correctly resolved without appearance of false connections. The mask of the entire image can be constructed by

$$M_{all} = (M_a \text{ AND } M_b) \text{ OR } (M_b \text{ AND } M_c) \tag{6.27}$$

The focussed area is obtained by the following criteria: If a fringe pattern is not seen during any of the images in a set, then the image is out of focus. It is important to note that the depth of field of Mirau object is larger than the coherence length of the LED. (This one of the reason laser illumination fails for many MEMS devices). The mask derived for phase unwrapping is shown in Figure II.7. Note that metal-3 edges abutting metal-2 structures of the CMOS process are visibly separate.

d. Z-displacement Map Guided Phase Unwrapping

The z displacement data computed can be improved in quality using the phase information. This technique is important as the relative information between the pixel is utilized. A modified version of Goldstein's phase unwrapping algorithm [123] was used to convert the phase change data to a z displacement. The modification introduced in the algorithm is the use of the z displacement data to derive starting points of the phase unwrapping. This technique ensures that relative z displacement of the disconnected pieces is maintained. One important implementation detail is that the phase unwrapping occurs in a region that is in focus and does not occur at any other pixel. This ensures that narrow gaps (common in MEMS structures) are not shorted to

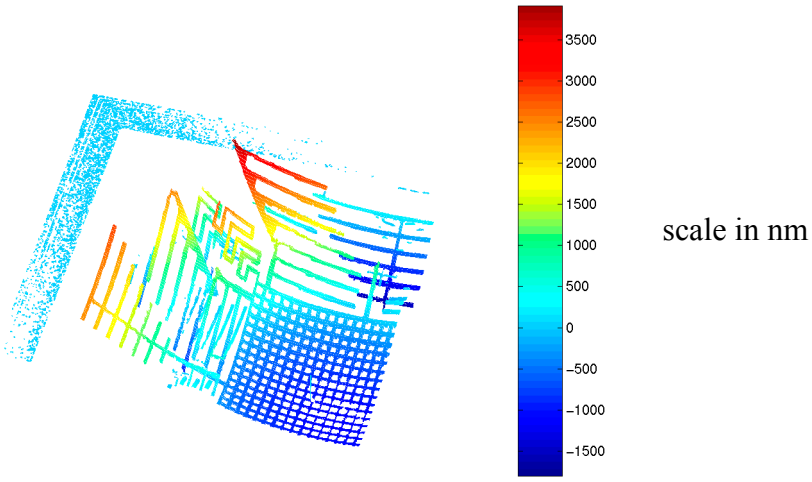


Figure II.8 The phase unwrapped result without the image intensity correction technique. Note that the disconnected regions and the scale are relative.

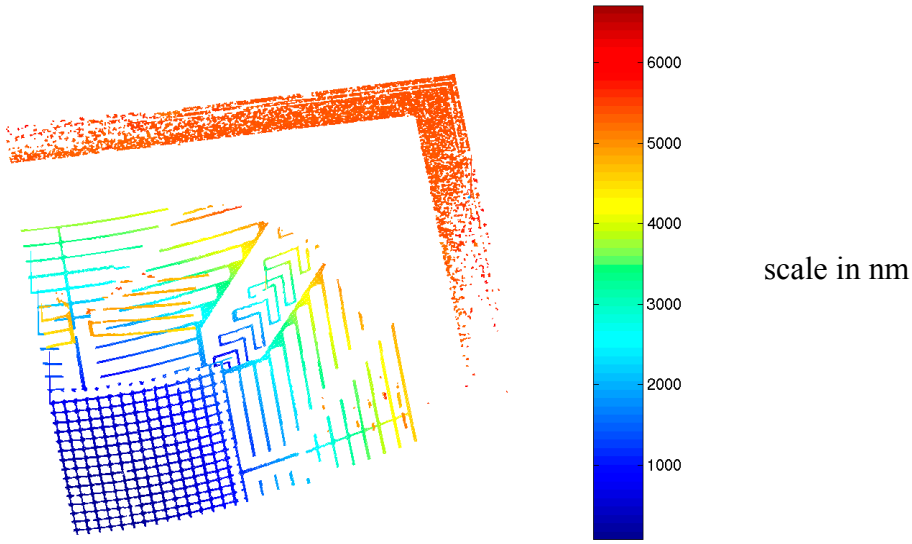


Figure II.9 The final profile measurement of the of the example devices. Note that disconnected regions have the correct absolute z displacement value

obtain erroneous phase unwrapping. The mask data is derived using the techniques mentioned previously.

The final phase unwrapped result using image intensity guided algorithm is shown in Figure II.9. The phase unwrapped result without intensity guided algorithm is shown in Figure II.8 Several such refined measurements can be combined to produce the final device profile.

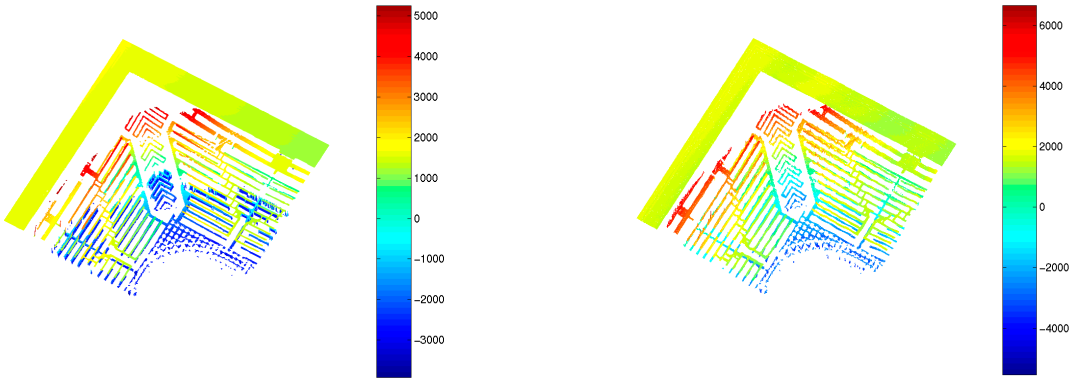


Figure II.10 Measurement of device profile for 0 phase of a 100Hz signal for 4 sets of image data. (a) intensity phase corrected measurement (b) The curl calculated from the intensity data.

$$Z_{full} = Z_{pcA} + Z_{pcB} \tag{6.28}$$

calculated in area of set ABC -set BCD. Several such maps can be summed together to stitch the final image. Another example in which Z images were stitched together is shown in Figure II.10.

Appendix II. Accelerometer Interface Circuits and Test Board Design

II.1 Z-axis Accelerometer Details

The results of the measurements of the accelerometer are based on the prototype CMOS die obtained from the MOSIS (http://www.mosis.com). An Agilent 0.5 μm CMOS process (Run no. Dec 4 2001, actuators61b, MOSIS die no. N9CNAQ, design no. 59410) was used.

The pins that are required for the sensor are

1. Pin D1vddclk.: 5V, digital voltage supply rail.

2. Pin D1vddmainckt.: 5V, analog voltage supply rail.

3. Pin V_{refp}: positive reference =3.5V

4. Pin V_{refn}: negative reference =1.5V

5 Pin Input_clk: input clock, the duty cycle of the input clock determines the time, clocks ph1 and ph3 are high.

6. Pin VSS!: ground.: 0V

7. Pin D1out: final output.

8 Pin VCM!: analog ground ~ 2.5V D.C.

9. Pin V_{ft}, DC supply for compensation of charge injection at the sense node.

10. Pin temp_d1: output voltage proportional to the chip temperature.

The layout of the test chip (actuators61b) with the location of the various devices on the chip is shown in Figure II.1

II.2 Description of Circuit Blocks

This section describes of some of the most important circuits blocks cells developed in the course of this thesis. These cells have been tested in several runs in the Agilent 0.5 μm process and the AMS 0.6 μm process. The cell are located in the cadence design library

Folded Cascode Opamp

Library Name: /afs/ece.cmu.edu/usr/hasnain/cadence/April00

Cell Name: foldedcascode (Figure II.2)

Views: layout, schematic, extracted, symbol

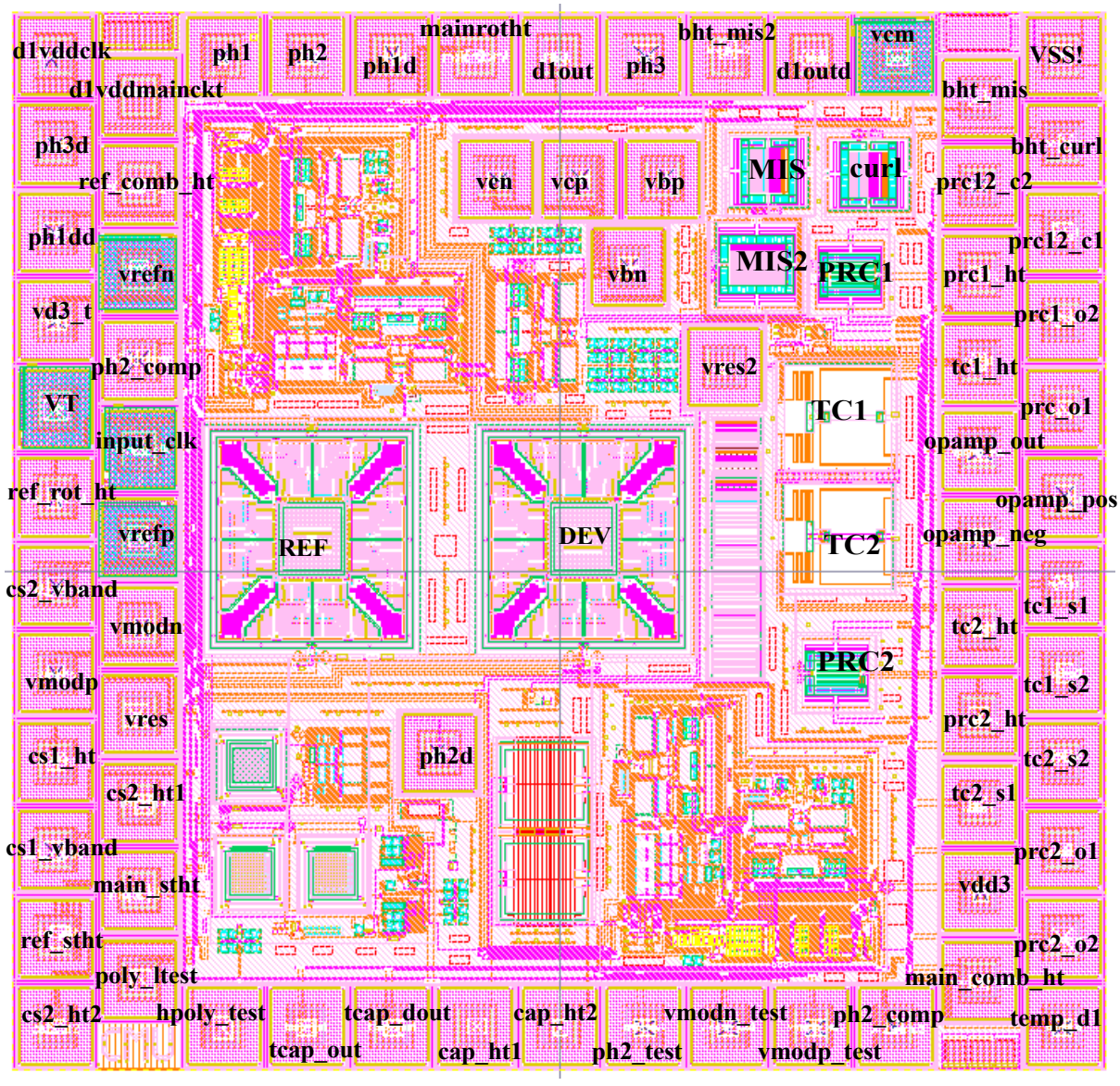


Figure II.1 The layout of the test chip the temperature controlled Z-axis accelerometer and the stress characterization test structures.

Purpose:

This cell describes a opamp with the following specifications.

f3db = 58MHz, Phase Margin = 80^{o}, Gain @ DC = 120dB

Test Deck Information

Library Name: /afs/ece.cmu.edu/usr/hasnain/cadence/April00

Cell Name: foldedcascode_sim2

Views: schematic, config

Uses the hierarchy editor to simulate the AC, DC and transient response of the opamp circuit.

Bias Circuit Information

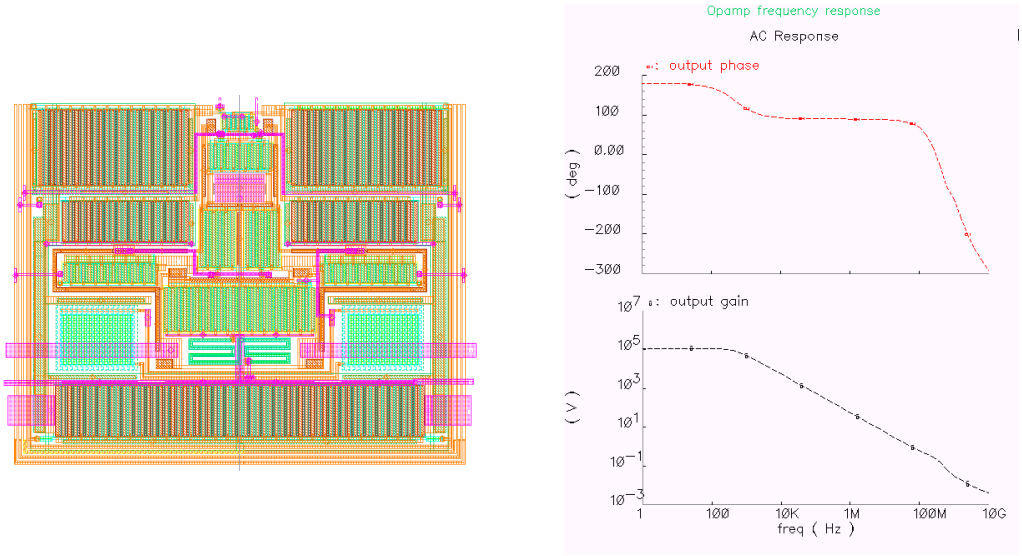


Figure II.2 Layout and the simulation result of A.C phase and magnitude response of the foldedcascode operational amplifier

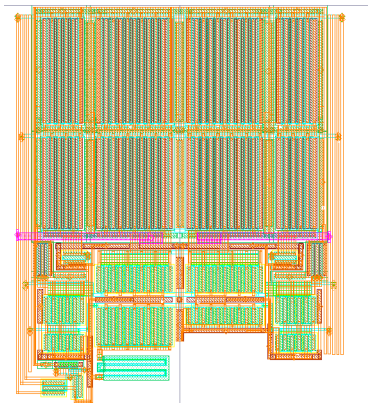
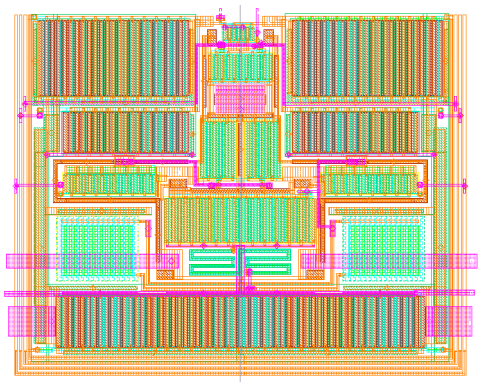


Figure II.3 Layout of the D.C. bias generation cell. The D.C voltages Vbn, Vcn, Vbp, and Vcp used to generate the bias voltages for the folded cascode opamp.



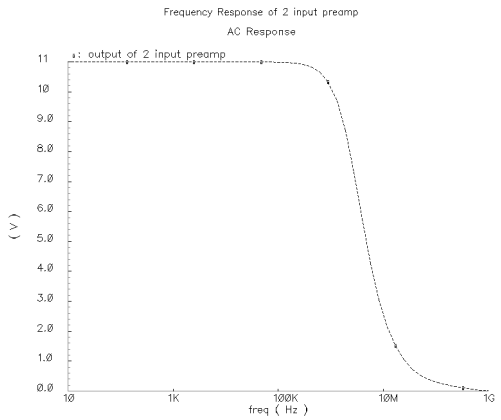


Figure II.4 The layout of the 4 input folded cascode opamp. The A.C response of the difference amplifier of gain 11, implemented with the opamp.

Library Name: /afs/ece.cmu.edu/usr/hasnain/cadence/April00

Cell Name: biasnw (Figure II.3)

Views: layout, schematic, extracted, symbol

Purpose:

This circuit provides constant-gm bias circuit over the full temperature range. This circuit has been designed to be used in conjunction with the 2 input and single input foldedcascode opamp.

Two Input Operation Amplifier

Library Name: /afs/ece.cmu.edu/usr/hasnain/cadence/April00

Cell Name: foldedcascode2 (Figure II.4)

Views: layout, schematic, extracted, symbol

Purpose:

This is an opamp with 2 fully differential inputs.This is used as a preamplifier or a single ended to double ended converter.

Test Deck Information

Test cell for foldedcascode2: the 2 input opamp

Library Name: /afs/ece.cmu.edu/usr/hasnain/cadence/April00

Cell Name: foldedcascode2_sim

Views: config, schematic

Purpose:

The nominal gain of the circuit = 11, gain = 11, f3db = 2Mhz

II.3 P.C Board circuit layout

The printed circuit board used for the testing of the z-axis accelerometer was designed using the PCB design software, Protel (http://www.protel.com). The off-chip circuits consisted of power conditioning circuits that generated a clean 5V and 12V power supply, and voltage references namely, V_{refp}, V_{refn}, V_{cm}, (analog ground), and V_{ft} (charge injection compensation). The D.C capacitance mismatch is compensated by variation of a 100kΩ resistance. The schematics for the power supply section of the PCB are shown in Figure II.5. The modulation frequency is set by a timer circuit based on the venerable LM555. The duty cycle of the output clock determines the time for which clocks ph1 and ph3 remain high. The input clock frequency is twice the modulation frequency. The details of the schematics are shown in Figure II.6. The demodulated output is low pass filtered to extract the D.C. bias and the A.C. acceleration sensitivity of the device. The signal conditioning circuit used in shown in Figure II.7. The files related to the PCB design are included on the enclosed CDROM.

II.4 Constant Resistance Circuit For Temperature Control

A temperature control circuit was designed using a single digital to analog converter integrated circuit (DAC0800), available from National Instruments (http://www.national.com/ds/DA/DAC0800.pdf). The schematic of the IC is shown in Figure II.9. A digital input to the IC determines the current ratio between the reference and the output currents. This was exploited to implement the circuit in Figure 5.17. The operational amplifier included on the chip was used for the comparison. The circuit implementation is seen in Figure II.10. The initial value of the reference resistor is set as twice the resistance of the polysilicon heater resistor. This is achieved at

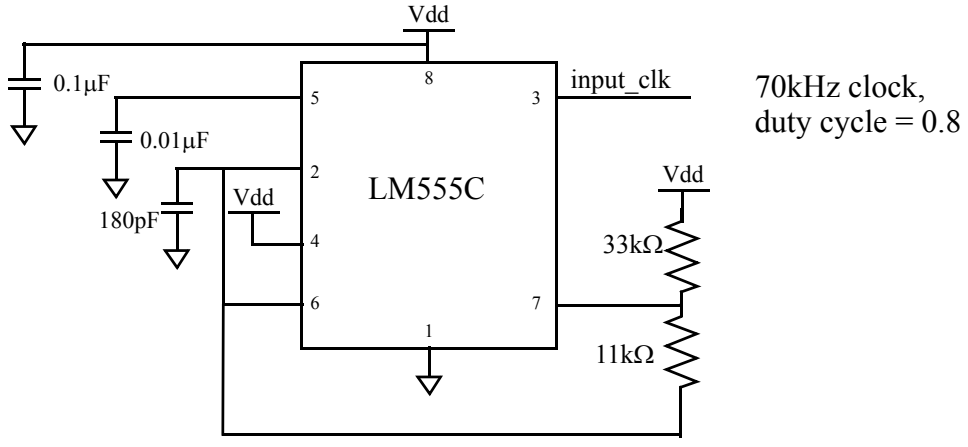


Figure II.6 The clock generation circuit designed using the 555 timer chip has a duty cycle of 0.8. The duty cycle determines the time of phase 1 and phase 3.

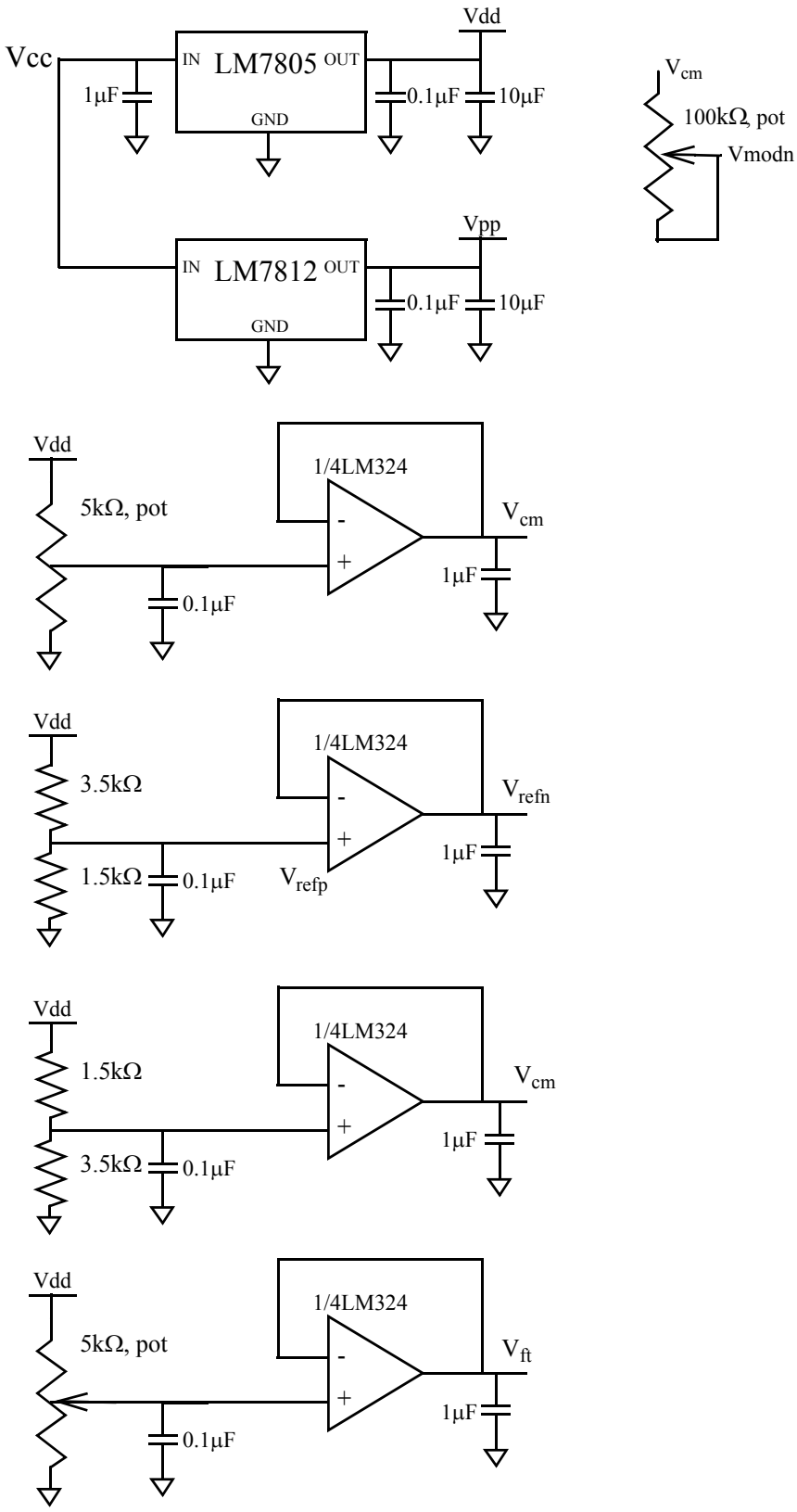


Figure II.5 Power supply conditioning circuits included on the P.C. board, along with the reference voltage generation buffers. The offset trim resistor is also included.

startup using a potentiometer. The potentiometer is tweaked till an output voltage as close to 0V can be obtained. At that point the 2 resistors are matched. It is assumed that current flow in the potentiometer does not change its resistance, and the TCR of the potentiometer is zero. Setting a digital word will set the temperature of the polysilicon resistor. At steady state, the input voltages of the opamp are equal.

$$\beta I_o R_{ref} = I_o R_{poly,\,To}(1 + \alpha_{poly}\Delta T) \tag{II.1}$$

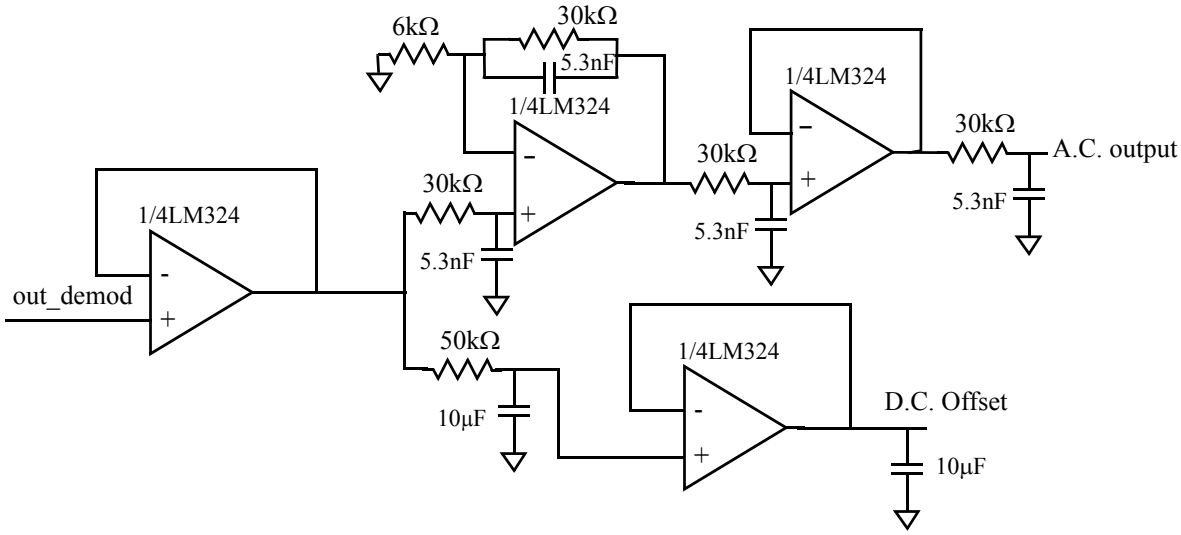


Figure II.7 Signal conditioning circuit used to low pass filter the modulated output from the chip to extract the D.C. offset and A.C. sensitivity to the external acceleration and temperature change. The demodulated output of the circuit is separated in to a D.C component to measure the D.C. offset of the measured acceleration, and the A.C component used to characterize the sensitivity of the accelerometer.

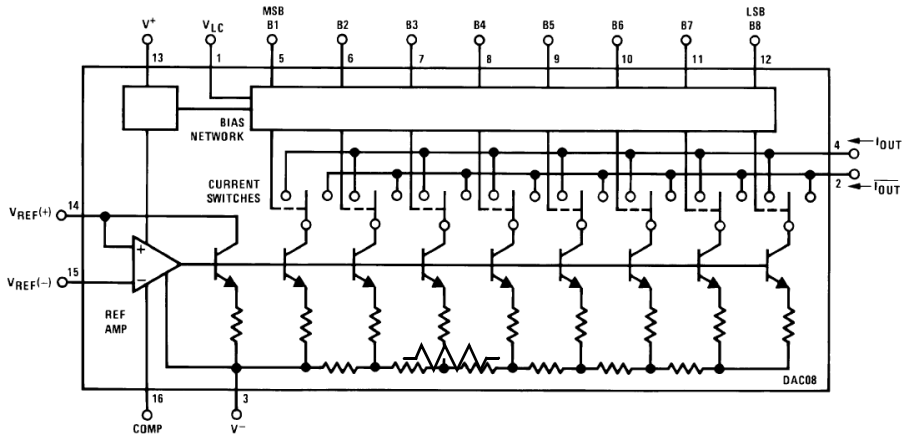


Figure II.9 Schematic of the digital to analog converter IC, DAC0800, available from National Semiconductors.

where, $R_{poly,To}$ is the polysilicon resistance at room temperature, T_o, α_{poly} is the TCR of polysilicon, β is the current ratio, and ΔT is in the increase in temperature. The value of R_{ref} has been set as

$$R_{ref} = 2R_{poly,\,To} \tag{II.2}$$

and, the current ratio is set by the digital word as

$$\beta = \frac{128 + D_{in}}{255} \tag{II.3}$$

where, D_{in} is the seven bit digital input word that sets the temperature. The temperature increase can the be expressed as

$$\Delta T = \frac{D_{in}}{255\alpha_{poly}} \tag{II.4}$$

For, α_{poly}=5.5 x 10^{-3}/K, the maximum temperature increase is 90.5°C, with a resolution of 0.7°C. For an increased temperature range a current amplifier can be used to increase the current ratio β. This circuit based approach was not utilized in the final temperature control scheme demonstration, as a design exploration experiment is difficult to perform using this scheme.

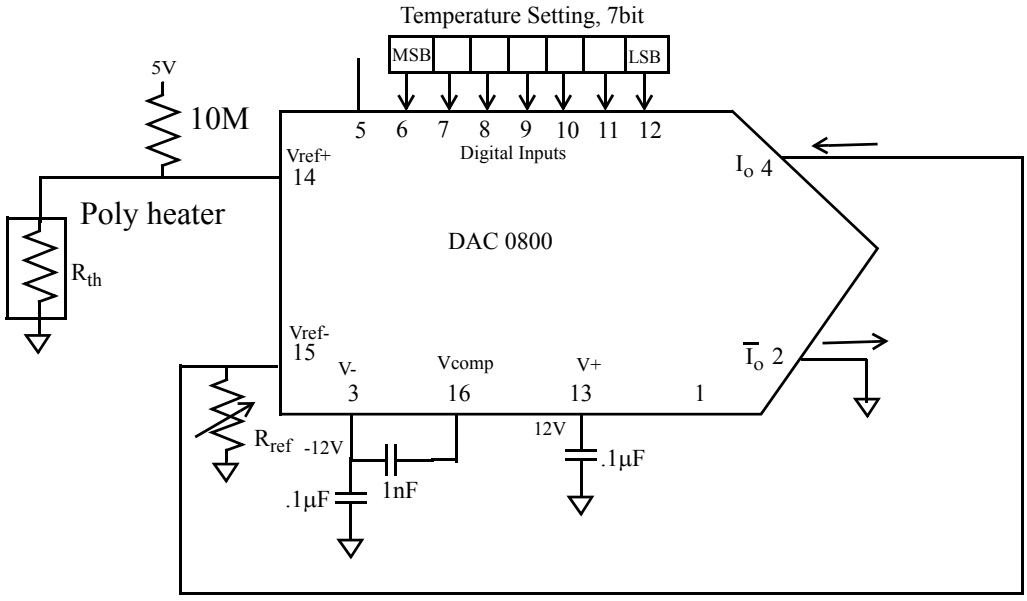


Figure II.10 Schematic of the digital temperature controller implemented using a single DAC chip

II.5 Design of the Temperature Control Software In Labview

The temperature control of the z-axis accelerometer was implemented in Labview. The software temperature control was implement by a binary search type of algorithm that changed the voltage applied using the Keithley source measurement, to keep the device resistance constant. The Labview code used for the controller has been included on the enclosed CDROM.