

## FPGA Platform-based Investigation of Structured LDPC Codes on Realistic Perpendicular Magnetic Recording Channels

Prof. Vijayakumar Bhagavatula,  
Data Storage Systems Center (DSSC)  
Carnegie Mellon University, Pittsburgh, PA, USA

Low density parity check (LDPC) codes are considered good candidates for very high density data storage systems because of their superior bit error rate (BER) performance over conventional channels in most PC-based simulations. However, PC-based simulations are too slow to attain very low BERs (around  $10^{-10}$  and lower). Over the past several years, we have been developing a field programmable gate array (FPGA) platform for LDPC code evaluations. Initially, we used a Lorentzian pulse response model for the longitudinal magnetic recording channel model with additive white Gaussian noise (AWGN), but recently, we have begun to include more realistic magnetic recording channel impairments (e.g., nonlinear transition shift, partial erasure, transition noise, etc.) in addition to AWGN. Our objective is to investigate various structured LDPC codes for their error floors and error distributions (in order to assess their compatibility with any outer error correcting codes) in the presence of realistic channel impairments in perpendicular magnetic recording and other data storage systems (e.g., optical recording, holographic data storage).

Over the past few years, we have been developing an FPGA platform [1, 2] for analyzing LDPC codes. Since the LDPC decoders need as their input soft information rather than hard information, we needed to implement the Soft Output Viterbi Algorithm (SOVA) in place of the conventional hard Viterbi Algorithm (VA). We also needed to implement the white Gaussian noise generator in FPGA hardware since we do not want the PC-based noise generation to be the bottleneck in the high-speed implementation. Our FPGA system includes a PC (with MATLAB, C and a PCI port), and an FPGA board with Xilinx Vertex II 6000 on it. Using this fully-parameterized general decoding module, we have been able to evaluate the BER of different types of structured LDPC codes (e.g., disjoint difference set or DDS LDPC codes, permutation geometry or array codes) as well Turbo Product Codes based on Single Parity Check (TPC/SPC) codes. We analyzed the BER for these codes when the underlying noise is additive white Gaussian noise (AWGN). Most of our evaluations were for structured LDPC codes of column weights 3, 4 and 5 and codeword length around 4600 bits with a code rate of 8/9. We are able to achieve BERs as low as  $10^{-12}$  using the FPGA platform. Such extremely low BERs are unthinkable in software simulations. Since we require about 100 errors before declaring a BER, this corresponds to simulating  $10^{14}$  bits. We have also investigated [3,4] error distributions from TPC/SPC codes and have observed that TPC/SPC codes do not offer noticeable performance gains over an outer Reed-Solomon code when we impose practical constraints such as no more than 2 channel iterations and no interleaving among TPC/SPC codewords.

Recently, we have extended our FPGA platform in the following ways.

- An FPGA implementation of transition noise (i.e., pulse width variation and peak shifts) simulator,
- An FPGA module to simulate nonlinear transition shift (NLTS),
- An FPGA module to simulate partial erasure,
- An FPGA module to estimate error distributions, not just error counts, and
- An FPGA implementation of a 11-tap equalizer to achieve the EPR4 target instead of assuming ideal EPR4 samples corrupted by AWGN.

Our preliminary investigations of LDPC codes with these more realistic impairments suggest that the performance of some of these codes may degrade significantly by these noise sources. This is a cause for concern and we will need a more systematic evaluation of the LDPC coded channels. Also, many of the LDPC codes evaluated (DDS codes and array codes) exhibit error floors above BERs of around  $10^{-10}$  which

suggests that finding good LDPC codes may be harder than previously envisioned. However, we observed that the progressive edge growth (PEG) quasi-cyclic LDPC codes [5] did not exhibit an error floor down to  $10^{-10}$  type BERs.

We are currently extending our FPGA platform to include partial response (PR) targets beyond EPR4 and impairments appropriate for perpendicular recording. Our FPGA platform is an excellent vehicle for careful investigation of various LDPC and LDPC-like codes for extremely high density recording. Given the improved capabilities of our FPGA platform, we are planning to investigate the following issues.

- Extension of FPGA platform to include partial response (PR) targets beyond EPR4.
- Extension of the readback signal generator in the FPGA platform to include perpendicular recording signals along with impairments observed in perpendicular recording.
- Systematic evaluation of different structured LDPC code types (DDS codes, array codes, TPC/SPC codes, PEG QC LDPC codes) for different code rates (8/9 and larger), different codeword lengths (4608 bits and longer), different levels of AWGN and different amounts of noise impairments. BERs, frame error rates (FERs) and error distributions will be acquired with the goal of analyzing the benefits/need of any outer error correcting codes.
- Sensitivity studies of the performance degradation as we go from AWGN channels to ideal PR + AWGN to real-world PR + AWGN to real-world PR with realistic signal impairments.

## References

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