EMT 2009 Call for Papers

Workshop on Emerging Memory Technologies

Austin, TX, June 21, 2009

Held in conjunction with the 36th annual International Symposium on Computer Architecture (ISCA-36)

Overview: In the near future, architects and system designers will be faced with a much wider array of memory technology choices for on-die cache, main memory, and backing storage than the conventional technologies we have relied on for decades (i.e. SRAM, DRAM, and hard disk drives). As process technologies scale down to the nanometer-regime, the characteristics and reliability of SRAM and DRAM are changing significantly. Further, improvements in the speed, density, power, and cost of FLASH memory, as well as its non-volatility, have made it a viable replacement for more conventional memories across the storage hierarchy. Solid-state drives (SSDs) are gaining significant momentum as HDD replacements, and FLASH has been suggested as a replacement for DRAM main memory and even on-die SRAM for some applications. Additionally, there are a number of emerging memory cell technologies (e.g. phase change, MRAM, nanotube, molecular) that show the potential to combine the speed of SRAM, with the density of DRAM, and the non-volatility of FLASH to become a future "universal" memory technology. Given the widening array of memory technology choices, architects and system designers must have a strong grasp of the current state-of-the-art as well as future developments in order to plan and design optimal systems. By optimally exploiting these new memory technologies, we can significantly improve the performance and efficiency of future computing systems.

Topics of Interest: Contributions on all aspects of emerging memory technology are encouraged. The topics of primary interest include (but are not limited to):

- Architectures and systems utilizing emerging memory technologies
- Architectures and systems utilizing conventional memory technologies in novel ways
- Evaluation and modeling of emerging memory technologies for higher-level design
- Methods for extending conventional memory technologies to nano-scale processes
- Comparisons of emerging and conventional memory technologies in future processes

Paper Submission: Authors are requested to submit extended abstracts in PDF format not exceeding 10 pages (8.5x11 inches) that include abstract, five key words, contact address, figures, and references. Please submit your extended abstracts via email to **kenmai@ece.cmu.edu** by **May 8th, 2009**.

Organizers:

Ken Mai (Carnegie Mellon University)
Guyeon Wei (Harvard University)
Ben Lee (Microsoft Research)

Please address all questions to Ken Mai (kenmai@ece.cmu.edu).