Introduction to Nanotechnology & Nanoelectronics

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ECE 18-200
Nov 10, 2005

Some facts:

Nanoscience and nanotechnology are "hot". It is one of the most-talked about topics among scientific and engineering communities. Government agencies and industry are investing ~ $2 billion per year directly on nanotechnology.

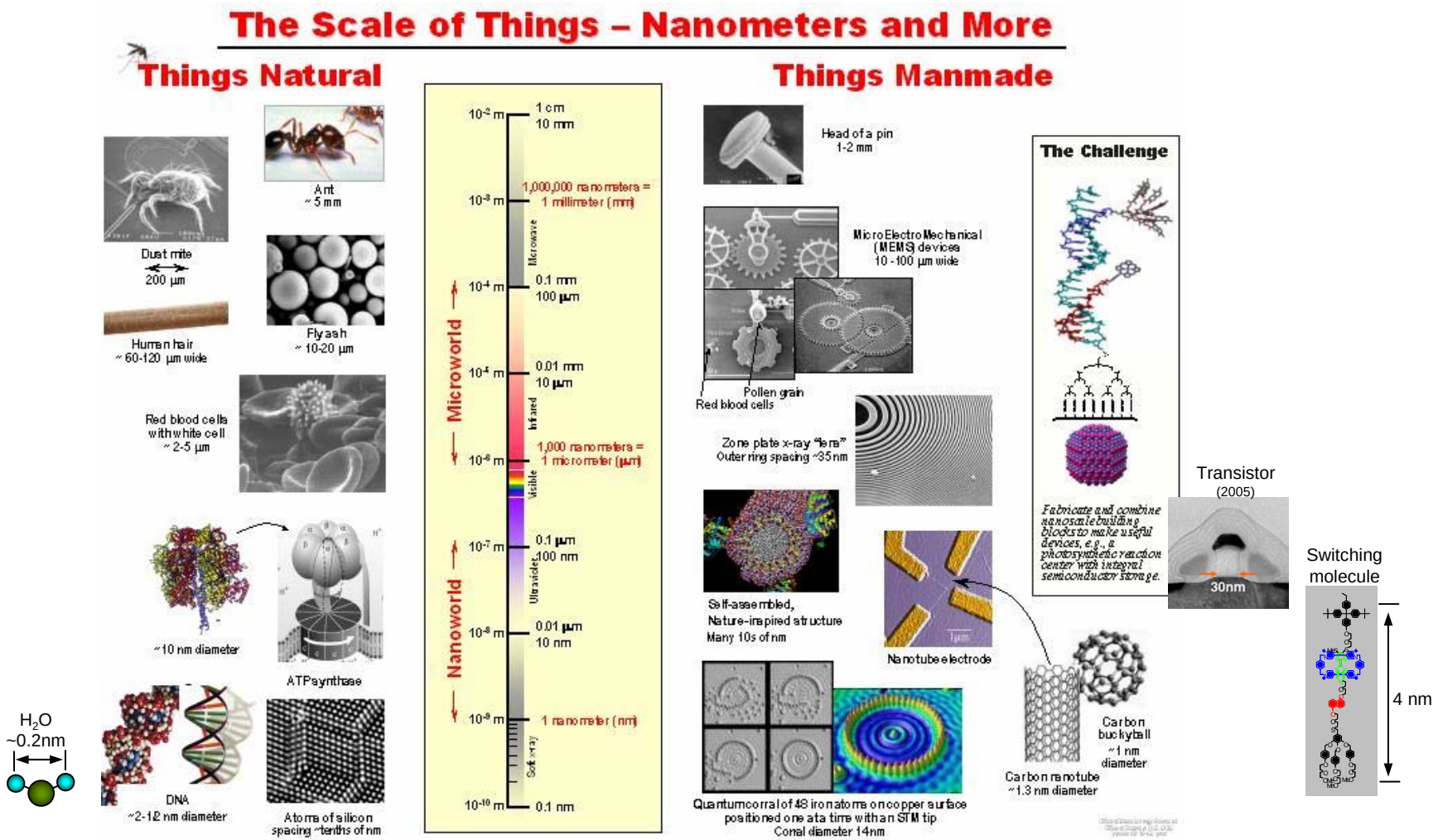
What is "Nanotechnology" ?

Nanotechnology is the understanding and control of matter at dimensions of roughly 1 to 100 nanometers, where unique phenomena enable novel applications. Encompassing nanoscale science, engineering and technology, nanotechnology involves imaging, measuring, modeling, fabricating, synthesizing and manipulating matter at this length scale.

Which area is it involved ?

Many scientific disciplines, e.g. physics, chemistry, biology, medicine, and materials etc., and almost all engineering fields. It expands over many industrial areas such as electronic, health care, chemical, so on and so forth.

Can you name any nanotechnology or anything made with nanotechnology ?



nucleus of hydrogen (proton)
~ 0.000001 nm

← 1 fm = 10^{-15} m

Source: National Nanotechnology Initiative

Is “nano” special in nature?

Probably not.

… kilo-, meter, milli-, micro-, nano-, pico-, femto-, atto-…

Why nanotechnology is getting popular now?

1. now we are able to image, make, and manipulate materials on this scale;

2. there are needs and applications in the real world (justified by the costs).

Two major distinct approaches build to nanoscale systems :

1. the more traditional approach:
   "top-down" – starting from bulk materials to fabricate nanostructures via patterning, etching, and deposition, etc.; more physical flavored. Best represented by CMOS technology.

2. the novel approach:
   "bottom up" – starting from basic elements to synthesize and assemble more complicated nanostructures; more chemical flavored. Nanocrystal, carbon nanotube, supramolecule, etc.

For the rest of the lecture, we are discuss nanotechnology based on these two approaches.

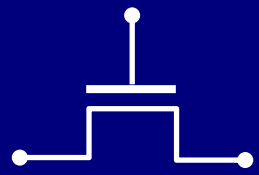
Top-down Approach

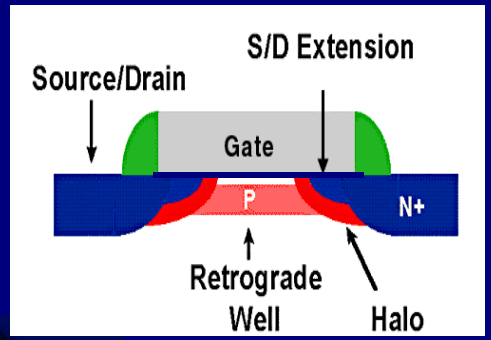
(best represented by CMOS fabrication)

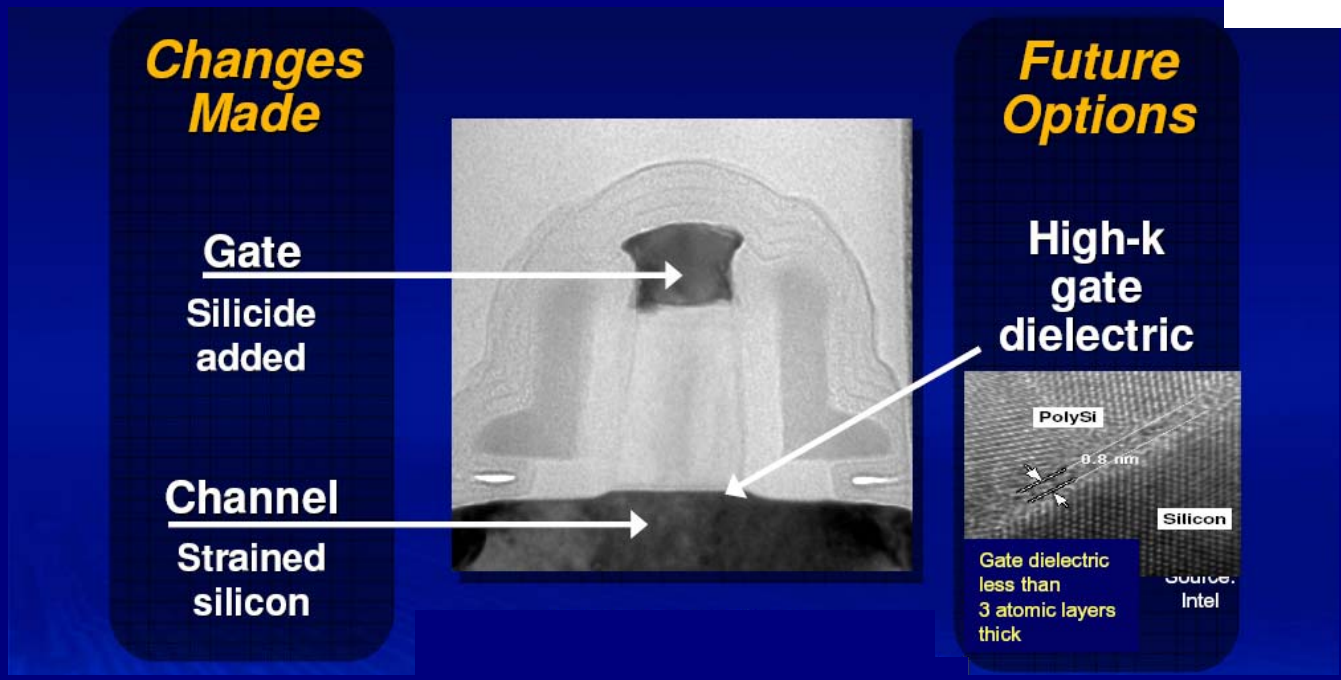
A close look of FET

(field effect transistor)

Source: Intel







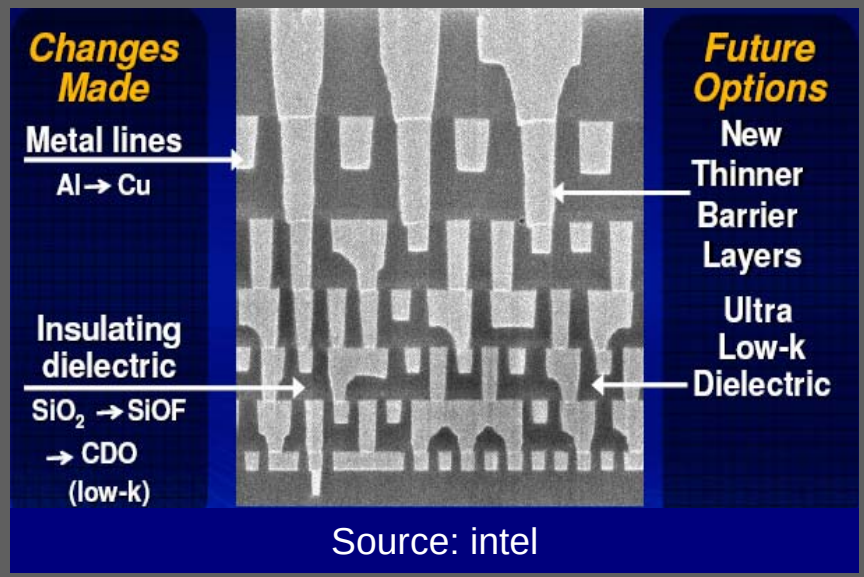
The challenge is to make a billion of them on a chip.

There are over 200 processing steps in CMOS IC fabrications.

To name a few:

patterning
etching
metalization
implantation
deposition
cleaning
CMP
annealing
wafer bonding
packaging

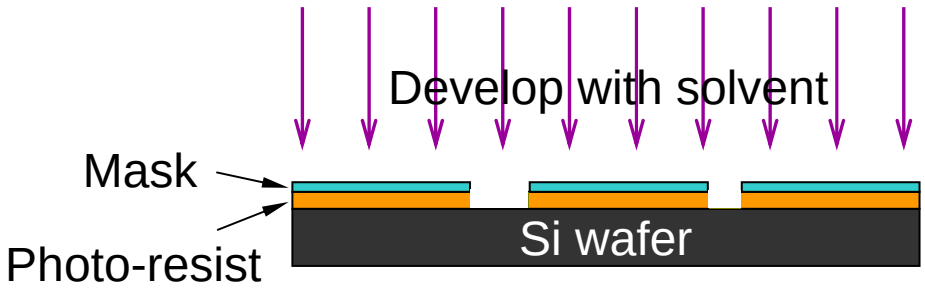
.
.
.



This time we will only talk about how to make small things.

Optical Lithography -sub micron technology

SUSS MA6



SUSS MA200/300PLUS

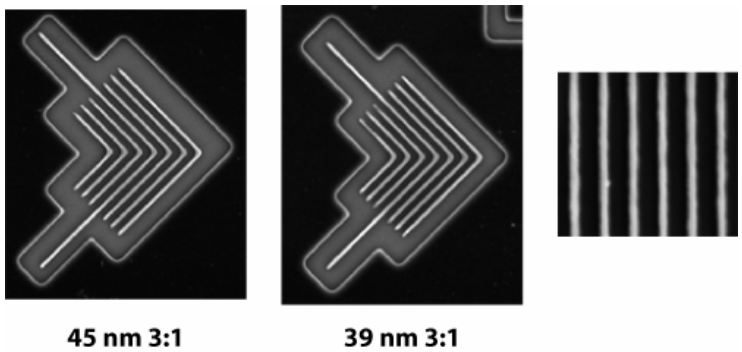
Advantage – very mature, fast, parallel processing.

Limits – relatively large feature sizes, mask can be very expansive.

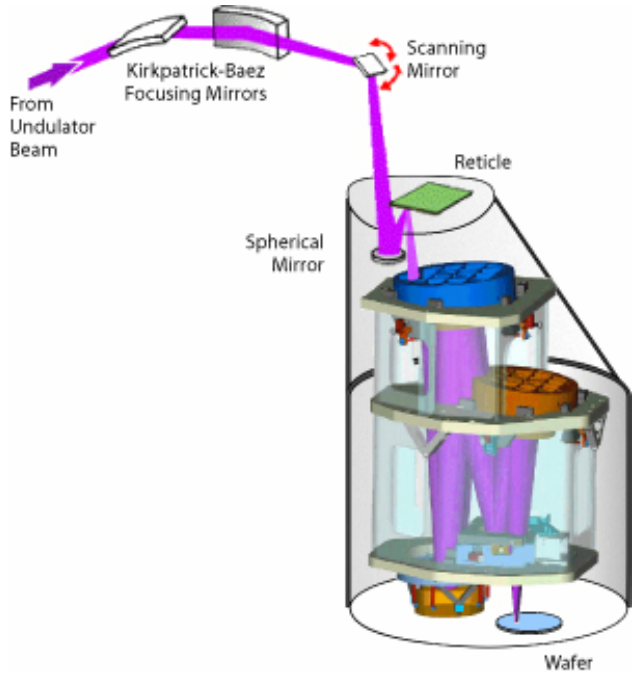
EUV Lithography

-Deep sub-micron technology

-10's to ~100 eV incident light



EUV system at ALS in LBL

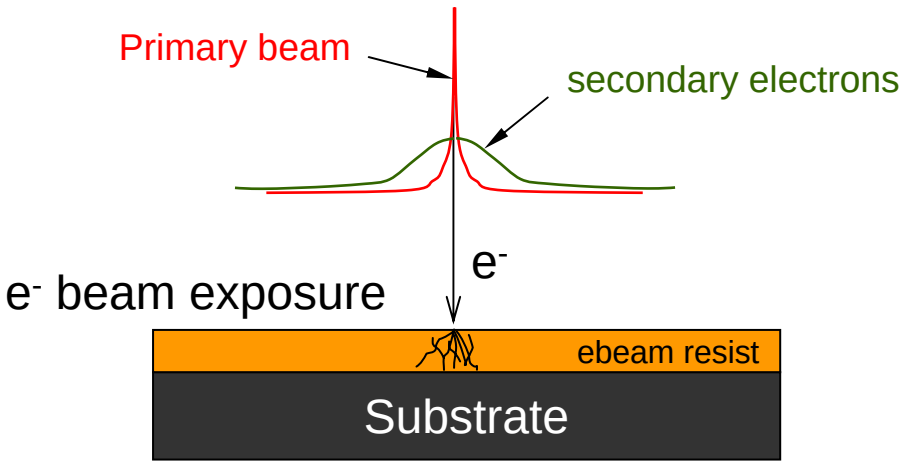


How it works:
The scanning mirror directs focused EUV light from the Kirkpatrick-Baez mirrors into the converted interferometer with the desired degree of spatial coherence and illumination pattern. Installed inside the interferometer tank, the Set-2 optic images the EUV light reflected from the mask-carrying reticle onto a resist-covered silicon wafer.

Advantage –small patterns, can be reasonably fast;
Limits – can be very expensive.

Electron Beam Lithography

High energy electrons (30-200 KeV) have much shorter wavelength (~ pm). Beam size can be sub-nanometer.

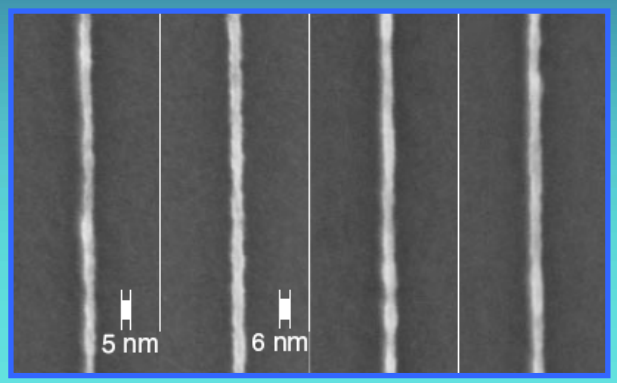


post-development

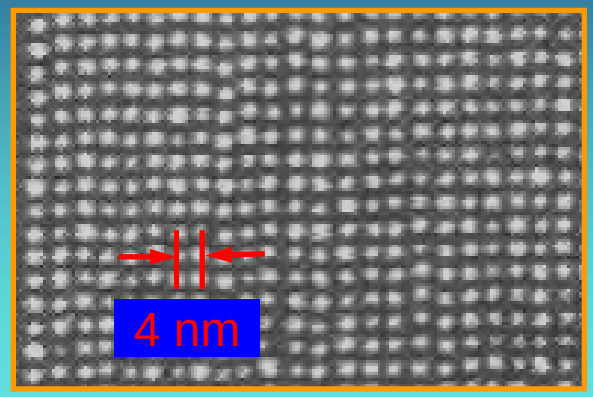
Quanta 600 FEG (FEI Company)

JBX-9300FS Electron Beam Lithography System

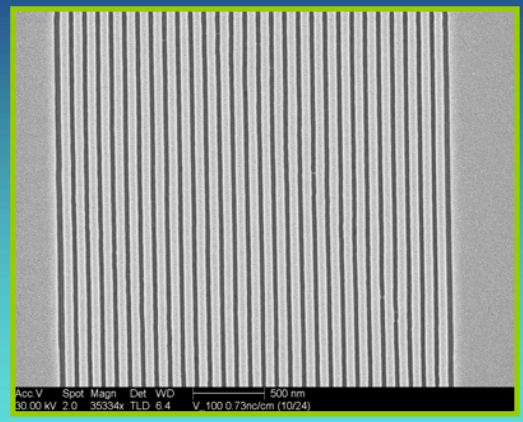
Electron Beam Lithography

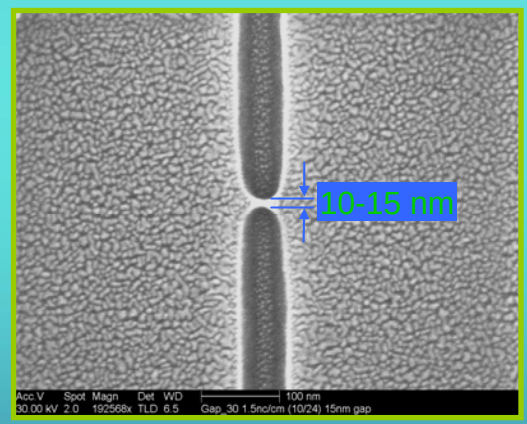


K. Yamazaki and H. Namatsu, *Jpn J. Appl Phys,*Vol 43, 6B, 3767 (2004).



Muray, Isaacson, and Adesida, *Appl. Phys. Lett.,* Vol 45, 589 (1984).





Done here at CMU !

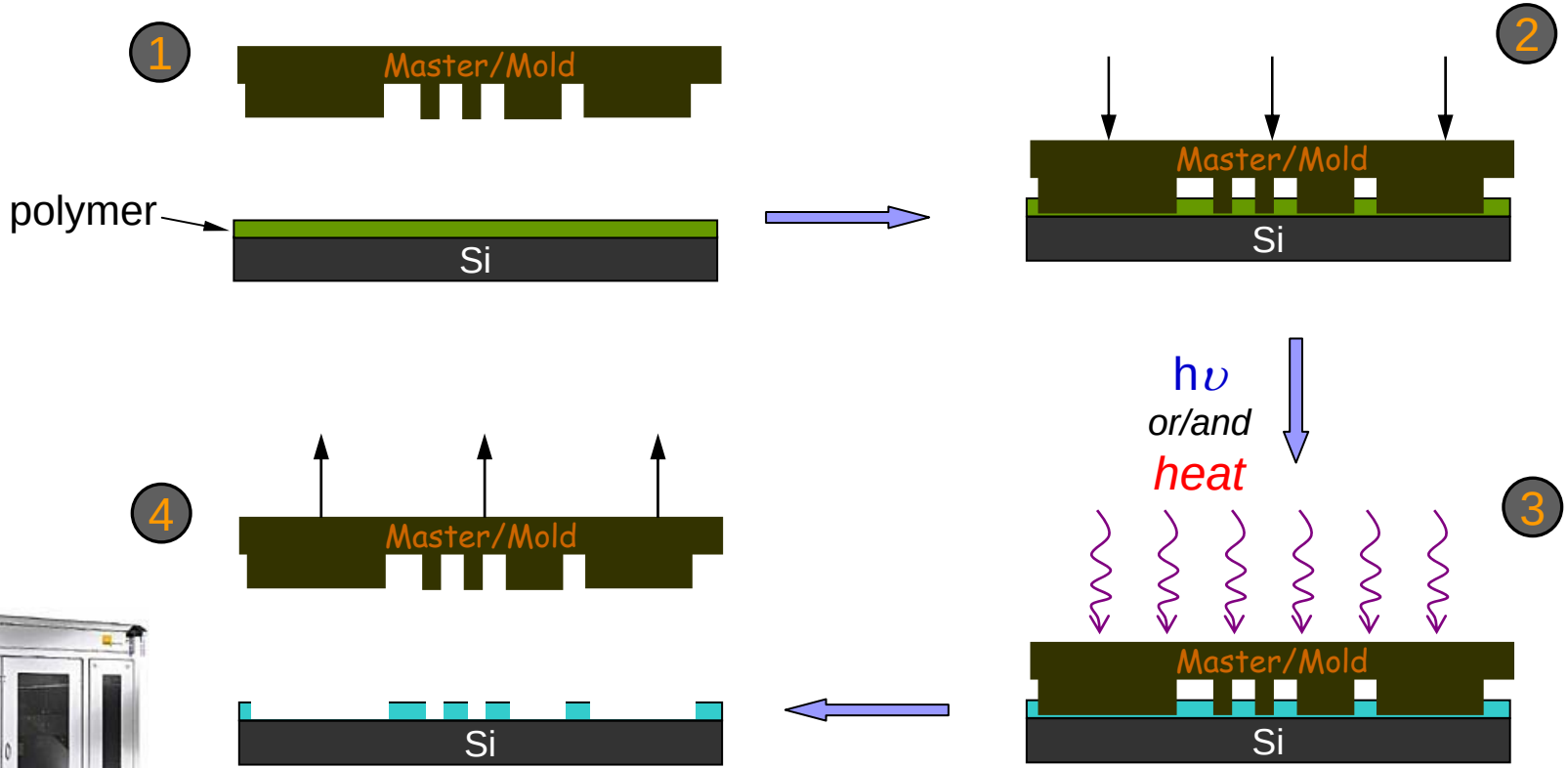
Wavelength is not an issue. Beam size can be sub-nanometer.

Advantage – small arbitrary patterns, no mask is needed.
Limits – serial process, slow.

Nano-Imprint Lithography

A schematics introduction

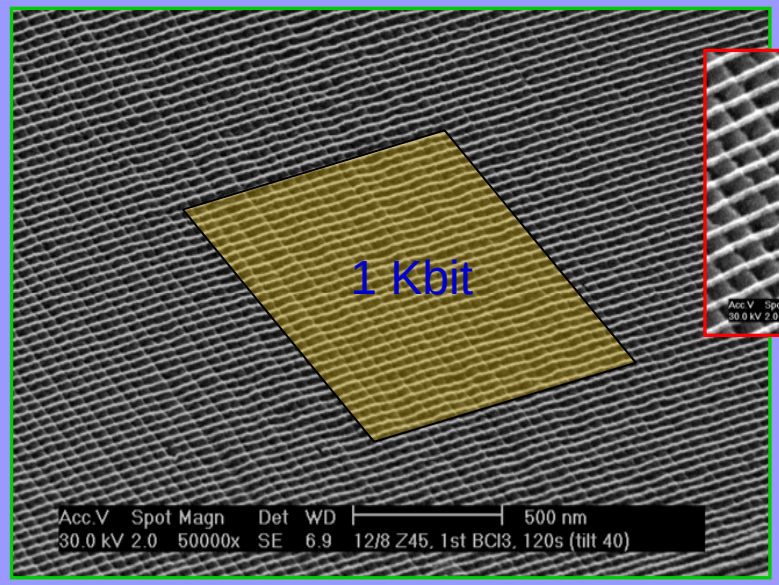
SB6e - Suss

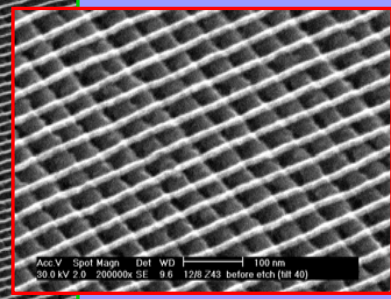


NPS 300 -Suss

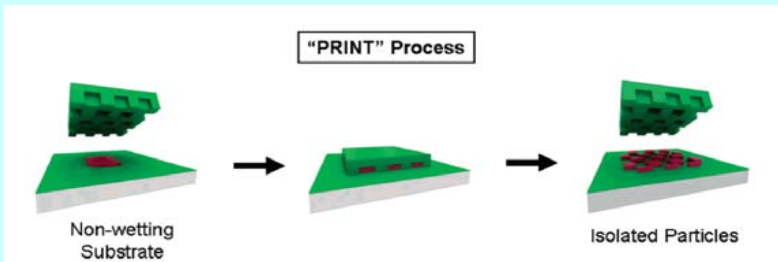
Ordered Nanowires array with extremely high density

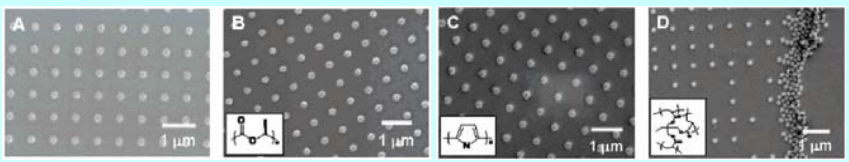
Cross-bar Memory - 10^{11}bit/cm^2



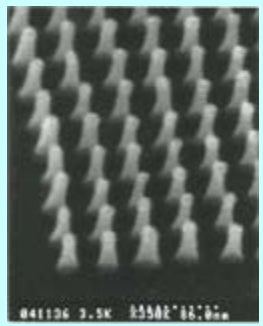


Heath Group – Caltech

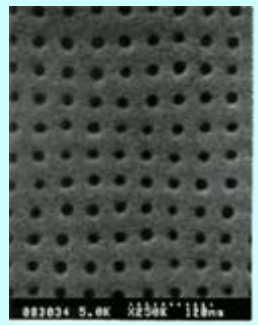




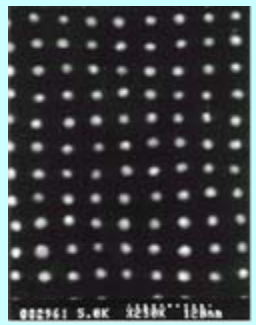
J M DeSimone Group – UNC/NCSU



Imprint mold with 10nm diameter pillars



Holes imprinted in PMMA



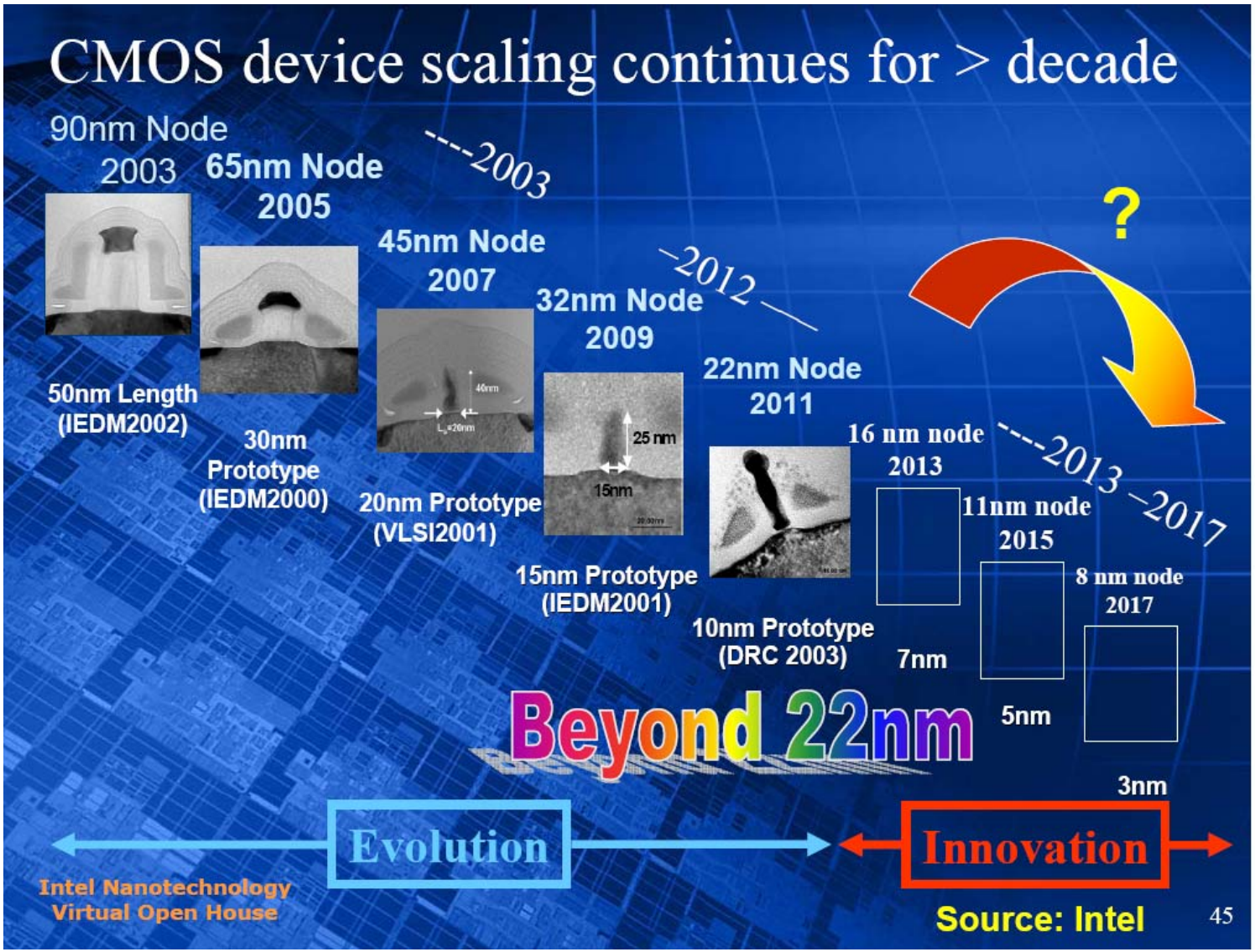
Metal dots fabricated by NIL

S.Y. Chou Group - Princeton

Techniques to make nanoscale patterns from top-down – lithography with:

UV light,
ebeam,
EUV,
X-ray,
Imprint,
etc.

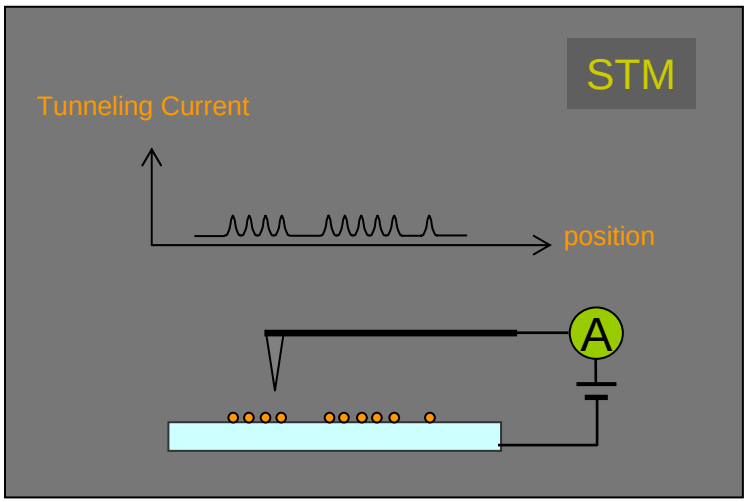
It is likely that the scaling of CMOS will continue down to 22nm node (~10nm channel length).

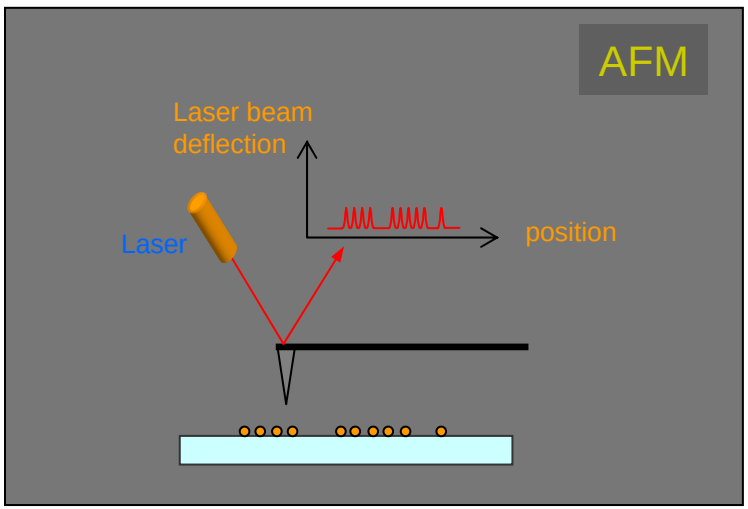

CMOS device scaling continues for > decade
90nm Node
2003
65nm Node
2005
45nm Node
2007
32nm Node
2009
22nm Node
2011
16 nm node
2013
11nm node
2015
8 nm node
2017
---2003
~2012
---2013 ~2017
?
50nm Length
(IEDM2002)
30nm
Prototype
(IEDM2000)
20nm Prototype
(VLSI2001)
15nm Prototype
(IEDM2001)
10nm Prototype
(DRC 2003)
7nm
5nm
3nm
Beyond 22nm
Evolution
Innovation
Intel Nanotechnology
Virtual Open House
Source: Intel
45

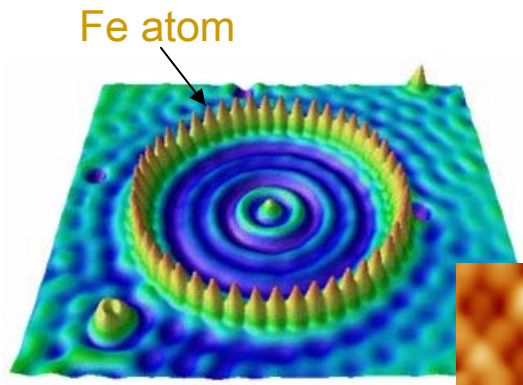
Bottom-up Approach

- SPM – imaging, and building structures atom by atom;
- Synthesis and applications of nanocrytal, nanotube, nanowire, and supramolecule;
- Self-Assembling of nano-components;
- Nanoelectronics with molecules.

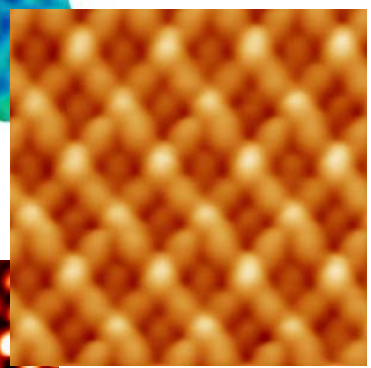
SPM – Microscopes that can "see" and move atoms



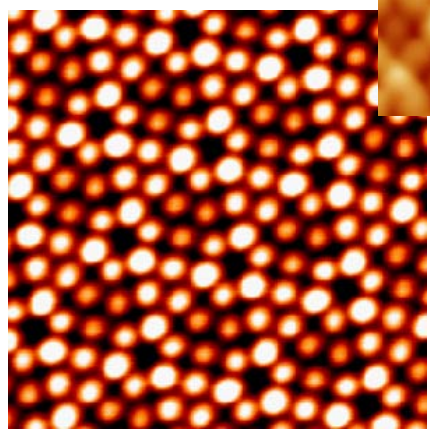




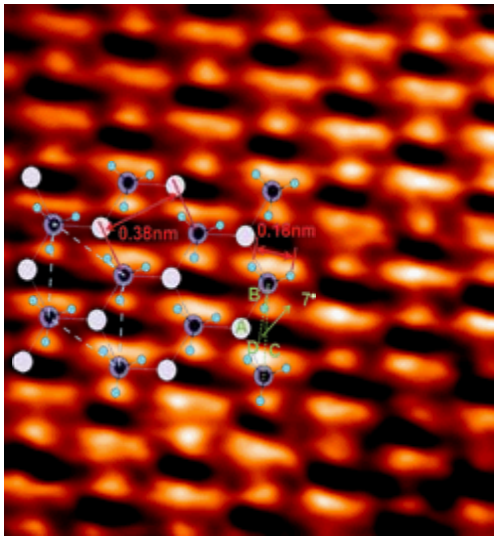
Quantum Corral
Source: IBM



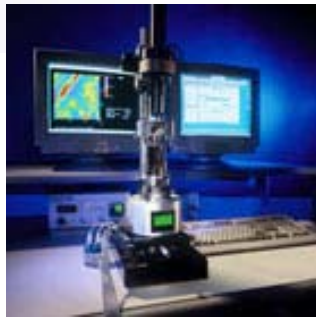
Ge/Si(105) surface
(NCAFM image)



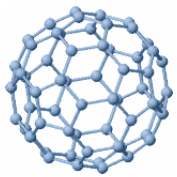
Si(111) 7x7 reconstruction surface
Source: Omicron



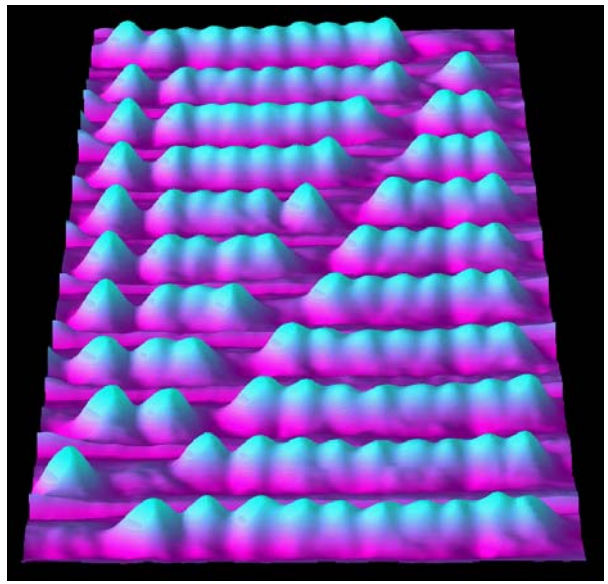
Low-temperature STM image of -CH3 on Si(111) surface. (Heath, Caltech)



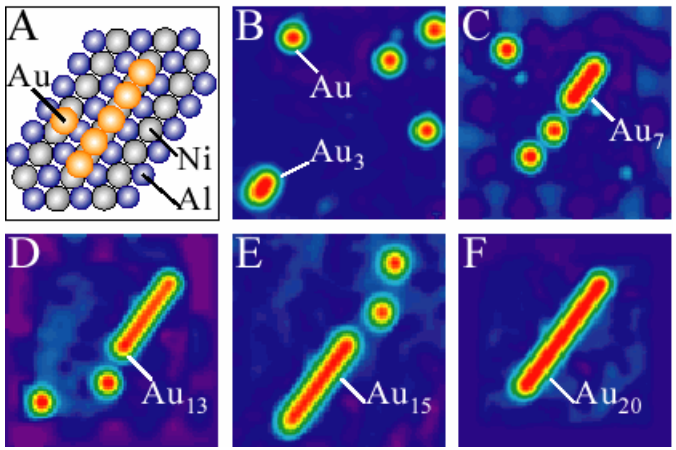
Atoms and molecules can be precisely manipulated by STM tips



C_{60} , ~ 1nm

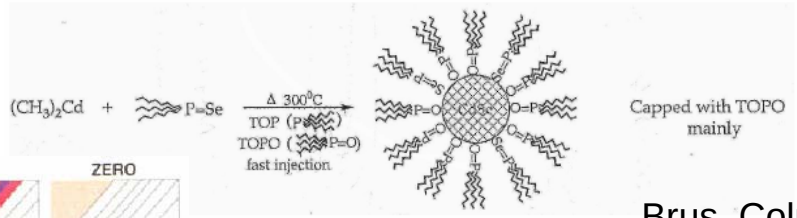


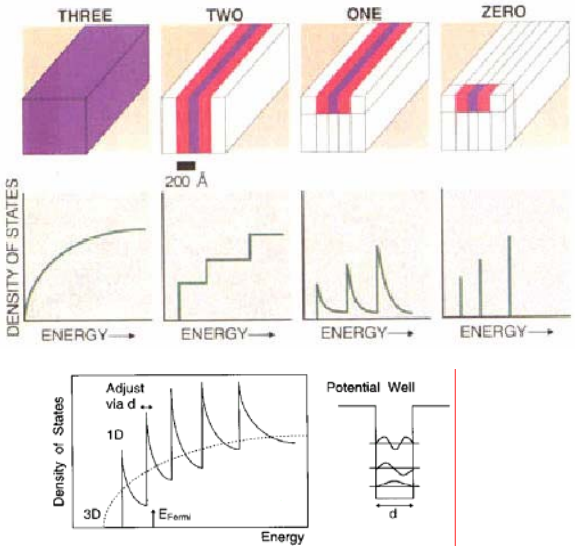
"nano-abacus" formed by C_{60} molecule along single atomic steps on copper surface. (Jim Gimzewski, UCLA)



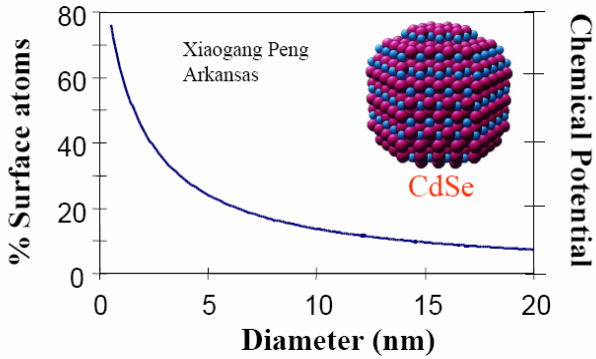
Development of One-Dimensional Band Structure in Artificial Gold Chains, W. Ho Group, UC Irvine.

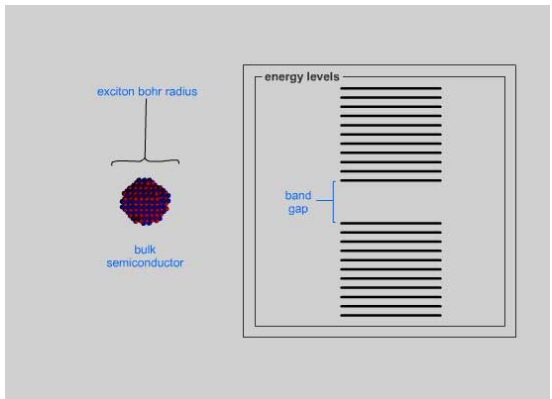
Nanocrystal / Nanoparticle

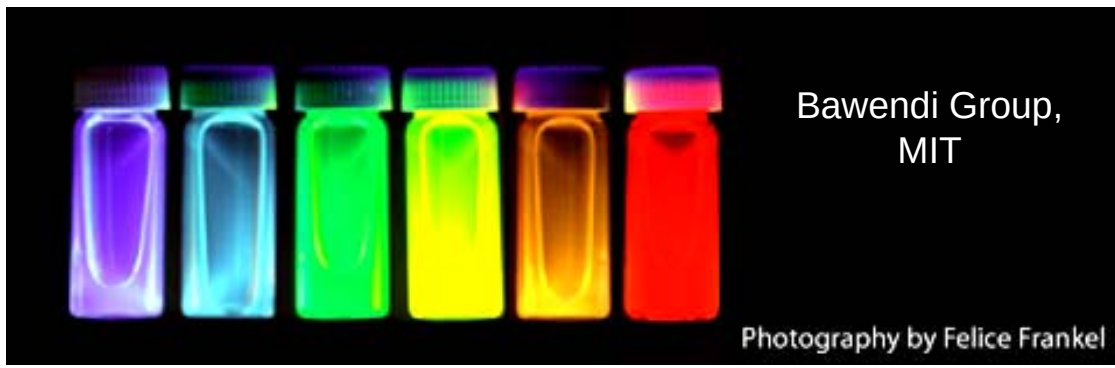




Brus, Columbia

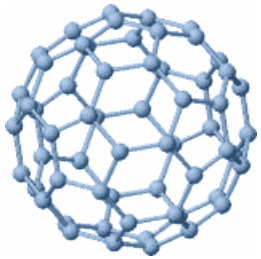




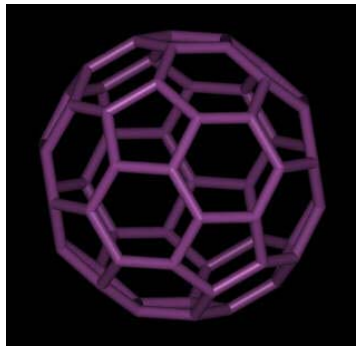


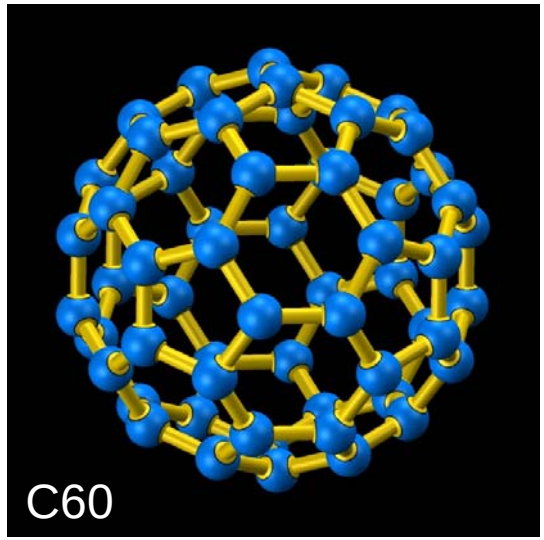
Quantum confinement - size effect

Optoelectronic applications



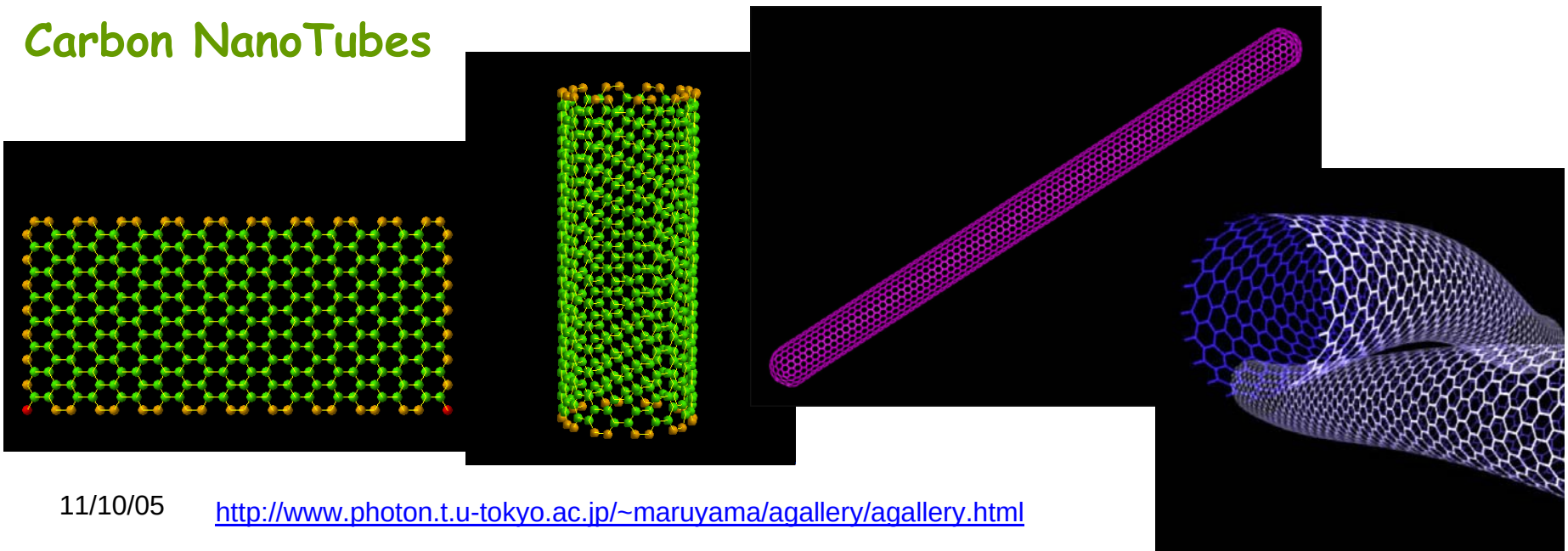
Fullerenes





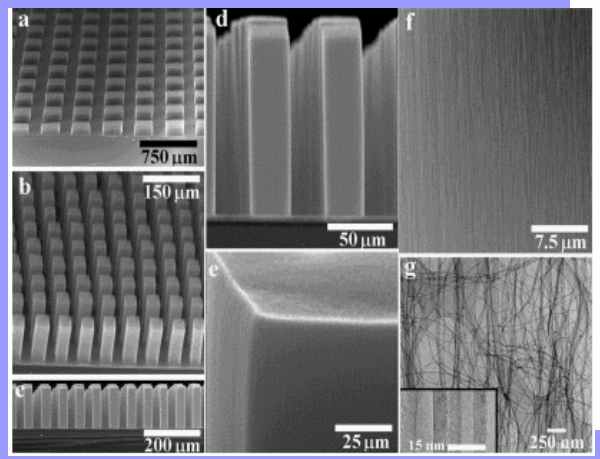
A whole family of Bucky Balls
C28, … C60, C70,… C240…

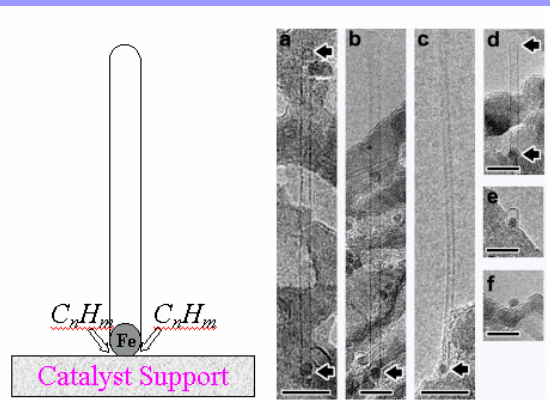
Carbon NanoTubes

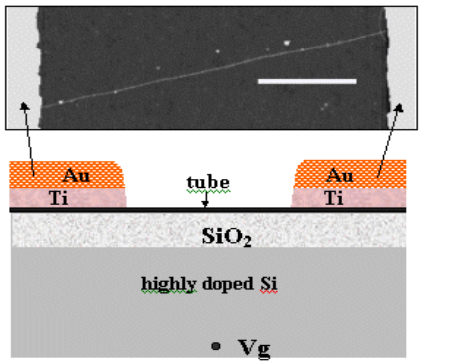


http://www.photon.t.u-tokyo.ac.jp/~maruyama/agallery/agallery.html

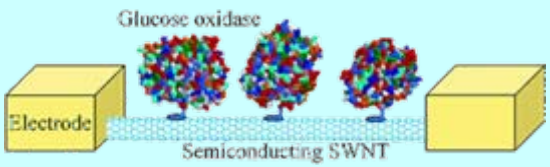
Carbon Nanotubes

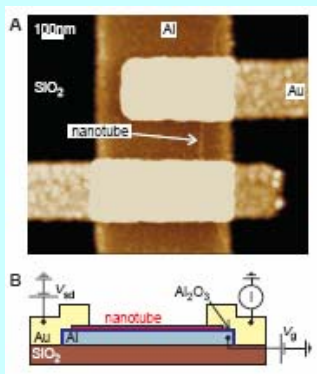


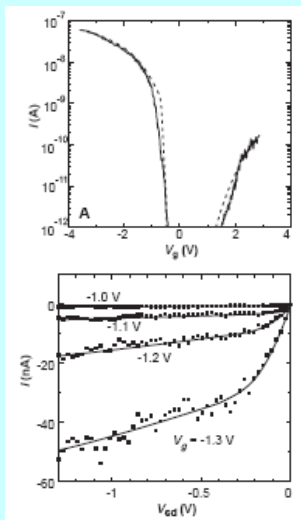


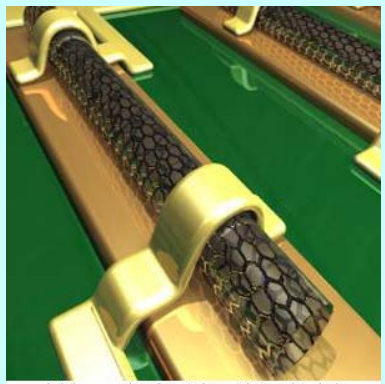


Carbon Nanotubes H. Dai Group, Stanford Univ.





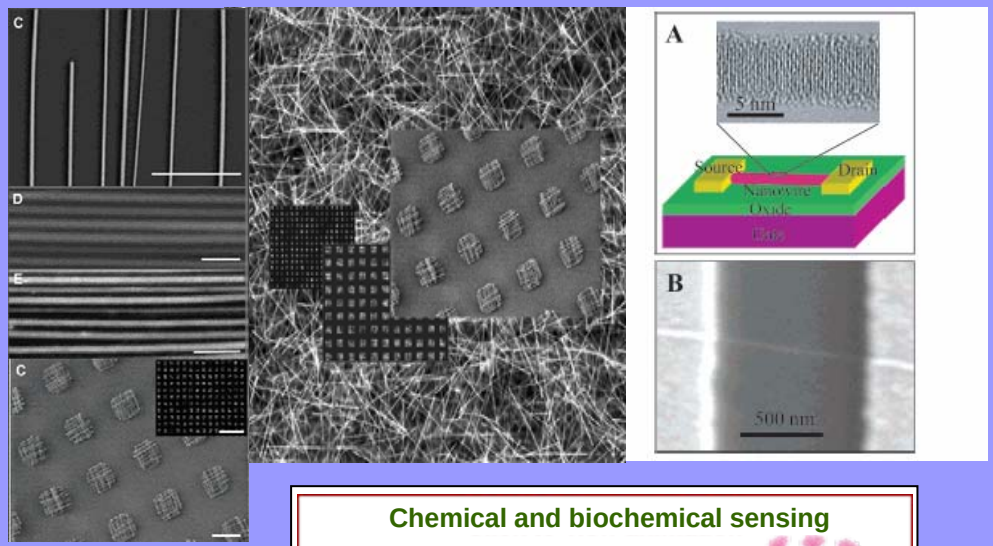


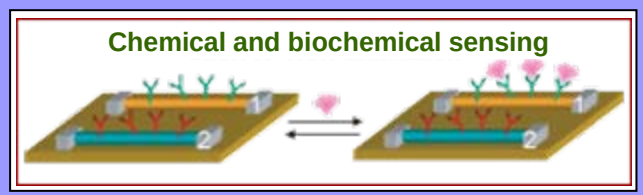


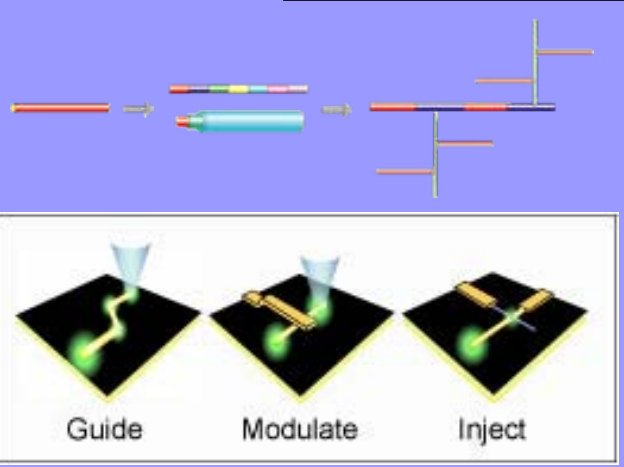
Artist's conception of a gated nanotube transistor logic circuit. Bachtold et al., *Science* **294** (2001) 1317.

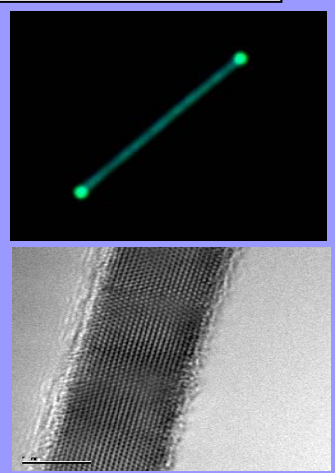
Carbon Nanotube sensor and transistor
C. Dekker Group, Delft Univ of Tech

Semiconductor Nanomaterials

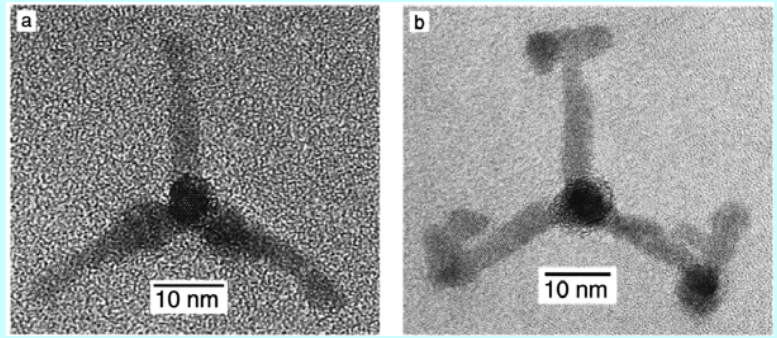




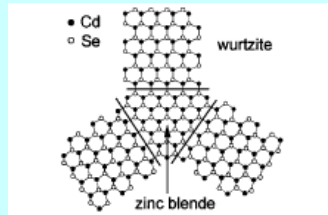


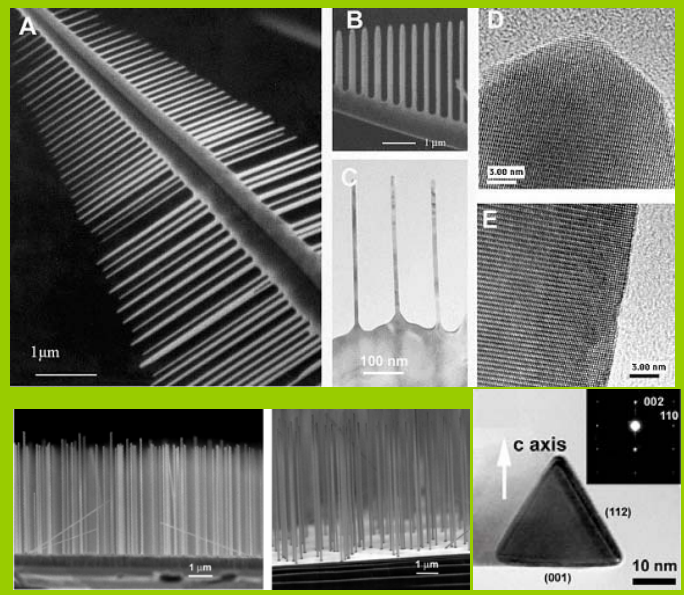


Semiconductor Nanowires, Lieber Group, Harvard



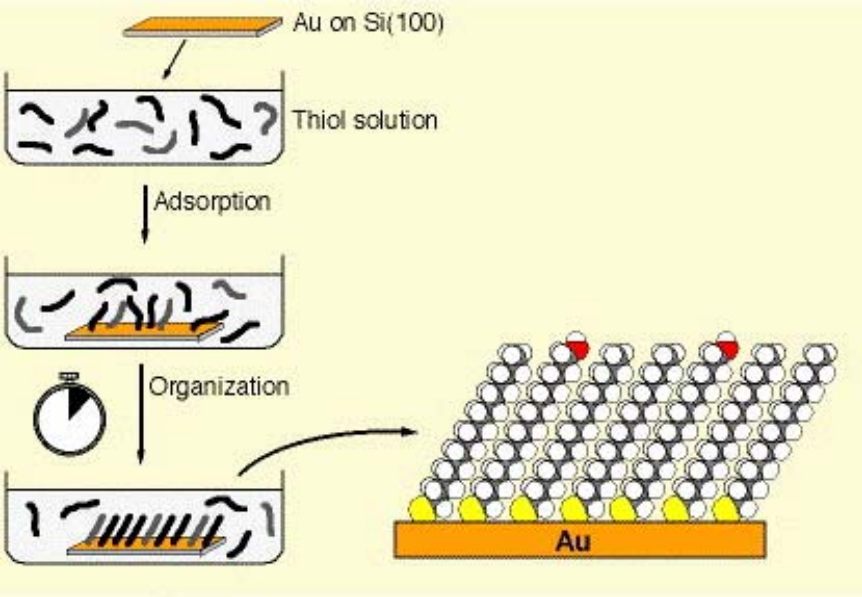
Semiconductor Tetrapod
Alivisatos Group, Berkeley



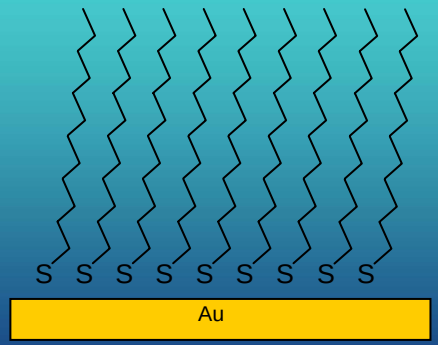


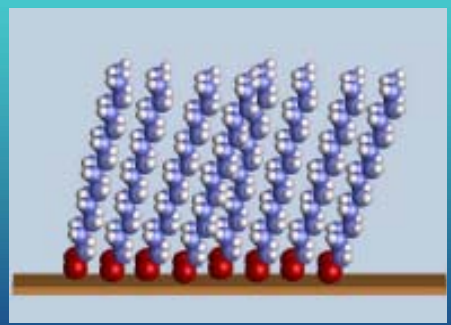
Peidong Yang Group, Berkeley

Self-Assembled Molecular Monolayer

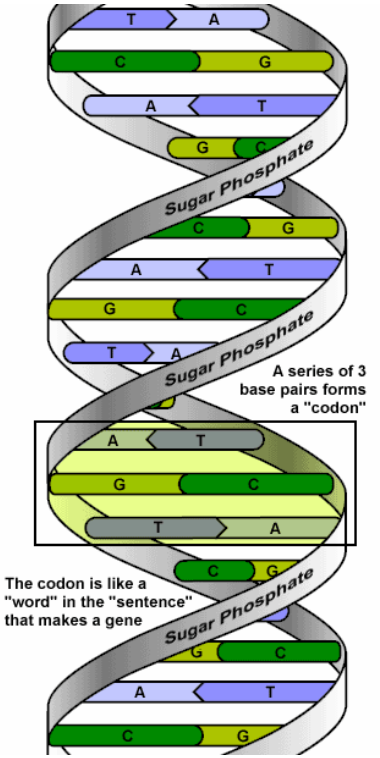


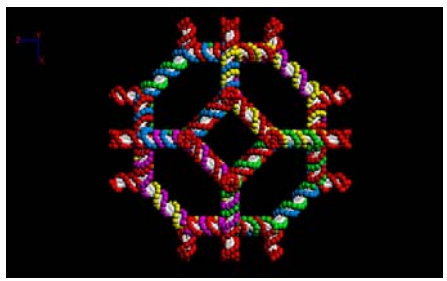
Atomic Force Microscope Image of SAM on Au

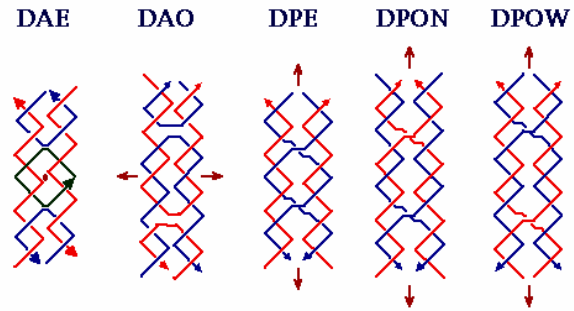




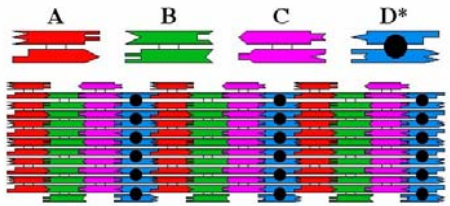
DNA Nanotechnology

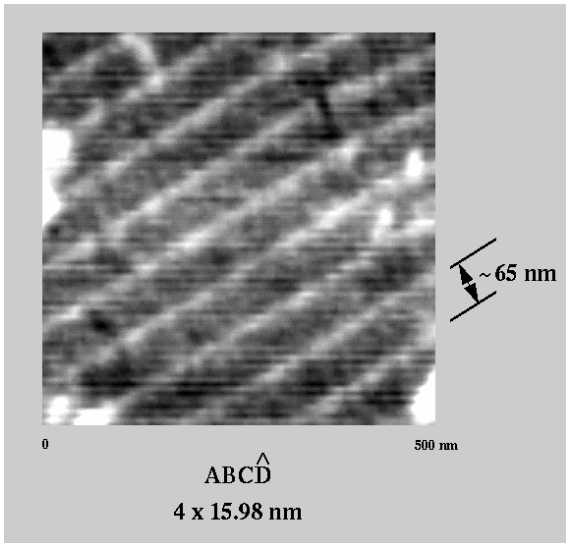




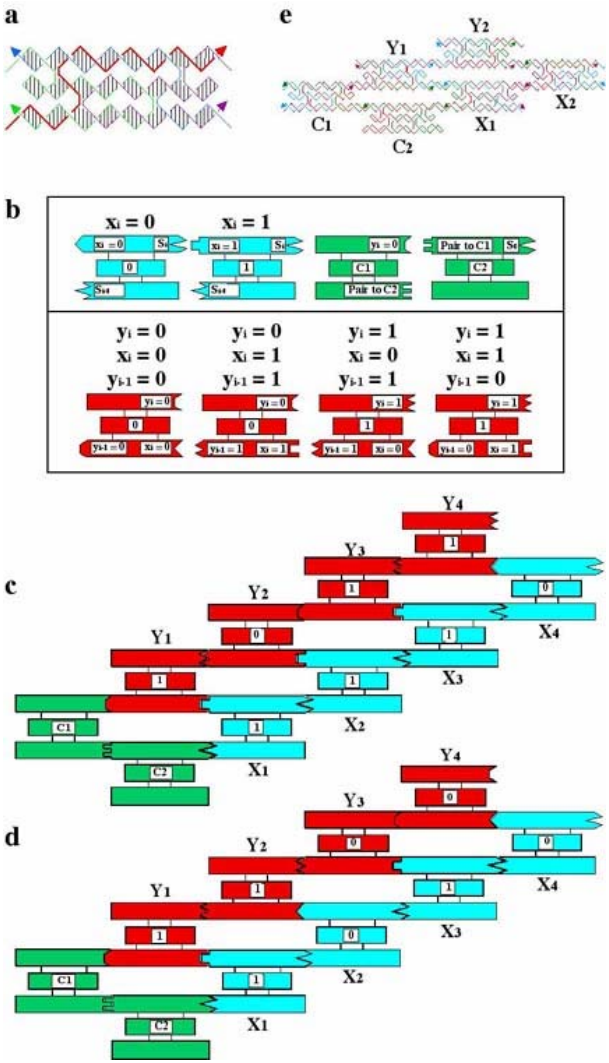


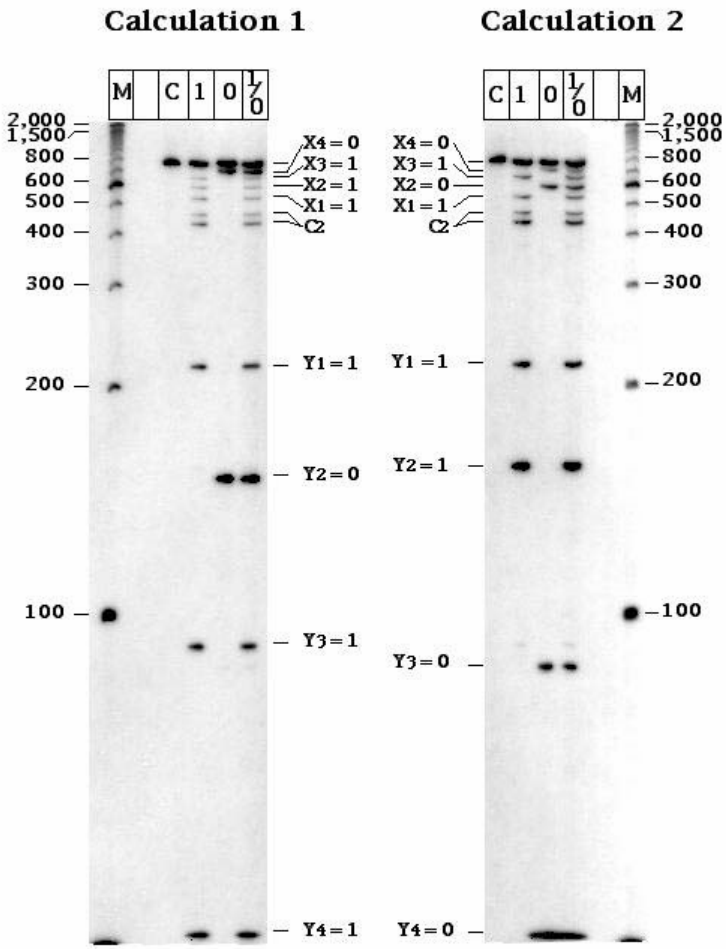
Specifically designed DNA building blocks



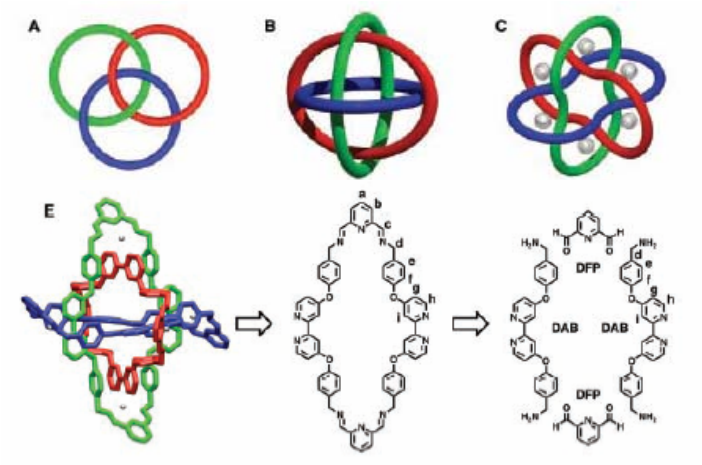


DNA-Based Computation and Algorithmic Assembly -a cool example: $Y_i = XOR [Y_{i-1}, X_i]$

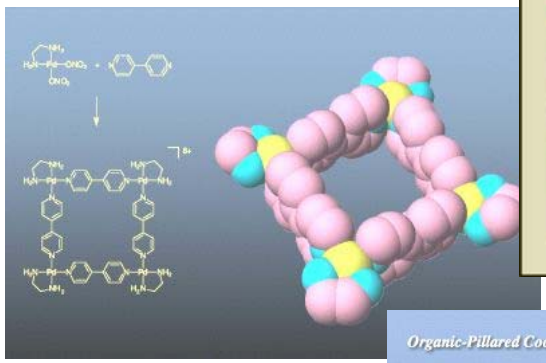


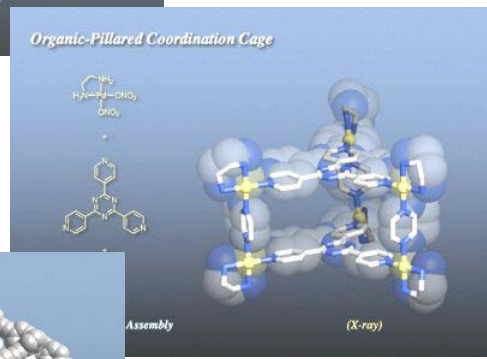


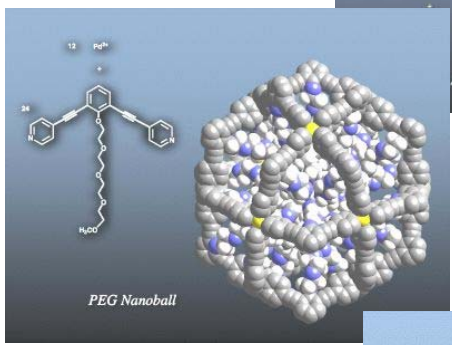
Supramolecules – advanced multifunctional molecules

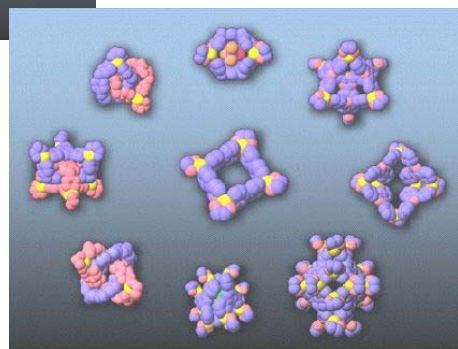


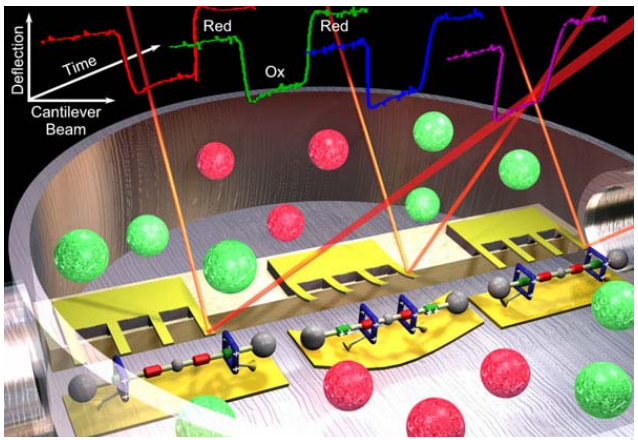
Molecular Borromean Rings









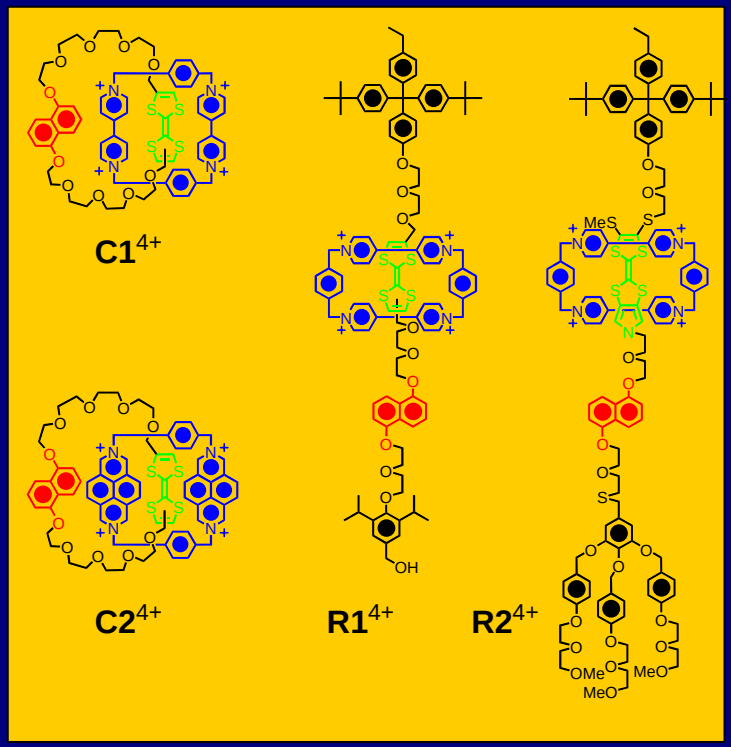


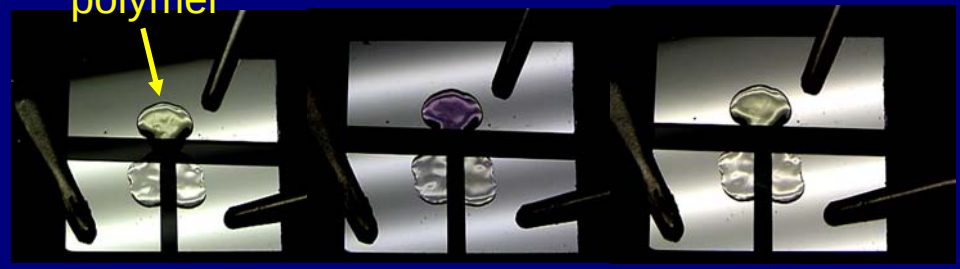
Molecular Muscles

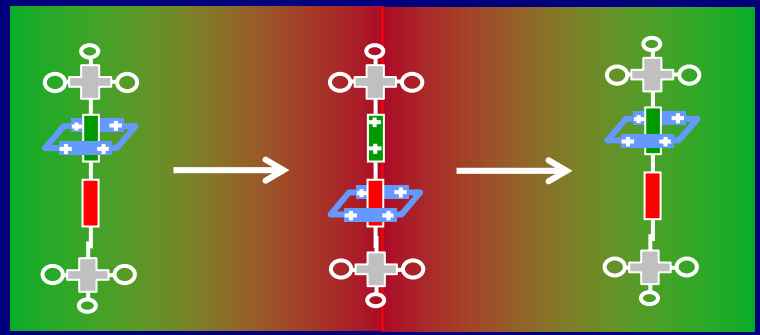
J. Fraser Stoddart Group, UCLA

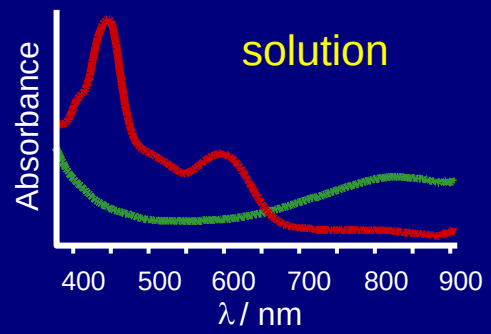
M. FUJITA Group
University of Tokyo

Bi-stable molecules

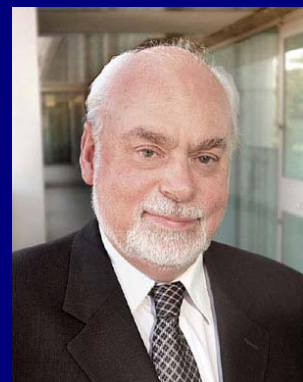






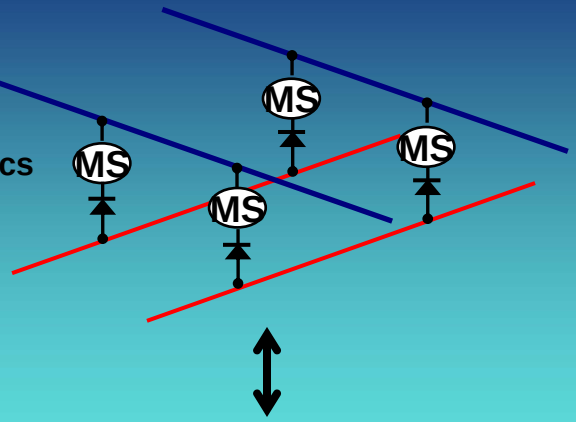


Fraser Stoddart's Group
CNSI / UCLA

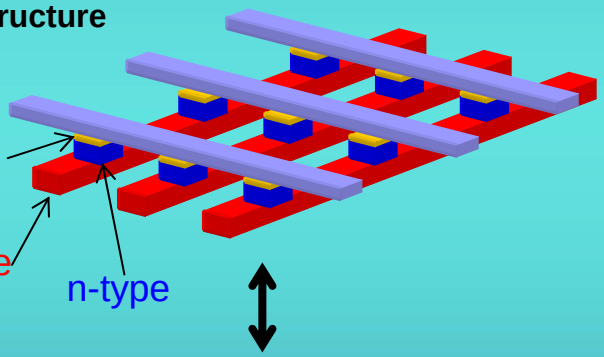


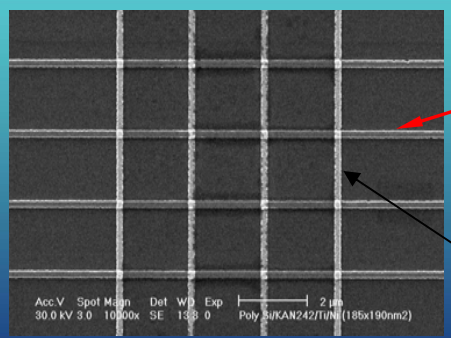
Cross-bar Memory – 10^{11}bit/cm^2

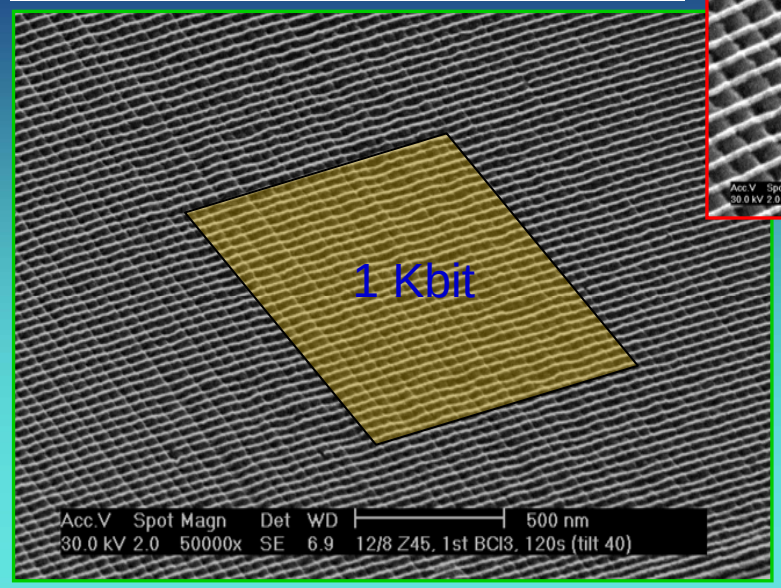
Schematics

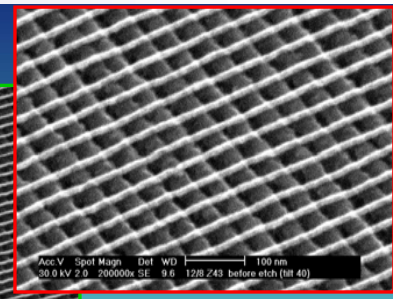


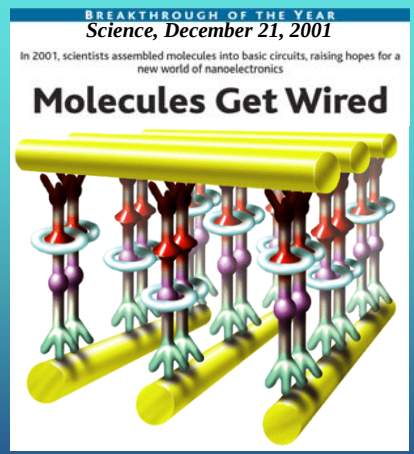
Device Structure

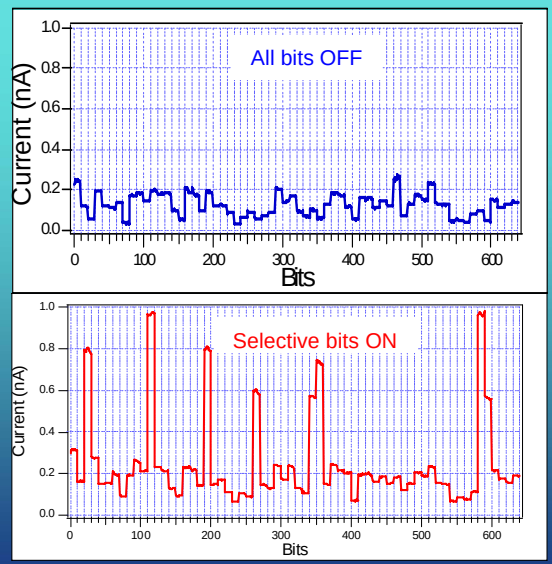




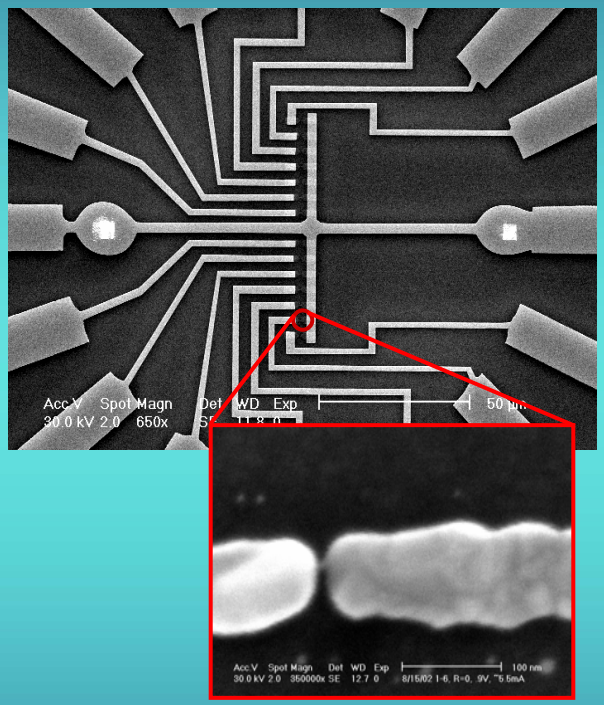




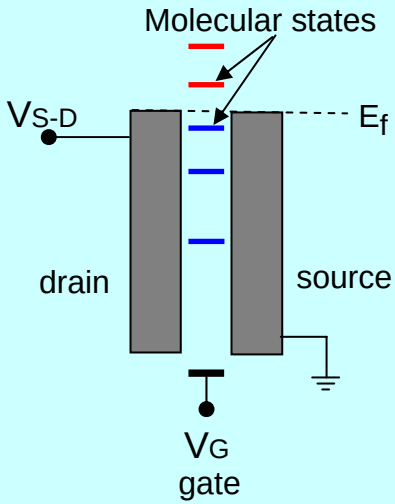




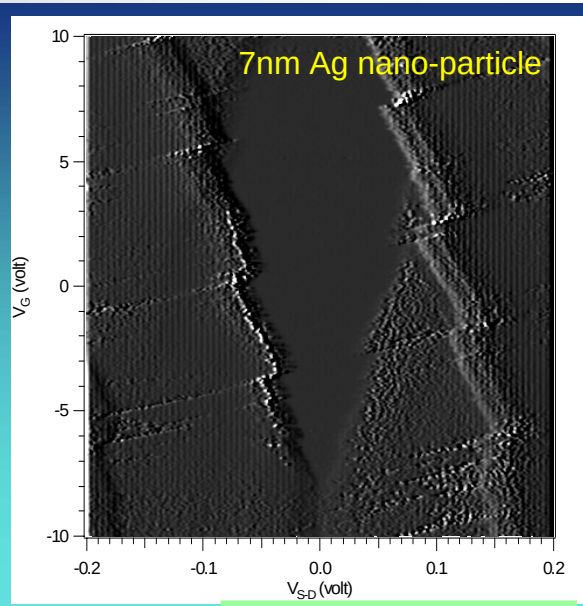
single-molecule transistor

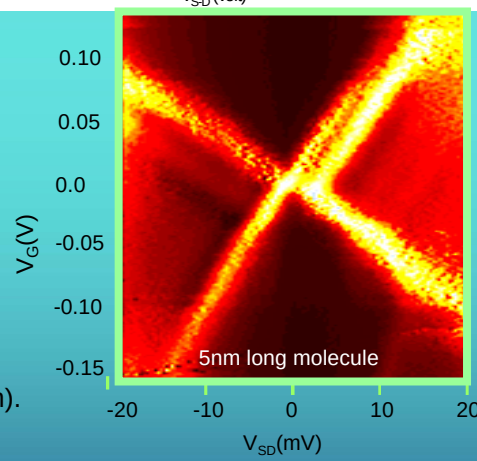


Schematic energy diagram

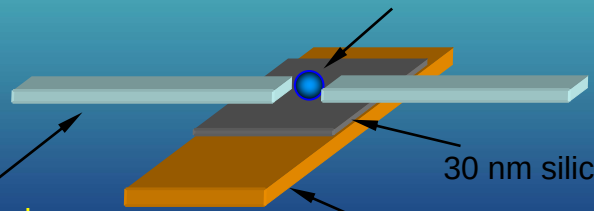


Molecular energy levels
can be tuned by gate potential.





Break-junction with single molecule (gap size can be controlled between ~1 to 10 nm).

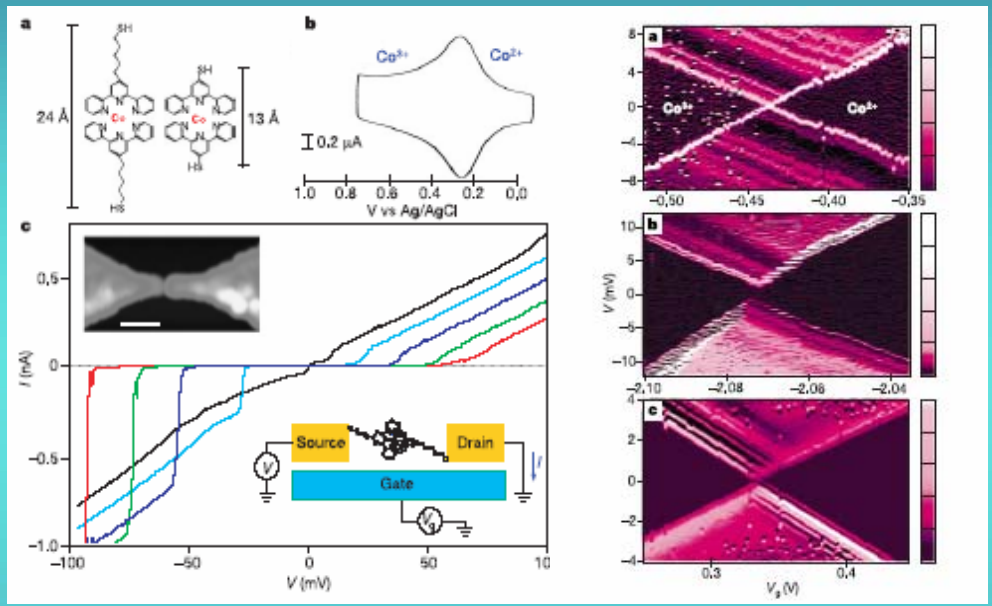


30 nm silicon oxide

Au or Pt electrode

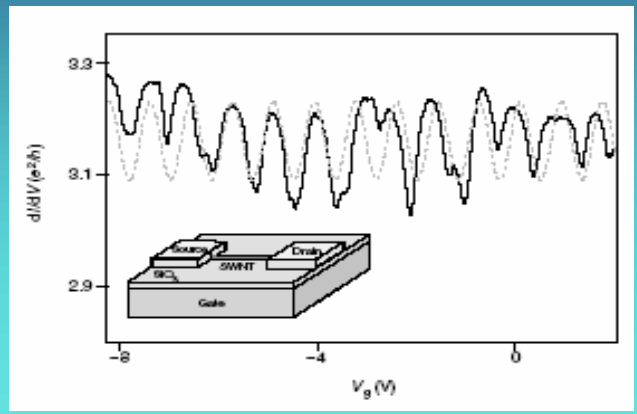
Gate electrode
(degenerately doped poly-Si)

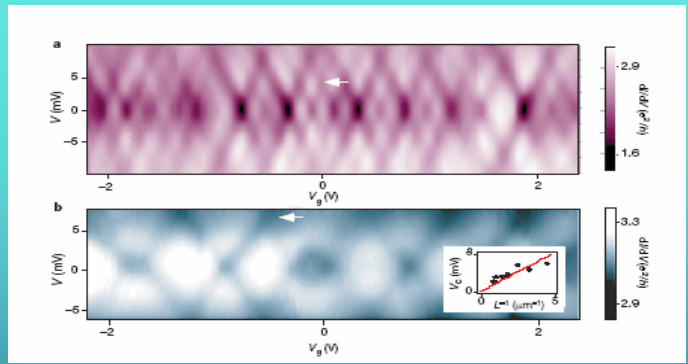
Single Molecule Transistor



P.L. McEuen Group, Cornell Univ.

Fabry-Perot measurement for electron wave

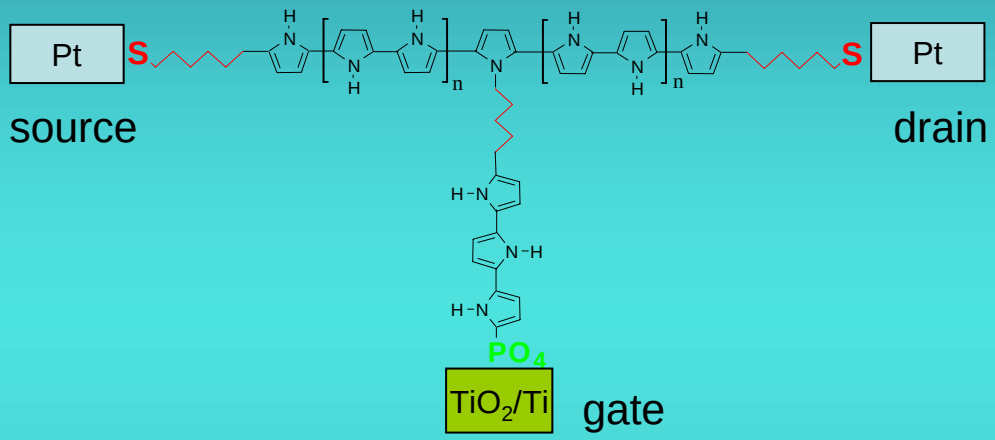


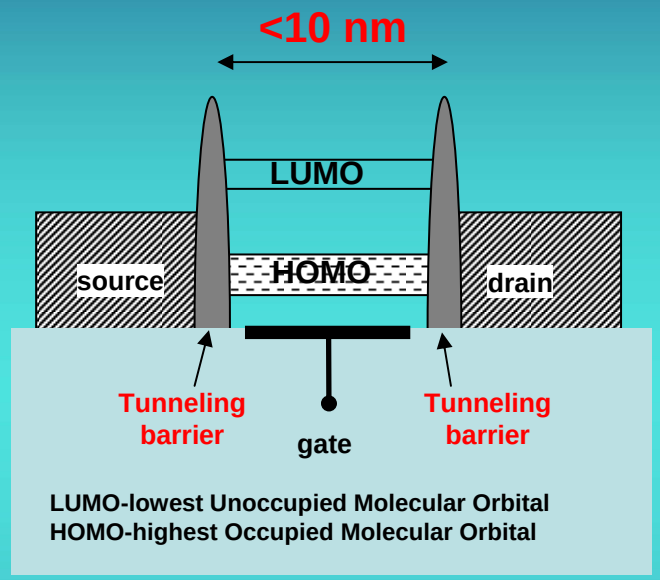


HK Park, Harvard Univ.

A True Single Molecule Transistor

Opportunities to go much smaller than 10 nm where *top-down* and *bottom-up* meet !

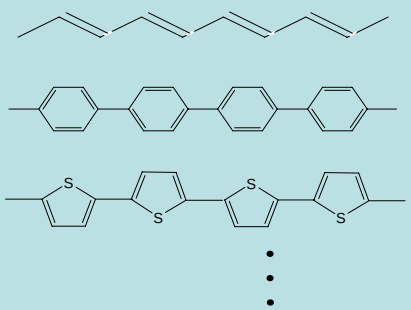




- Built-in gate to increase gating efficiency
- Tunneling barriers to adjust coupling
- Anchoring groups to realize Selective-Self- Attachment

Conductive and Semiconductive Oligomers

- bandgap ~ 1-3 eV
- chemically or electrically doped
- polymer conductivity ~ 5×10^2 (S cm^{-1})

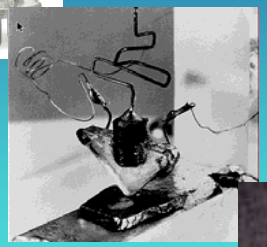


acetylene

phenylene

thiophene

Just in the world of electronics

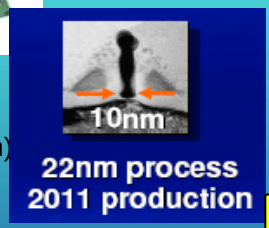


1947, Shockley, Bardeen, & Brattain

1958, Kilby

1971, Intel 4004

current, Intel Xeon
(65nm generation,
36nm channel length)



(Source: Intel)

In six decades, device features have been reduced by x 10^6!

Entering the world where molecules and chemistry work the best!

What's next?
(< 10nm)
How to get there?

Number of transistors on a chip approaching 1 billion vs. 100 billions to 1 trillion neural networks in an average human brain.