Electrical & Computer ENGINEERING

Semiconductor Intellectual Property ("IP") for Digital & Analog Designs

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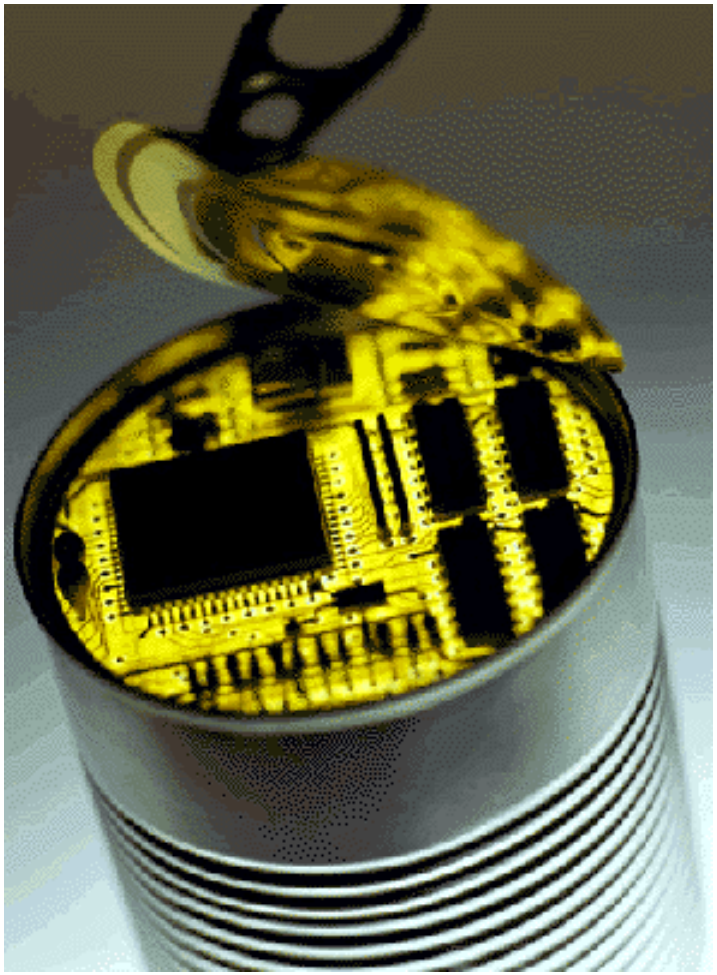
Intellectual Property

- **"IP" is any product of the human intellect that is unique, novel, and unobvious (and has some value in the marketplace).**
  - An idea or invention
  - Expression or literary creation
  - Business method, or industrial process, or chemical formula
  - Computer program / algorithm

- ***Semiconductor* IP**
  - Stuff that let's us design large chips faster, from pre-existing blocks
  - **What are these blocks? How hard are they to design and use?**

You Already Know Two Important Kinds of IP

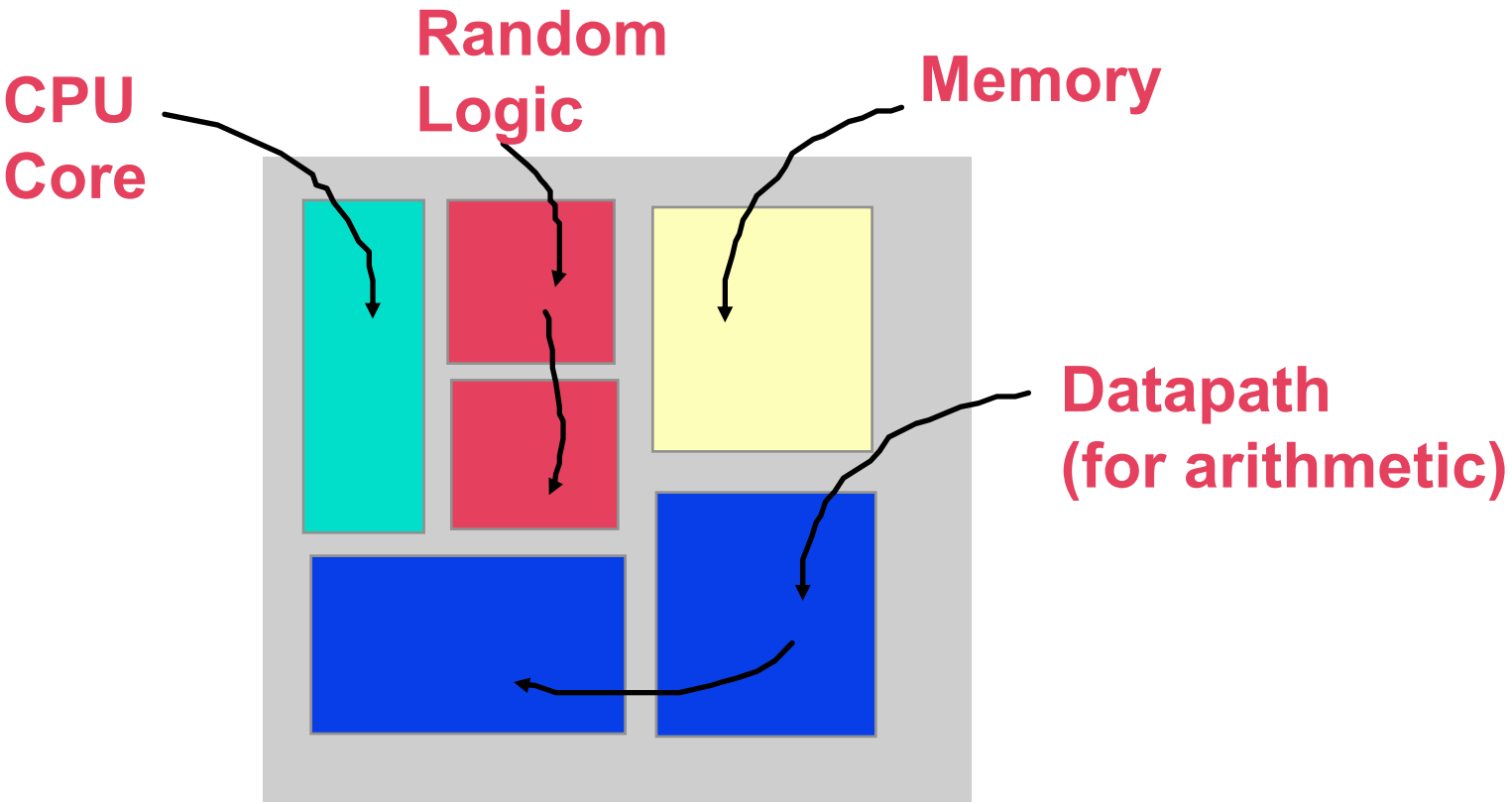
- Chips on boards



- Software binaries or source code

Semiconductor IP Targets "Systems On Chip"

- **Lots of big, separate blocks on a modern "SoC"**
  - I don't want to design them all by myself – I want to just **buy** some of them

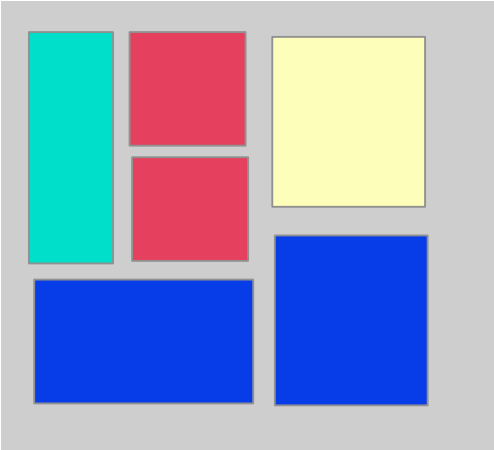


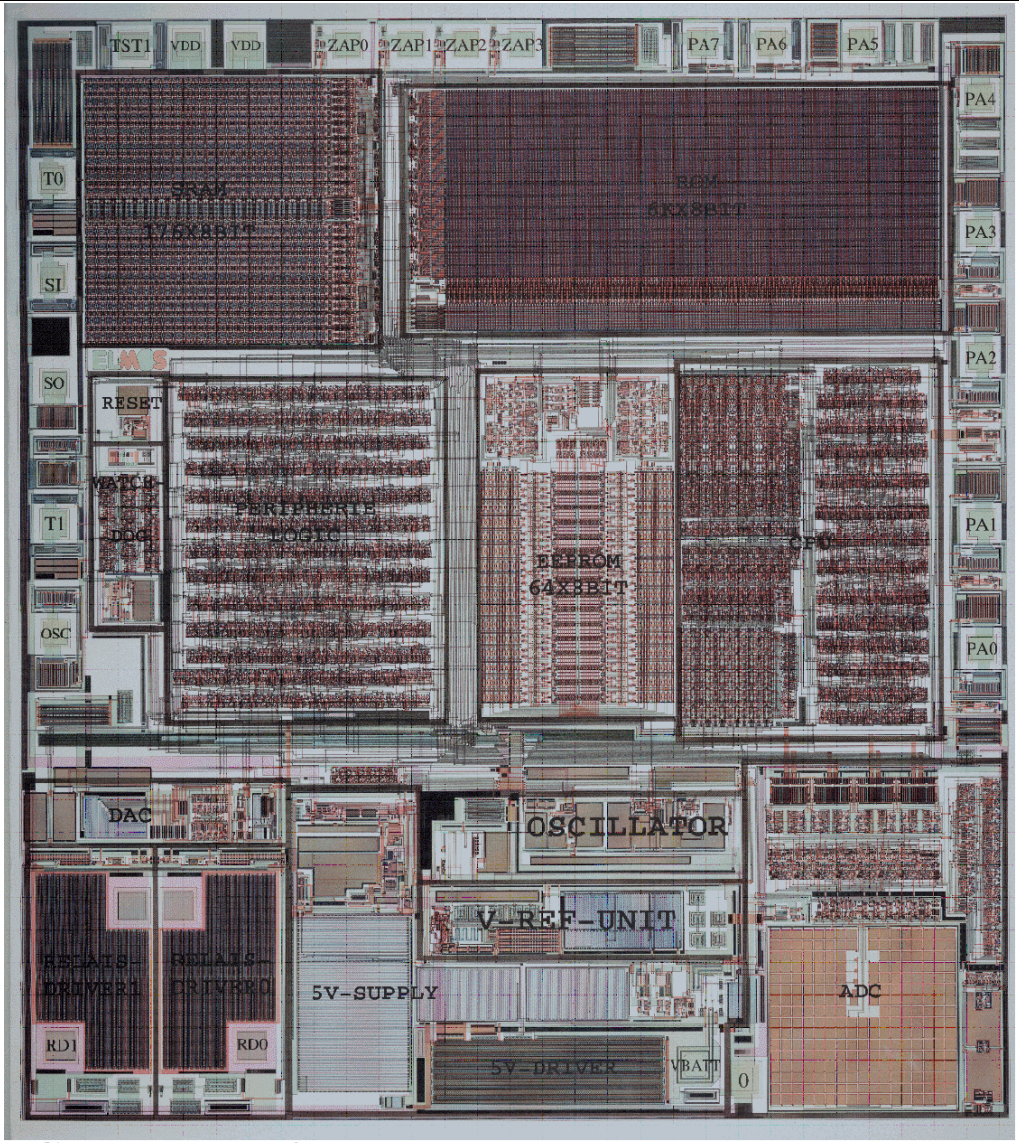
Typical IP Components for Digital Chips

- **Small stuff**
- **Logic gates**
  - Gates, flip flops, adders, muxs, etc
  - Can build arbitrary logic from these
- **Memories, register files**
  - For large storage, beyond a few flip flops, you need these
- **Datapaths**
  - For complex arithmetic beyond simple ADD or MULTIPLY
- **Big stuff –called "cores"**
- **CPUs**
  - 8-bit to 32-bit
  - Small & simple, or big & complex
- **Digital signal processors (DSPs)**
  - For voice, video, image, telecom apps, more efficient than a CPU
- **Single-purpose cores**
  - MPEG engine, MP3 engine, ethernet network processor, etc

Real Example

- They really do look like this...





[Courtesy Neolinear, Inc.]

Automotive SoC Example

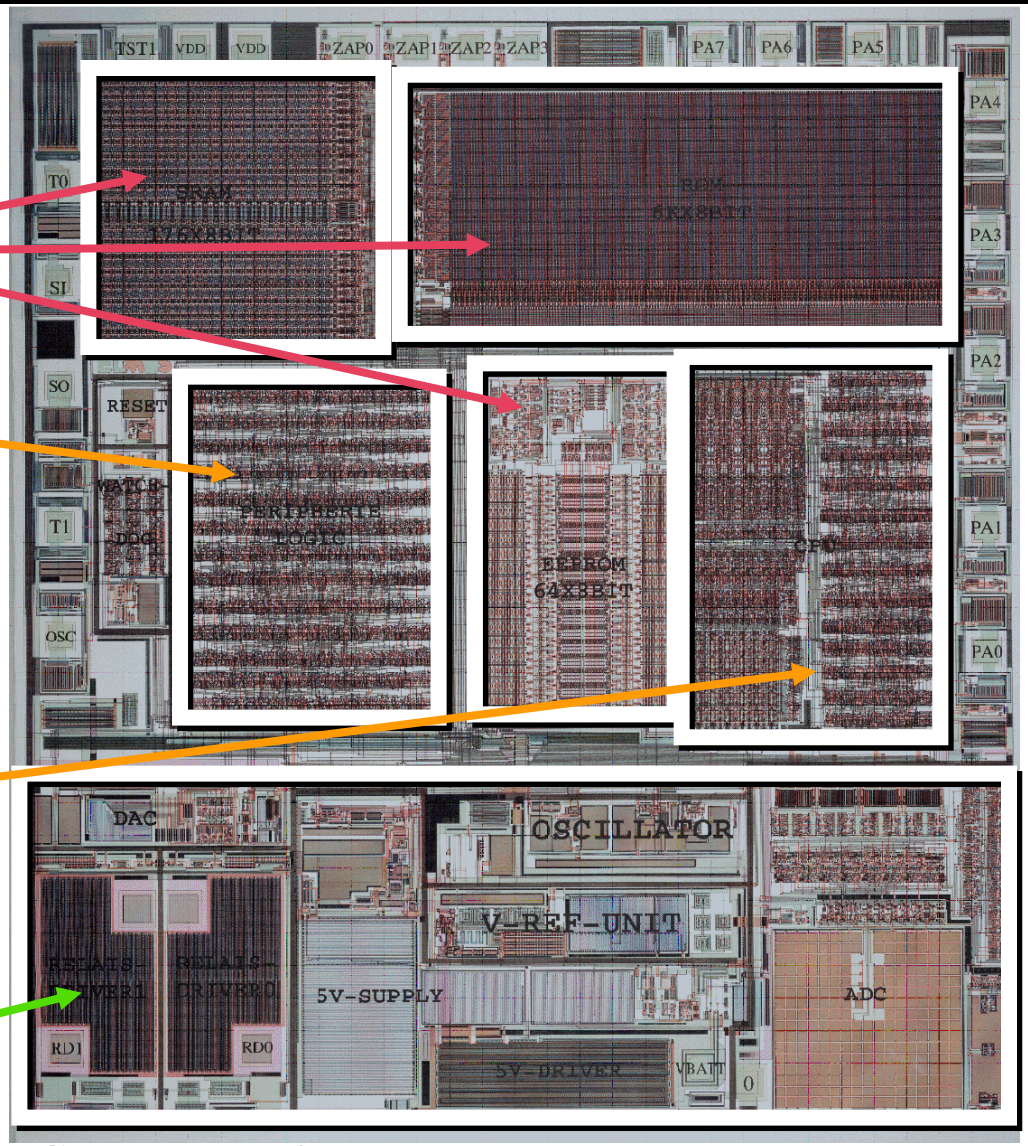
- Look at blocks

Memories

Random control logic

CPU core

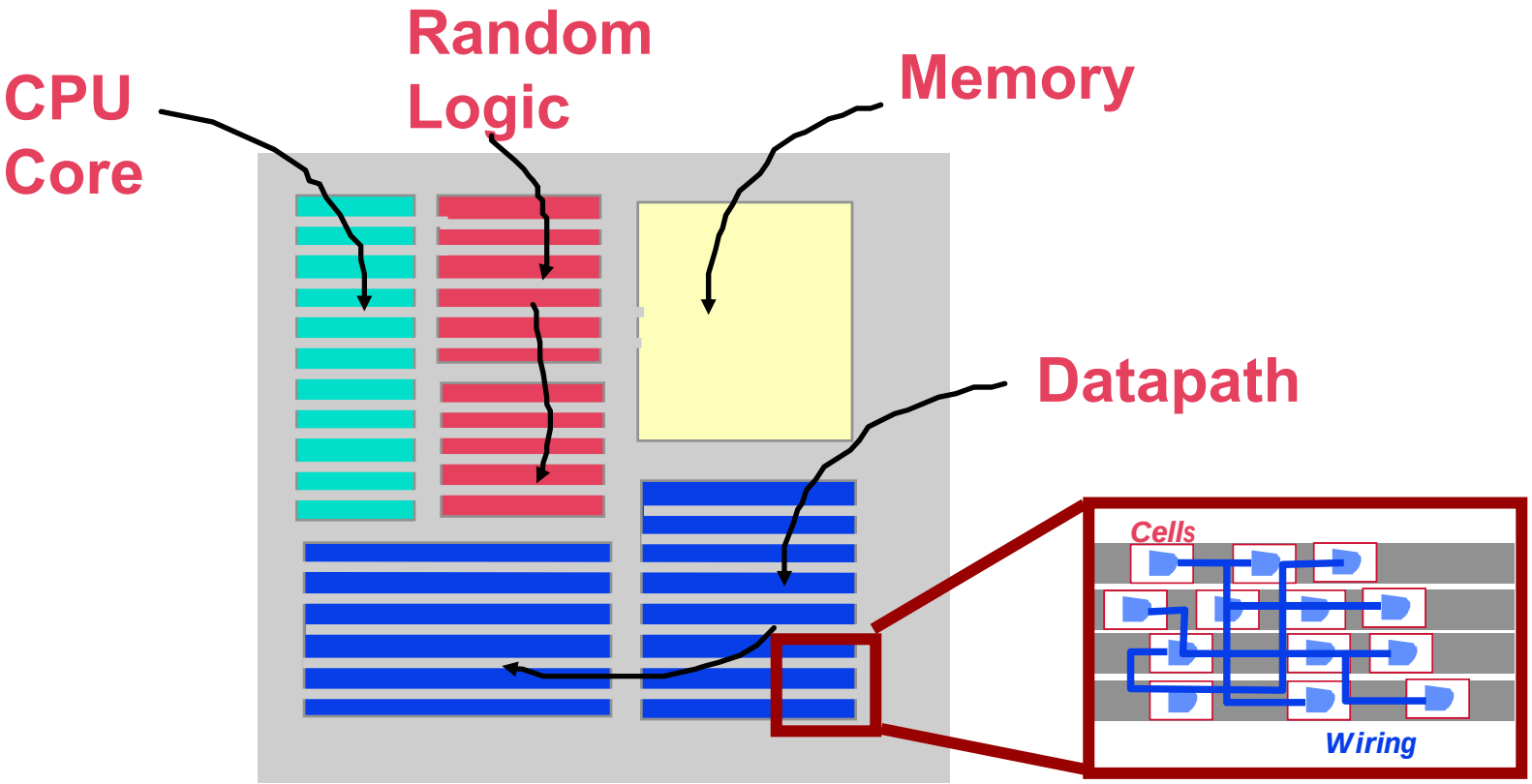
Analog interface to external world



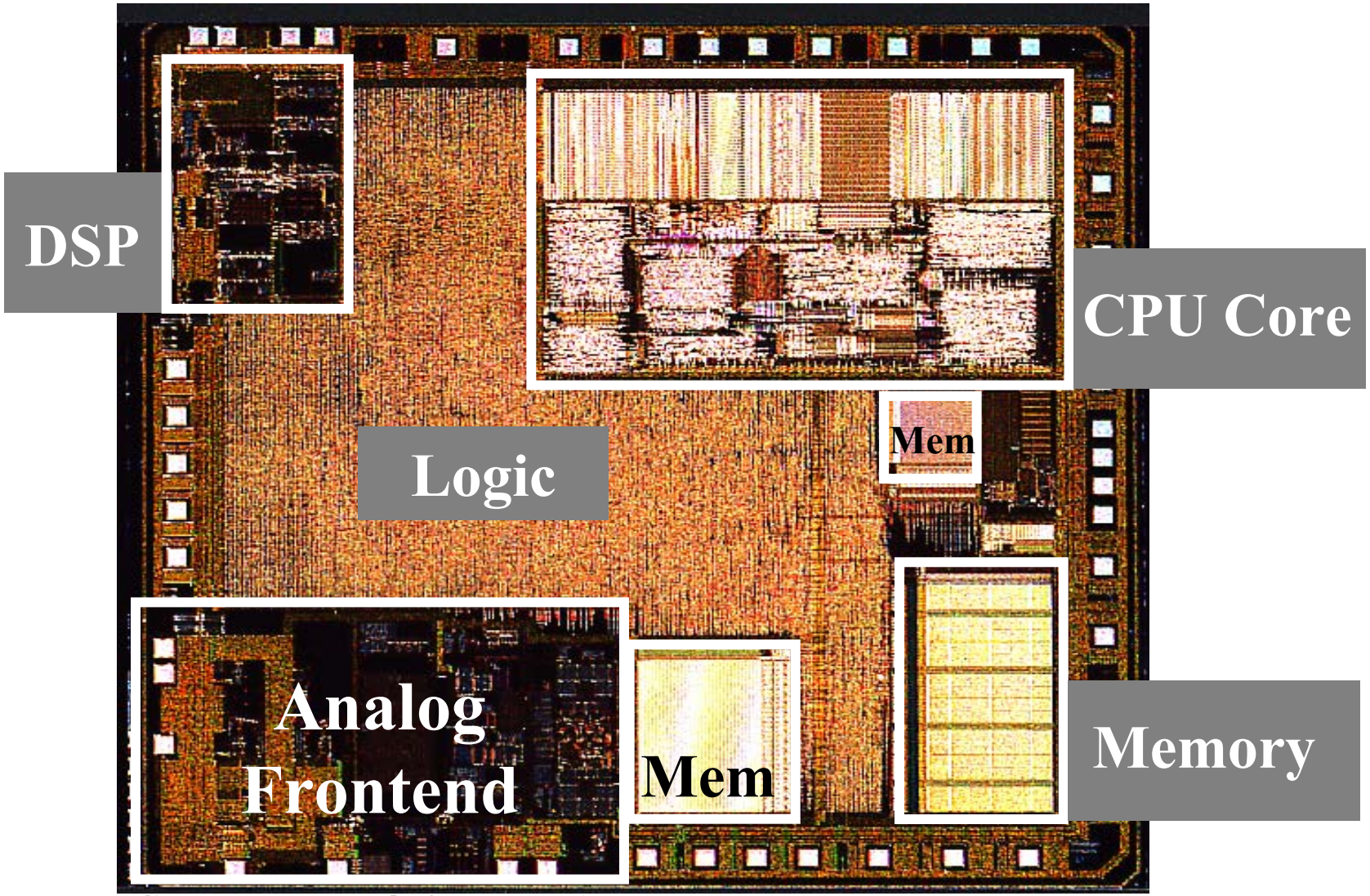
[Courtesy Neolinear, Inc.]

Non-Memory Blocks Are Made Out of Gates

- Called "standard cells" – you buy a "library" of them
  - Standard cell = 1 gate or flip flop
  - Arranged in rows on surface of the chip



Bigger SoC Example: Network Chip

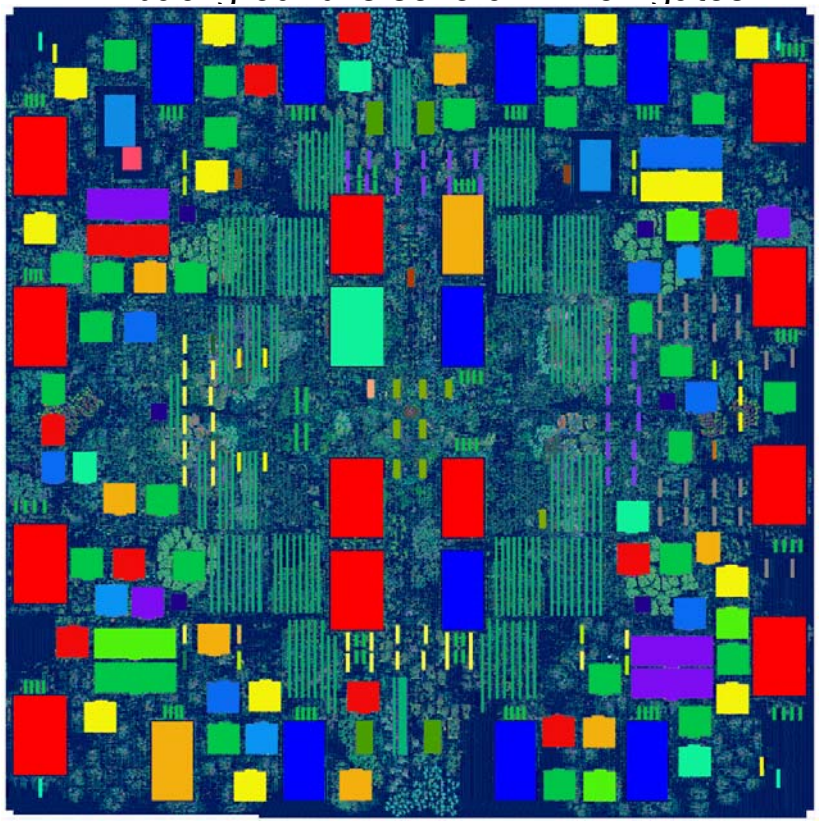


Courtesy Frank Op't Eynde, Alcatel

How Complex – How *Big* – Do These Get?

- **How many "equivalent" gates?**
  - 10 -20 million
- **How many "placed" objects?**
  - 1 – 5 million
  - (i.e., 4X – 5X more "equiv gates")
- **How about memories?**
  - > 100 memories not uncommon
  - Kbits – Mbits per memory
- **IO pins**
  - 200 – 800 common

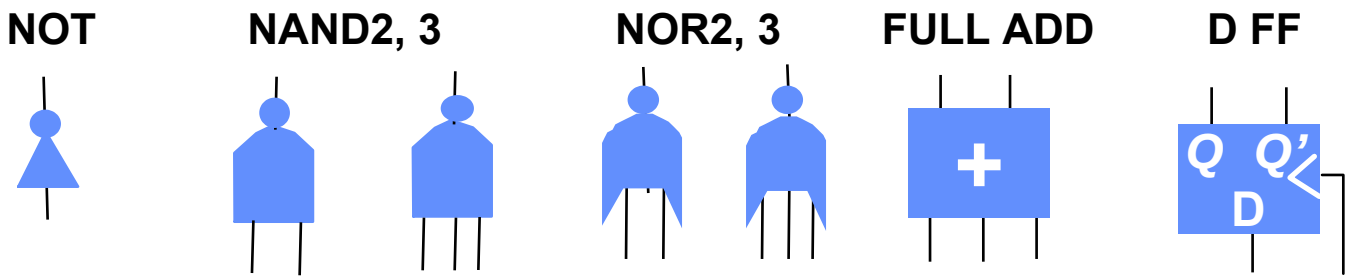
- **Example: IBM network switch**
  - Every big colored block is a memory, background is several million gates



Courtesy Juergen Koehl, IBM

What Do You Actually Get In A “Cell Library”?

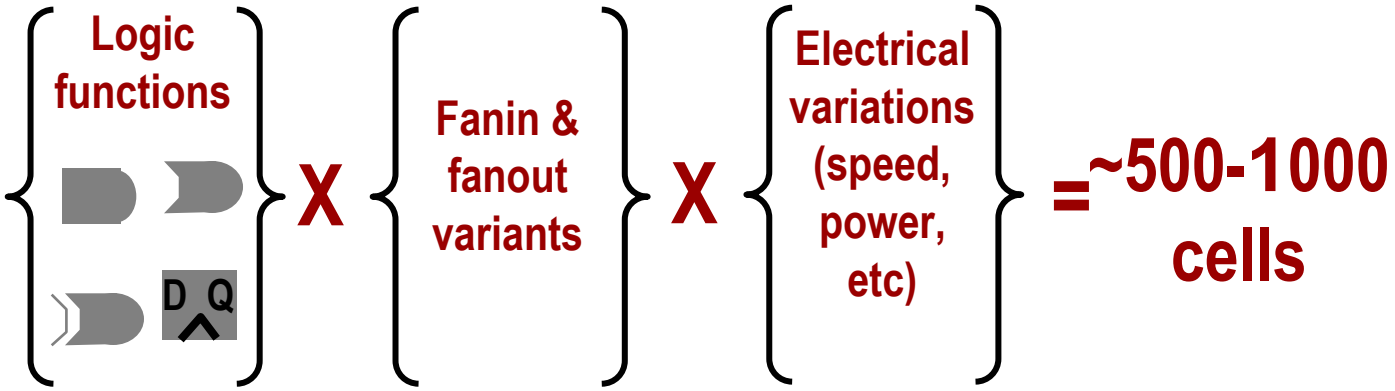
- **You get gates and flip flops and small arithmetic blocks**



- **What you also get…**
  - The timing and power info for each different gate or flip flop--for **simulation**
  - Electrical **circuit** and mask-level **layouts** to use to do the real silicon

How Big is a Std Cell Library--How Many Cells?

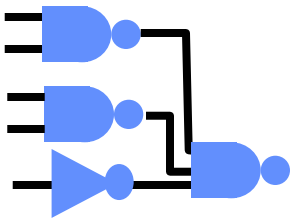
- **Often, pretty big**
  - Big enough to get all necessary logic functions, IO variants, with different electrical properties (eg, speed vs power)



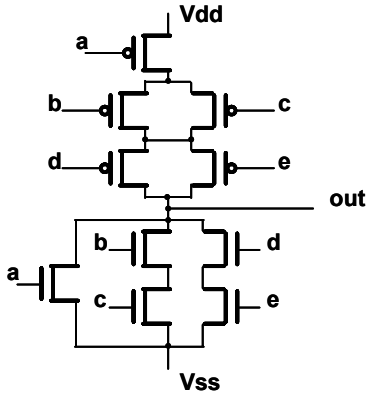
- **Suggested way think about a standard cell**
  - **Inside** the cell: messy silicon/electrical stuff
  - **Outside** the cell: a box with pins
  - Cell **hides** these messy silicon details

Logic → Circuit → Layout Abstractions

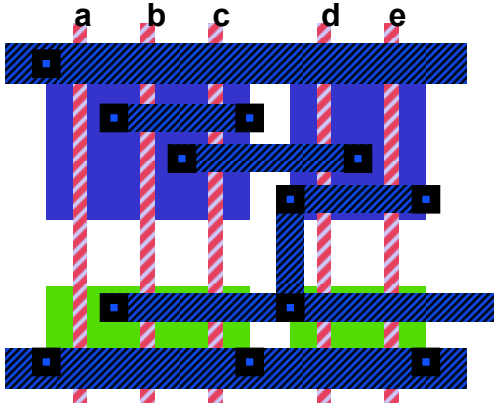
A complex library gate (AOI221)

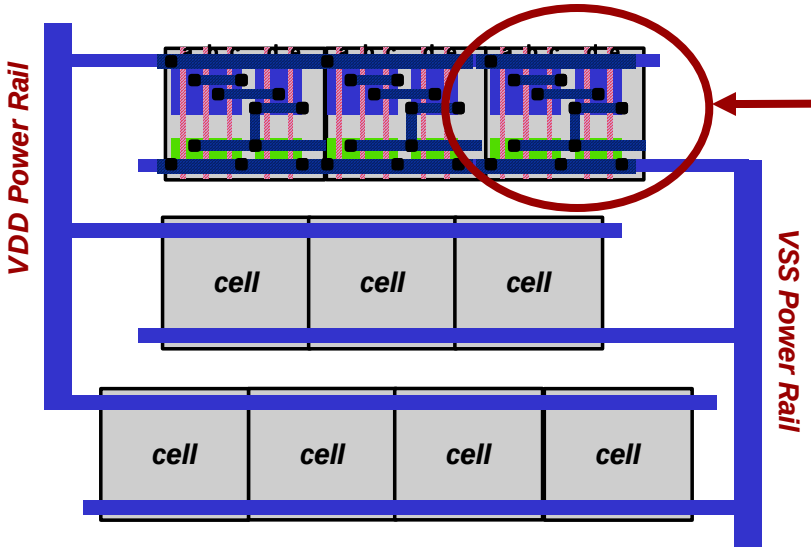


Transistor circuit



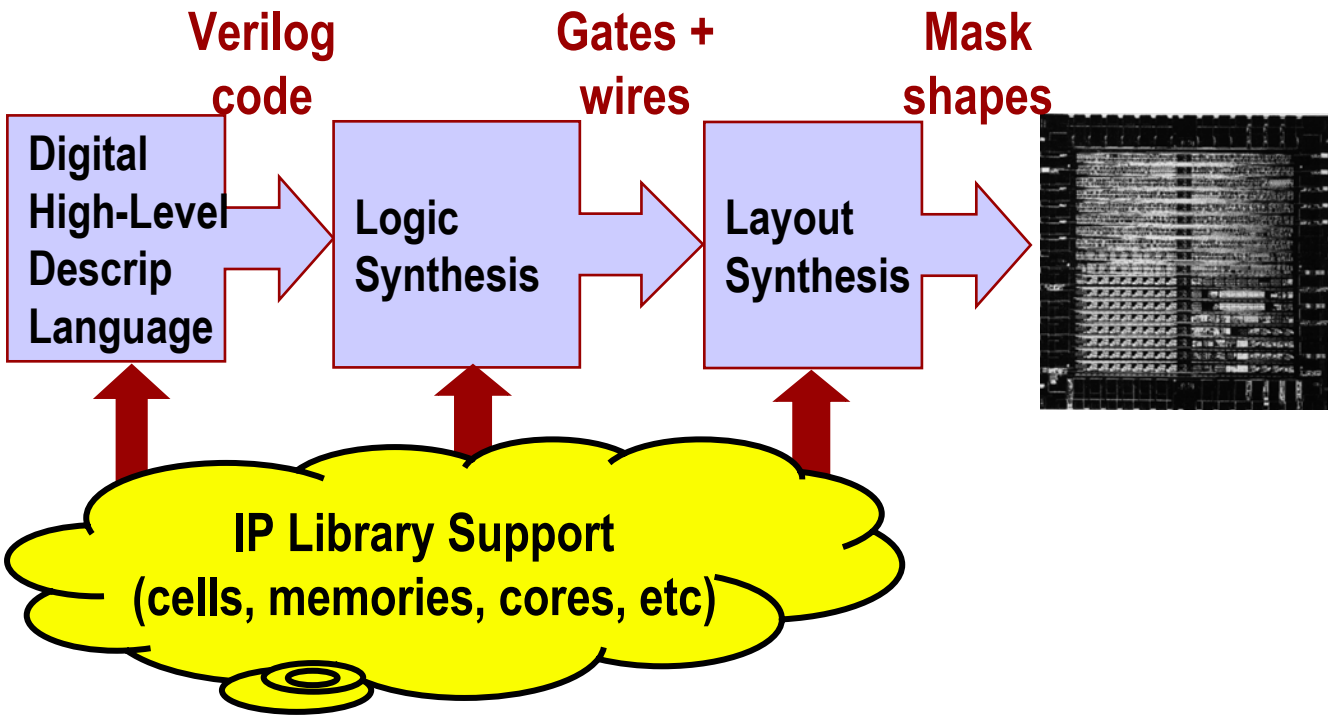
Mask shapes for layout





Placed in rows on surface of chip; wires go over the top of the cell rows

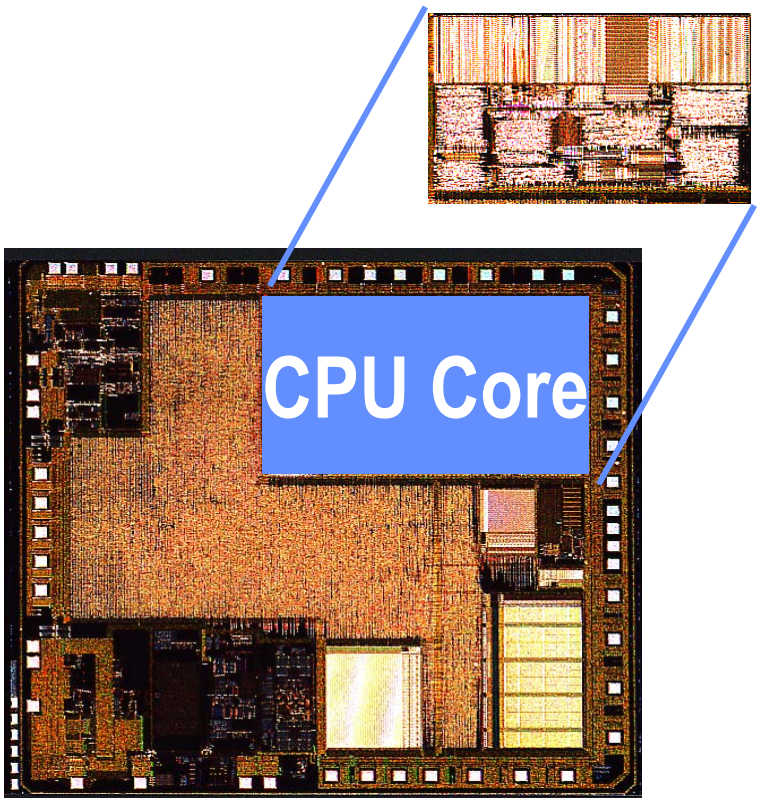
How Does Overall Design Happen?



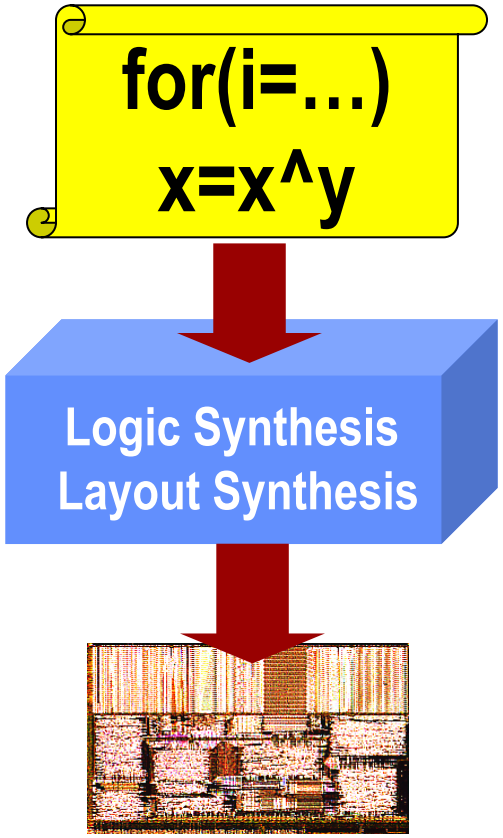
- Thru a sequence of CAD tools, that use these various libraries, IP blocks, etc. Overall sequence is called a "**flow**"

Flavors of Semiconductor IP: Hard vs Soft

- Hard IP = a fixed mask layout for the block you want to use



- Soft IP = a synthesizable version of block, eg, a Verilog program



Example: CPU vs Memory Cores

- **People often buy CPUs as hard IP cores**
  - Just get the layout, drop it in your chip as a block, and run with it
- **But memory blocks are not like this. They're usually soft**
  - You don't buy a layout.
  - You buy a program that "makes" the memory layout. Called a "**generator**"
- **Why? Too many different memory variations for hard IP**
  - You want to specify how many words, how many bits/word, how fast, how much power consumed, what shape the memory block should be, etc etc
  - Easier to provide this flexibility in software that builds the memory structure

You Already Know a Version of This Tradeoff

Software

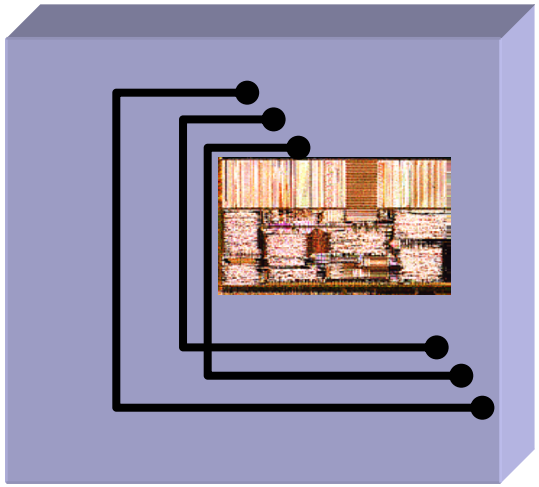
- **Hard IP = Executable Binary**
  - You get the binary file
  - You can run it, cannot change it
- **Soft IP = Source code**
  - You get the source itself
  - You can change it as you like
  - You get to compile it

Semiconductor IP

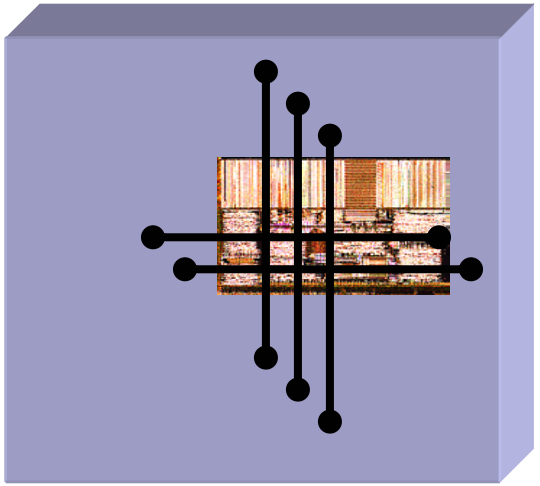
- **Hard IP = mask layout**
  - Cannot change it
  - Only works in a specific semiconductor mfg process
  - Min flexibility, max “ease of use”
- **Soft IP = Synthesizable version**
  - Can change it, can move it to any mfg process for chips you want
  - Lots more work – you have to synthesize it, make sure its correct

Hidden Side Effects With Hard IP

- **Related to fact that the manufacturing process for chips is *very* complicated**
- **Problem: Mfg steps on one part of chip can affect other parts**
- **Typical example for hard IP**
  - You buy a layout for a CPU core
  - Vendor guarantees the performance – eg, the speed…
  - …but only if you do **not** put any wires over the top of the block(!)



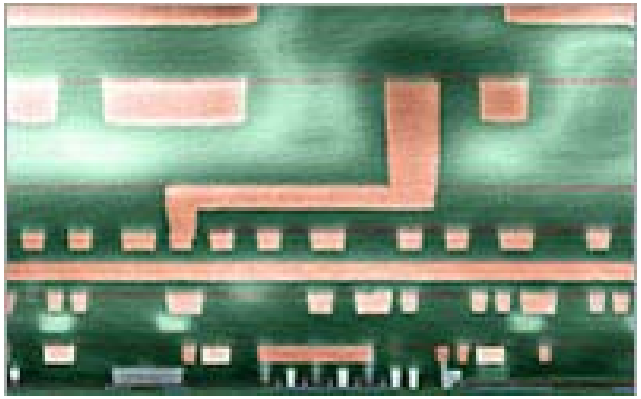
OK



No!

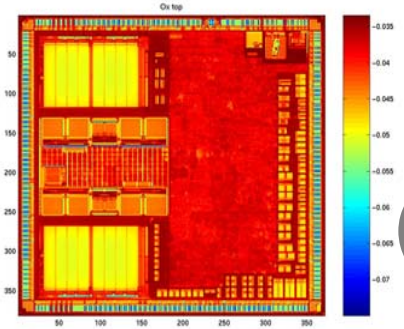
Why? *Many* Layers of Metal Wiring on Chip

- 10 layers in a modern microproc

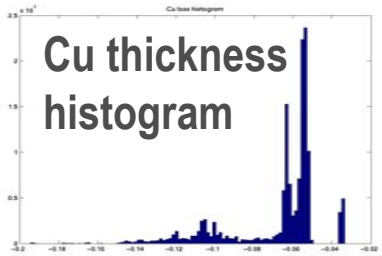


Cross-sectional view of IBM G5 processor wiring done in copper technology

- Unfortunately, stuff "over there" affects stuff "over here" on chip



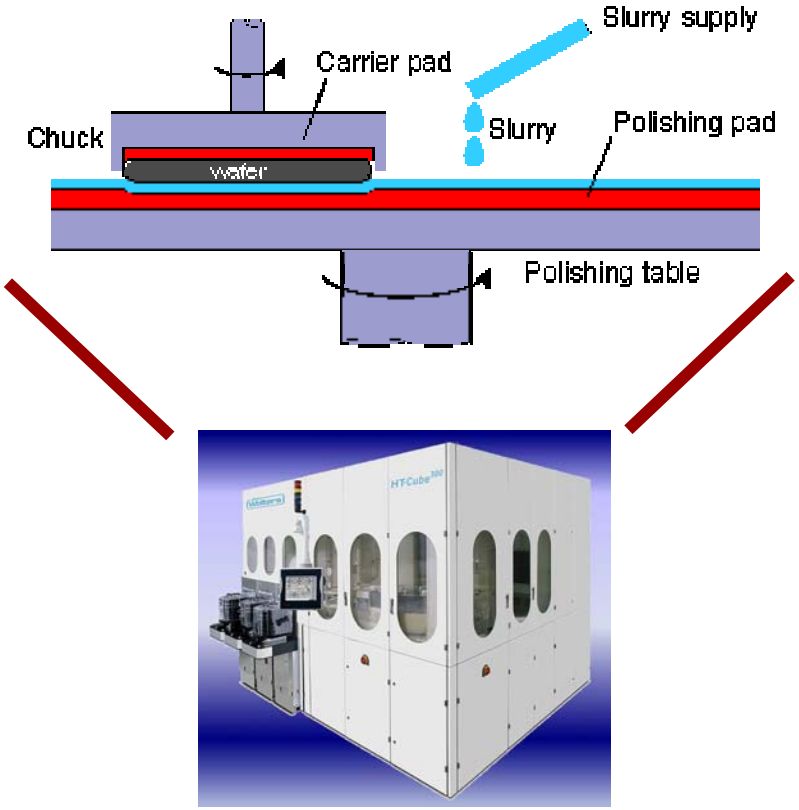
Cu thickness distribution (different chip)



[Courtesy IBM]

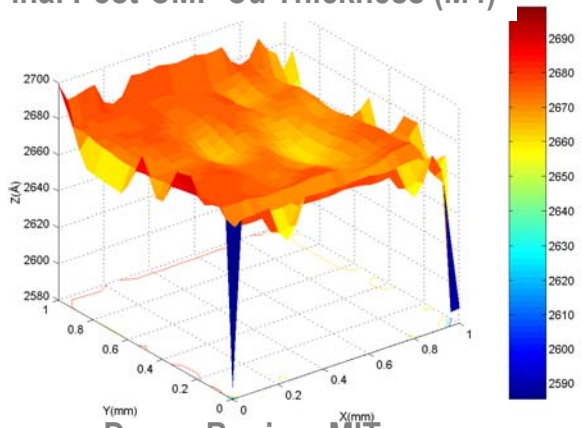
Example of Chip Mfg Interaction: CMP

- ***Chemical Mechanical Polishing*** **– used to make each metal wiring layer "flat" so you can put the next metal layer on chip**



Thickness **depends** on how much metal wire is in the neighborhood. Thickness **changes** electrical behavior of these local wires

Final Post-CMP Cu Thickness (M4)



Duane Boning, MIT

Consequences for IP

- **As technology "scales" and gives us smaller transistors, it also makes these across-the-chip manufacturing effects worse**
  - Hard to be perfect fabricating things that are ~100-1000 atoms across
- **So – how does this impact semiconductor IP?**
- **Many people think hard IP will soon be dead**
  - You cannot guarantee its performance if it depends on what *other* stuff you choose to put on the chip
  - If you cannot *change* it – remember, it's a fixed layout – then you have no hope of *correcting* these problems inside the IP block
  - So, maybe the future is all about soft IP. This is a big debate today.

Another Aside: IP is Big Bucks Business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ARM to Buy Artisan for $913 Million
08.23.2004, 09:51 AM
Shares of ARM Holdings PLC fell nearly 19 percent Monday morning, following news that the British chip designer plans to buy integrated circuit system maker Artisan Components Inc. for $913 million in cash and stock.

ARM

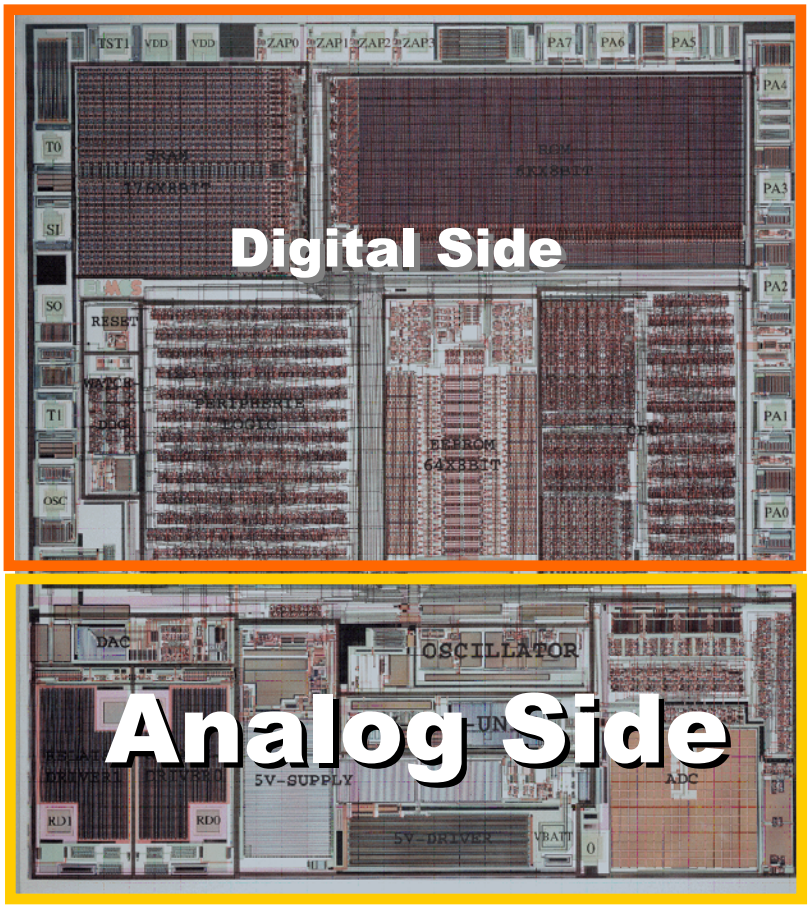
- World's biggest supplier of CPU cores (ARM microproc) for SoC applications

Artisan COMPONENTS

- World's biggest supplier of standard cell libraries and memory blocks for chips

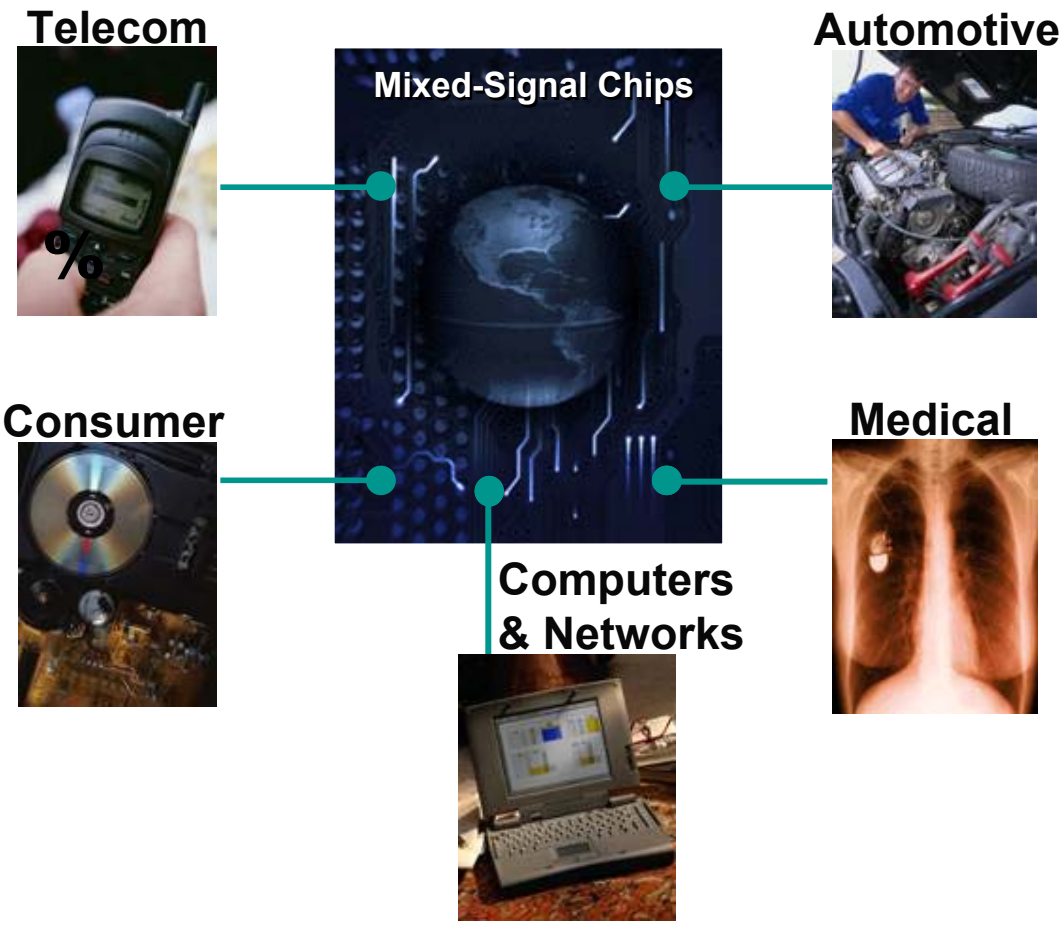
What About the IP for the *Analog* Side…?

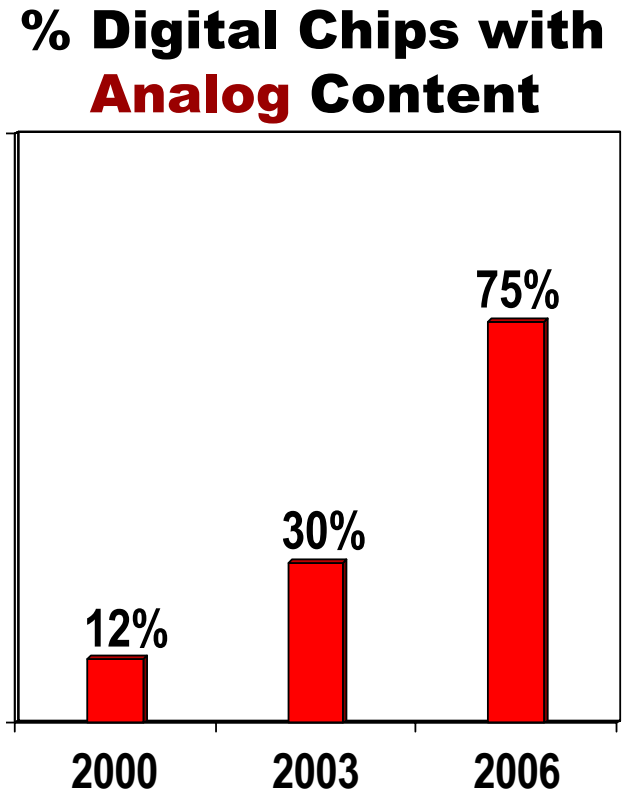
Mixed-Signal SoC Design



[Courtesy Neolinear, Inc.]

Why This Matters: Many "Mixed-Signal" SoCs

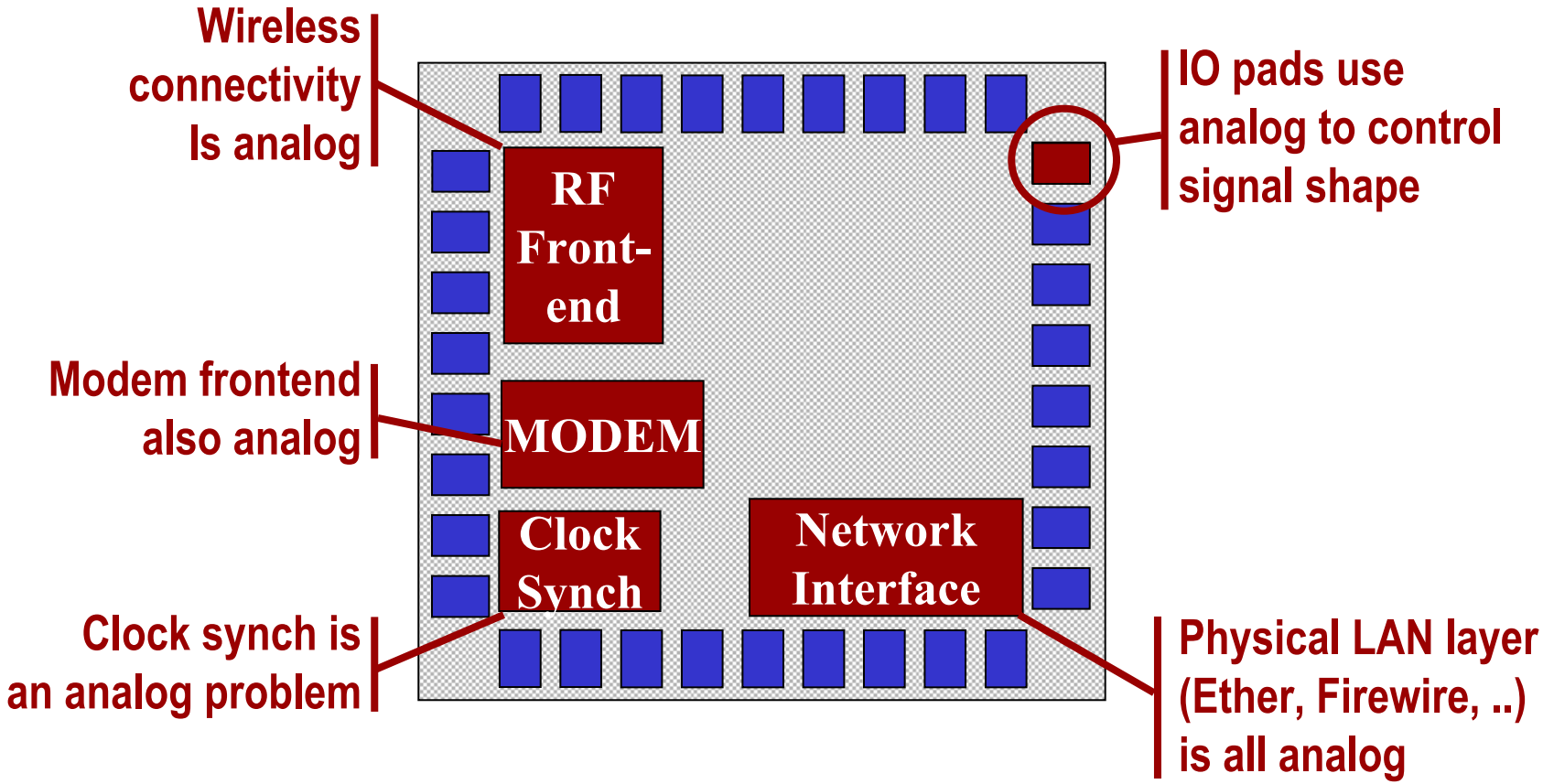




[Source: IBS 2003]

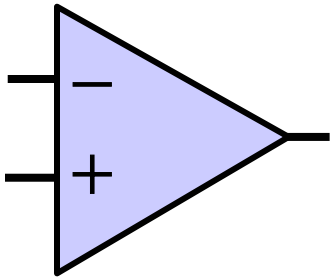
Lots of Digital "Support" Functions Are Analog

- Some obvious, some not



Problem: Analog "Std Cell" Libs Don't Work…

- Why: too many continuous specifications for analog cells



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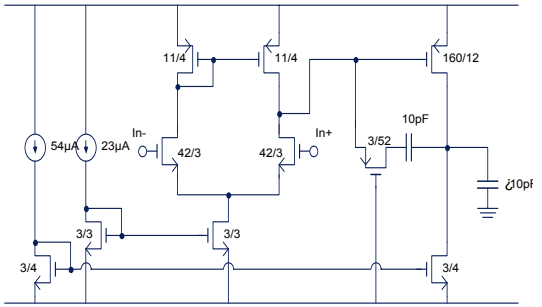

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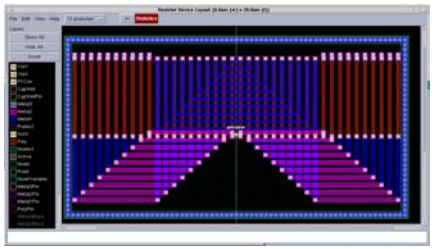
10 independent performance specifications

➡ X { Spec=LOW Spec=HIGH variants for ALL combinations } = **~ 1000 variants for just *this* cell**

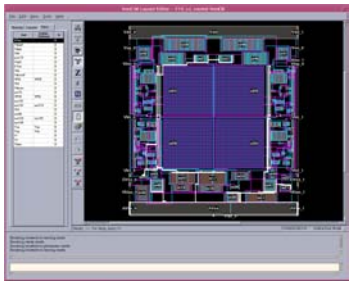
- Can't just build a practical-size, universal analog library

Analog IP: What Are People Actually Doing?

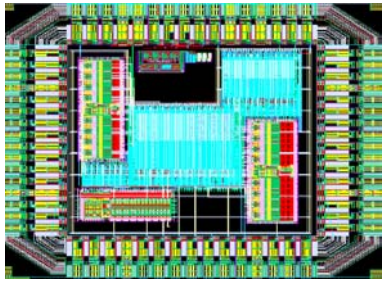
- **Device-level IP**
  - Generators for individual devices
  - Mix of Hard IP & Soft IP



- **Cell-level IP**
  - Synthesizable building blocks
  - Soft IP



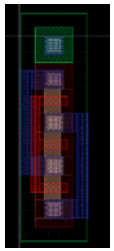
- **System-level IP**
  - Larger blocks for useful chip functions
  - Mix: can be Hard IP, can be Soft IP



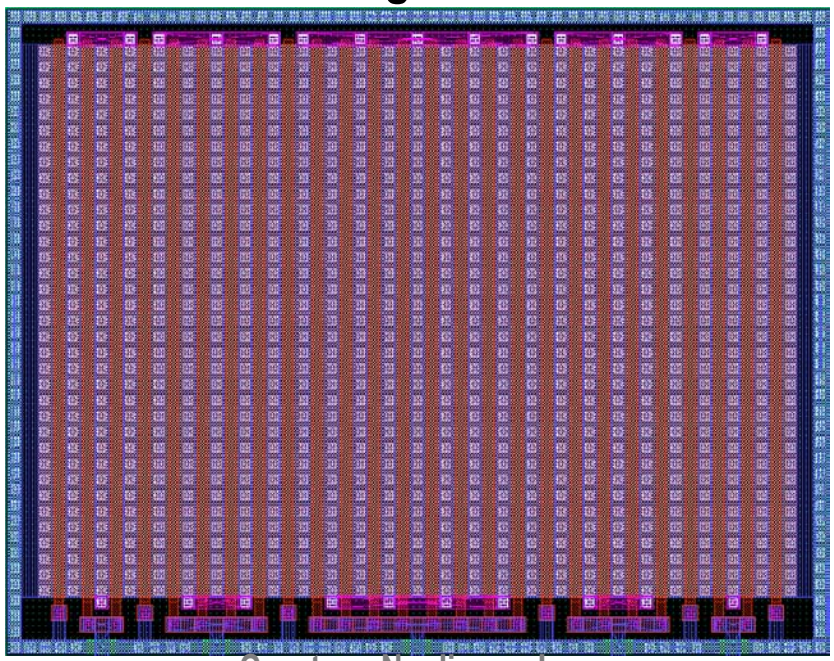
Analog Device-Level IP

- **Individual analog devices a lot more difficult, more "fussy"**
  - Need to deal with very precise electrical quantities, or be very big to handle large currents or voltages at the physical interfaces
  - Making **generators** for these devices – soft IP – is most common

2 Digital Devices



1 Analog Device



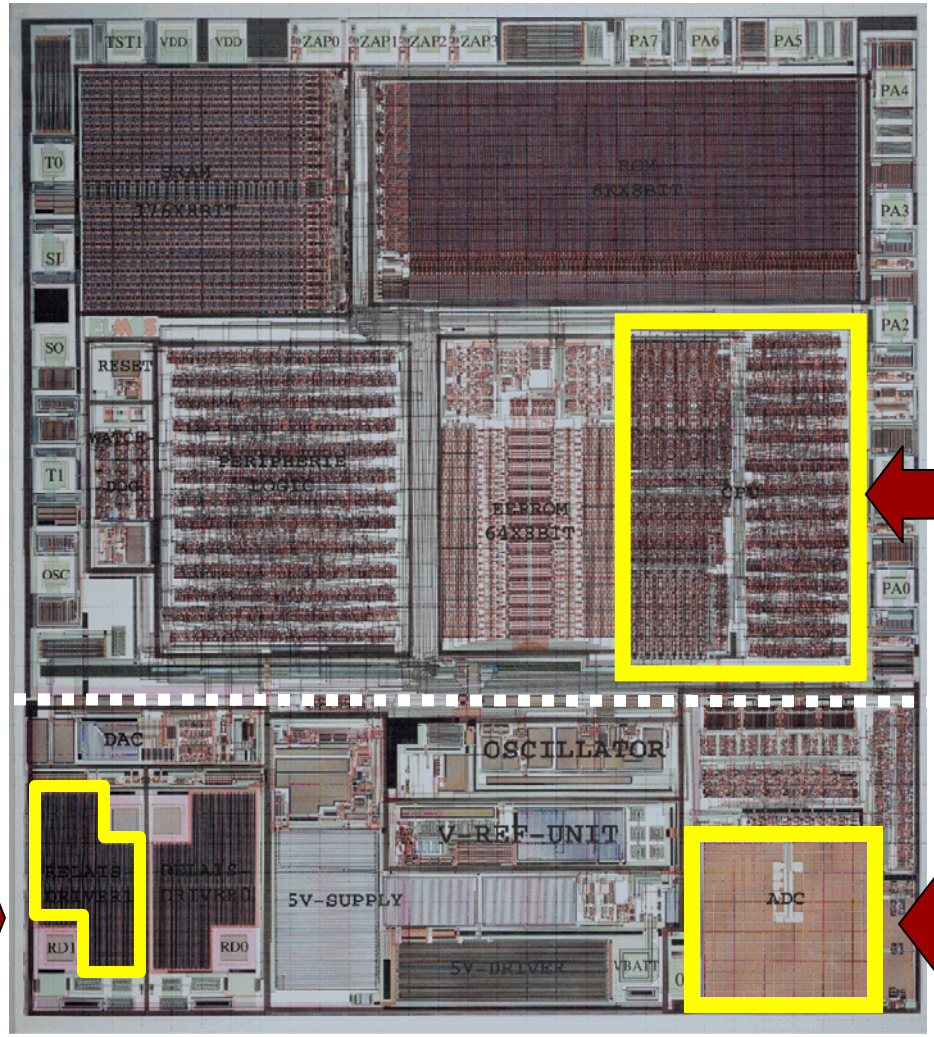
Courtesy Neolinear, Inc

Real SoC-- Analog vs Digital Devices Example

digital

analog

1 FET



A small CPU core

A few capacitors

[Courtesy Neolinear, Inc.]

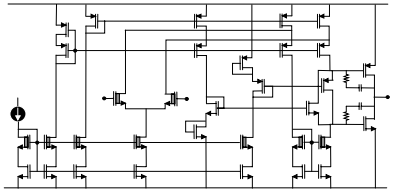
Analog IP: Same Sort of Hard vs Soft Issues

- **But made worse by the fact that analog circuits are much more sensitive to the mfg process than digital circuits**
  - So, they're much harder to design, and to "retarget" to a new mfg process
- **Most analog IP today is hard IP**
  - Buy a layout for something like an Ethernet or Bluetooth interface
- **Synthesis tools for soft IP are just emerging commercially**
  - Took about another 10-15 years to figure out how to do this for analog

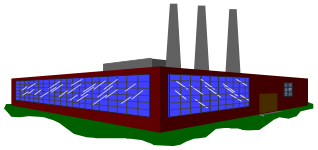
From Analog Synthesis → Analog IP

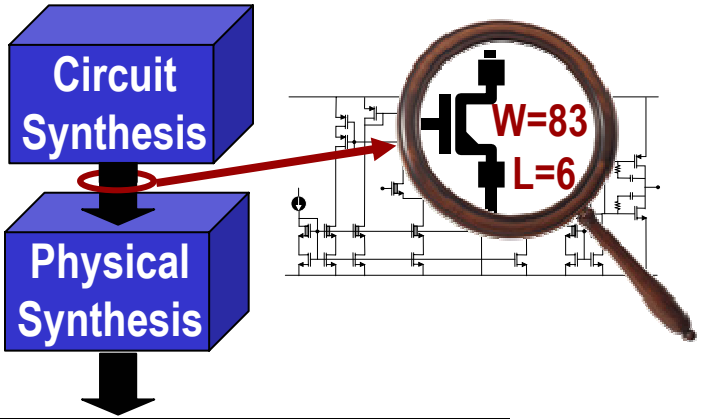
- **From Neolinear synthesis tools -- CMU startup company**

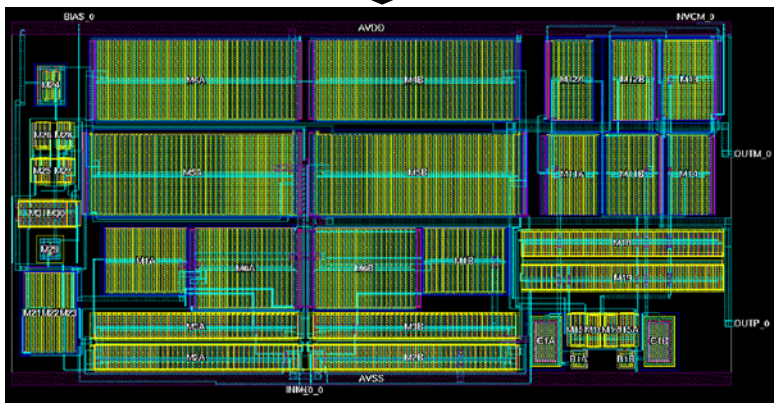
Unsized commercial diff-amp cell



0.6um proprietary CMOS fab

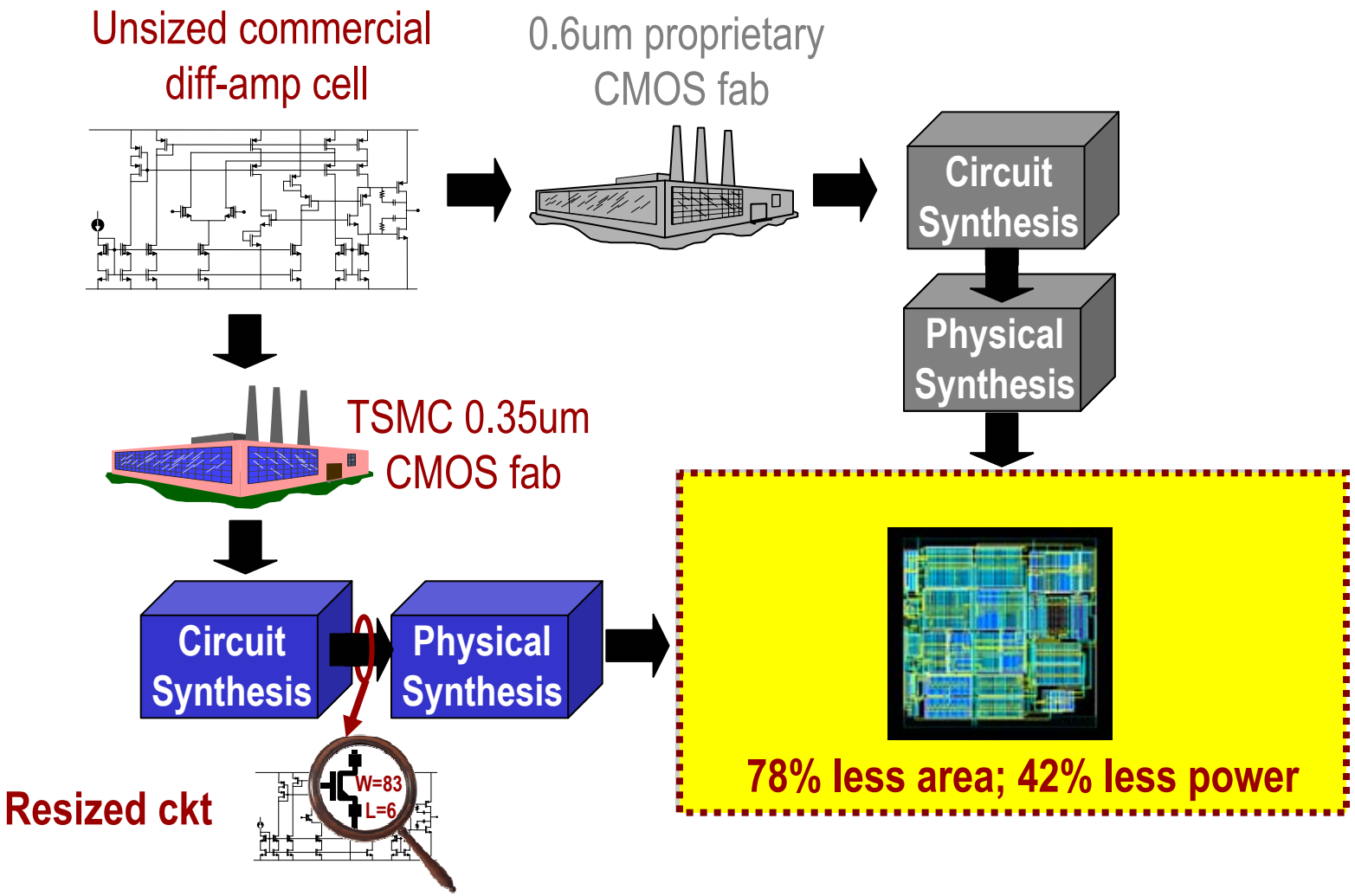






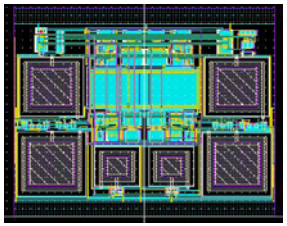
From Analog Synthesis → Analog IP

- **Ex: from commercial version of flow, at SRC member company**

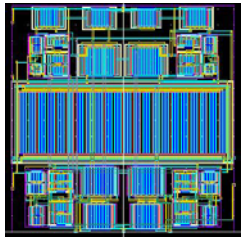


With Synthesis, You Can Create *Soft* Libraries

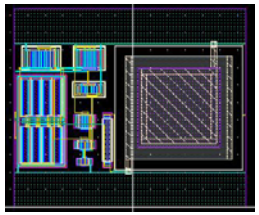
Sample & hold



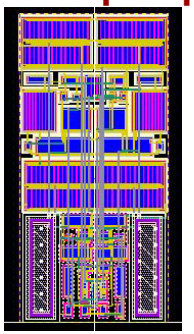
Opamp (CMFB)



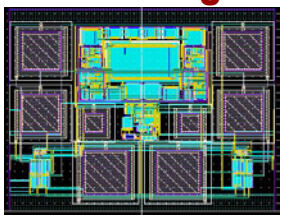
Opamp (2stage)



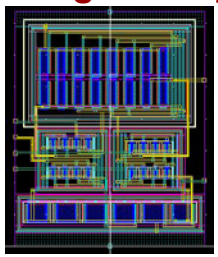
Diff. Opamp



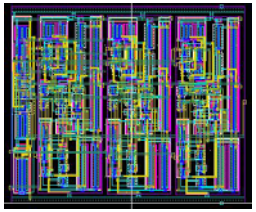
Gain Stage



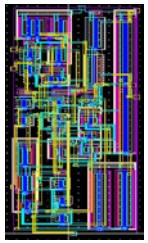
Charge Pump



Divider

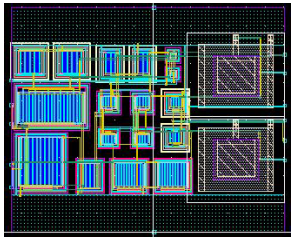


D FF

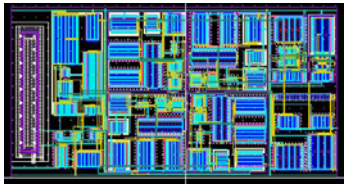


- Examples from NeoIP soft analog IP library of basic blocks

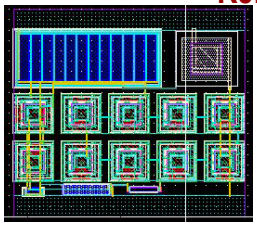
Comparator



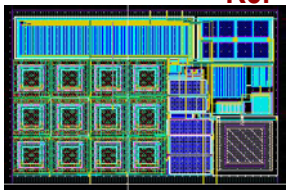
VCO (Diff. Ring)



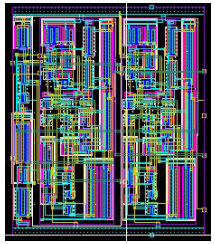
Bandgap V_{Ref}



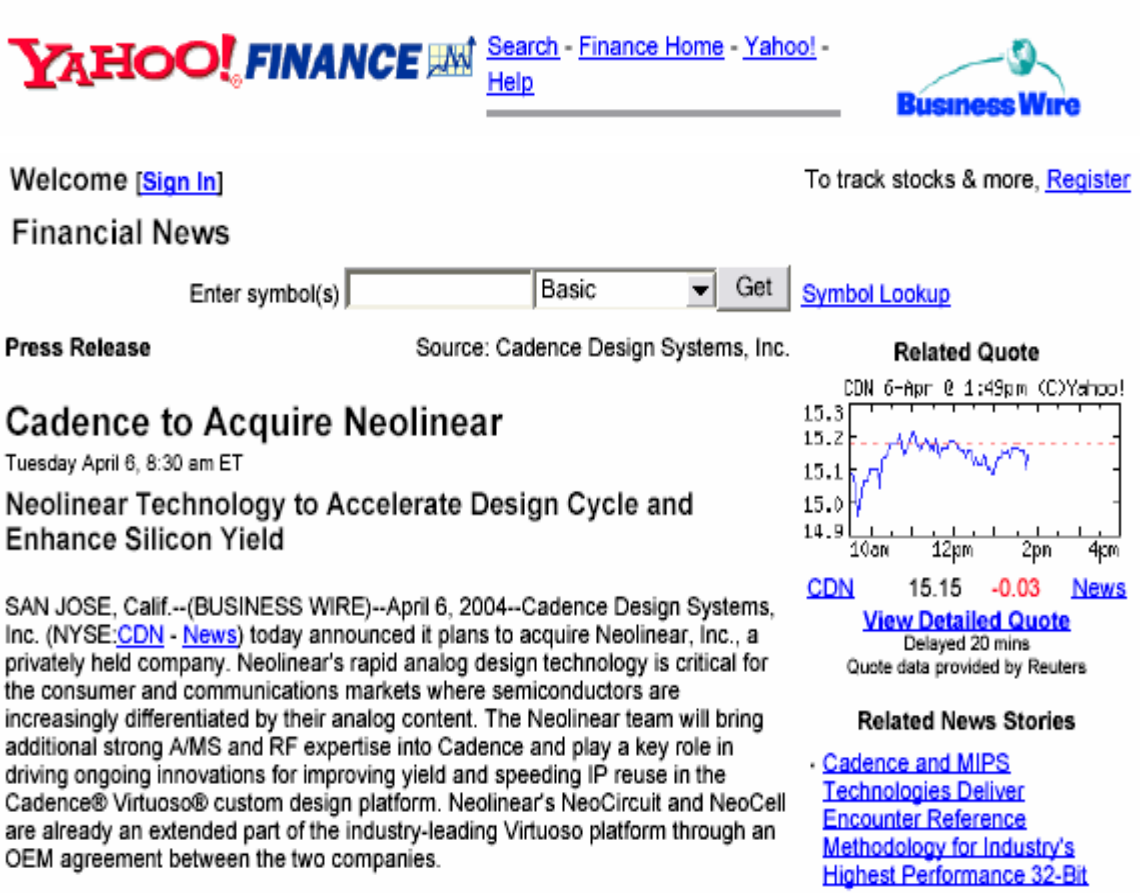
Bandgap I_{Ref}



Freq Detector



Aside: Analog Side is *Also* an Interesting Biz



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Press Release Source: Cadence Design Systems, Inc.

Cadence to Acquire Neolinear

Tuesday April 6, 8:30 am ET

Neolinear Technology to Accelerate Design Cycle and Enhance Silicon Yield

SAN JOSE, Calif.--(BUSINESS WIRE)--April 6, 2004--Cadence Design Systems, Inc. (NYSE:CDN - News) today announced it plans to acquire Neolinear, Inc., a privately held company. Neolinear's rapid analog design technology is critical for the consumer and communications markets where semiconductors are increasingly differentiated by their analog content. The Neolinear team will bring additional strong A/MS and RF expertise into Cadence and play a key role in driving ongoing innovations for improving yield and speeding IP reuse in the Cadence® Virtuoso® custom design platform. Neolinear's NeoCircuit and NeoCell are already an extended part of the industry-leading Virtuoso platform through an OEM agreement between the two companies.

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- **Biggest analog synthesis tools player**

Summary

- **Semiconductor IP is a critical part of how we design big chips**
  - Nobody has time to build every block they want from scratch
  - Want to be able to buy or generate the blocks we need
- **Digital IP**
  - Standard cell libraries, CPU cores, memory block generators are common
  - Soft vs hard IP is the big distinction. Unclear what tomorrow will look like
- **Analog IP**
  - Not nearly so mature, mostly hard IP today
  - Emerging tools to handle soft IP, still a research issue
- **Still a big, active research area, for both digital & analog**