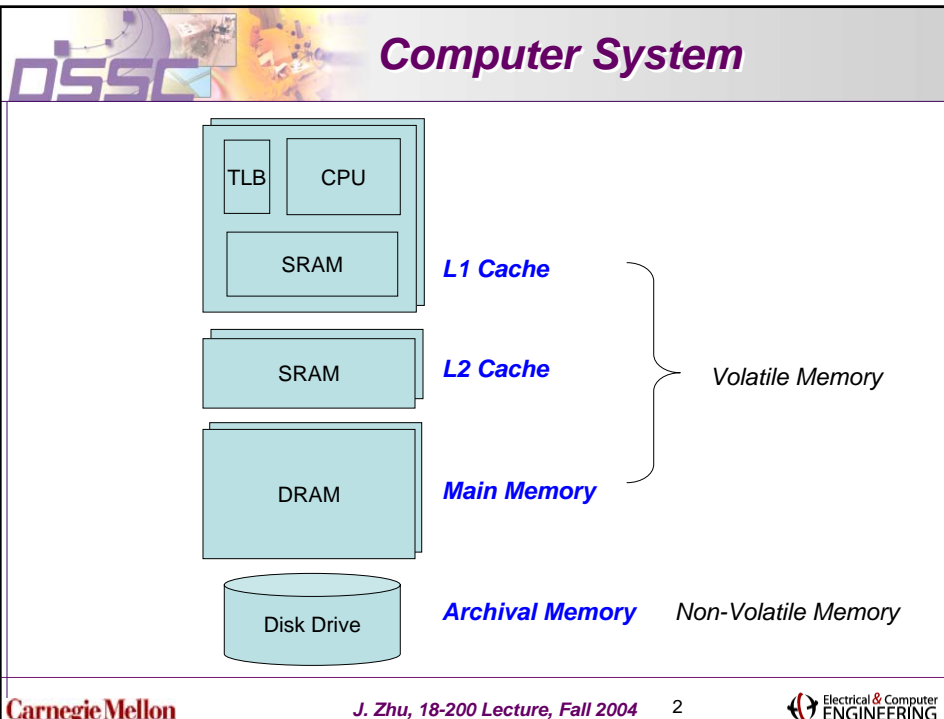



Magnetic Random Access Memory (MRAM)

Jimmy Zhu
ABB Professor in Engineering

Department of Electrical and Computer Engineering
Carnegie Mellon University

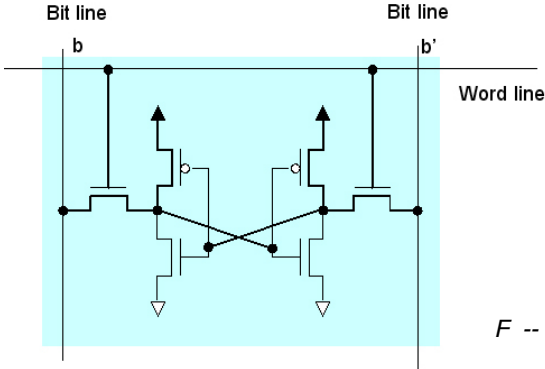




Static RAM (SRAM)

Cache Memory

6-Transistor CMOS SRAM




Fast:
Access time: $< 1 \text{ ns}$
 $= 10^{-9} \text{ second}$

Expensive:
\$100 / MByte


Low Density:
 $> 120 F^2$


F -- minimum fabrication feature size



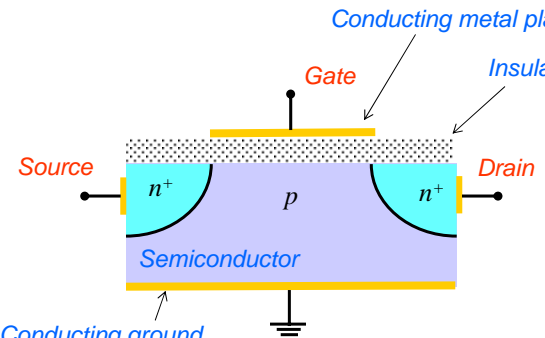
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3



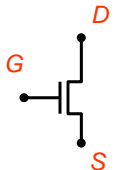


Field Effect Transistor (FET)




n-channel FET

MOSFET:
Metal-Oxide-semiconductor-FET




symbol



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4



How a FET Works: Transistor On

<http://www.pbs.org/transistor/science/info/transmodern.html>

Active condition:
 $V_{GS} > V_T$
 i.e. $V_{GG} > V_T$

n-channel FET

Drain current will be a function of gate voltage.

Legend: ● electron with charge $-e$

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How a FET Works: Transistor Off

Cutoff condition:
 $V_{GS} < V_T$
 V_T threshold voltage

n-channel FET

Zero Drain current.

Legend: ● electron with charge $-e$

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A Modern CMOS Process

The diagram illustrates the structure of a modern CMOS process. The top left shows a 3D schematic of a transistor with labels: Gate Oxide, Field Oxide, N+, P-Type, Source / Drain Regions, and Field Oxide. The top right shows a circuit symbol for an inverter with input V_{in} and output V_{out} , and supply voltage V_{DD} . The main part is a cross-sectional view of a Dual-Well Trench-Isolated CMOS Process, showing layers: gate-oxide, Tungsten, TiSi₂, AlCu, SiO₂, poly, n-well, p-well, n+, p-epi, p+, and SiO₂.

Dual-Well Trench-Isolated CMOS Process

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Dynamic RAM

The diagram illustrates the structure of Dynamic RAM. It shows a cross-sectional view of a trench capacitor with labels: Poly-silicon word line, Metal bit line, Source and Drain regions, and Trench capacitor. To the right is a photograph of a DRAM array center with labels: DRAM ARRAY CENTER, D5188 189, 84233C820X+VL01BD, 000041 2.5 kV X7.

Main Computer Memory

- Individual access time 60 ns
- 10 F²
- \$4 /MByte
- All "1"s need to be refreshed every 1 ms.


State "1" $V = \frac{Q}{C}$

State "0" $V = 0$


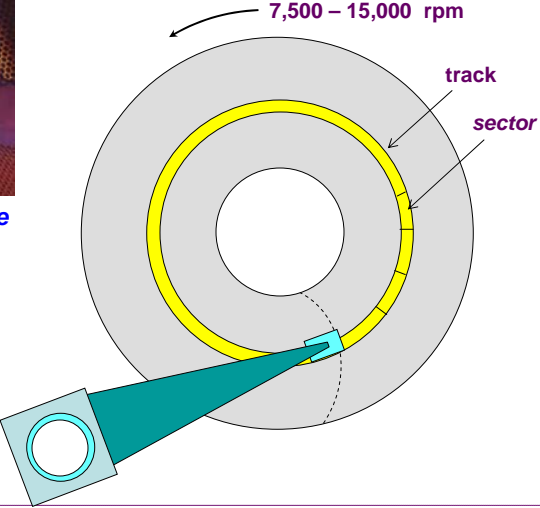
Bit line

Word line

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Rotational Latency

Inexpensive: \$0.001/1MByte


Rotational Latency


- Average latency: 3 – 6 ms
- Wait until desired sector passes under head
- Worst case: a complete rotation
 - 7,500 rpm = 8 ms
 - 15,000 rpm = 4 ms



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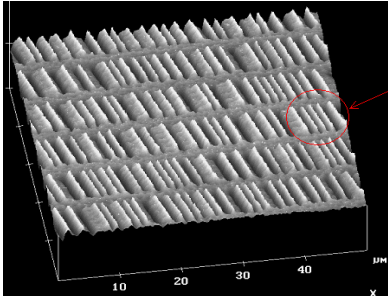
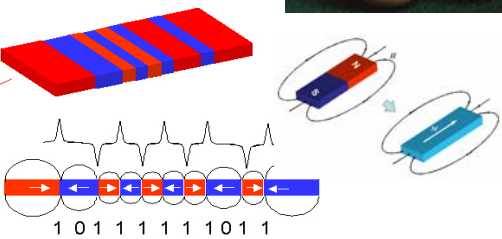






Hard Disk Drives

18-316 Introduction to Data Storage

18-517 Data Storage Systems Design






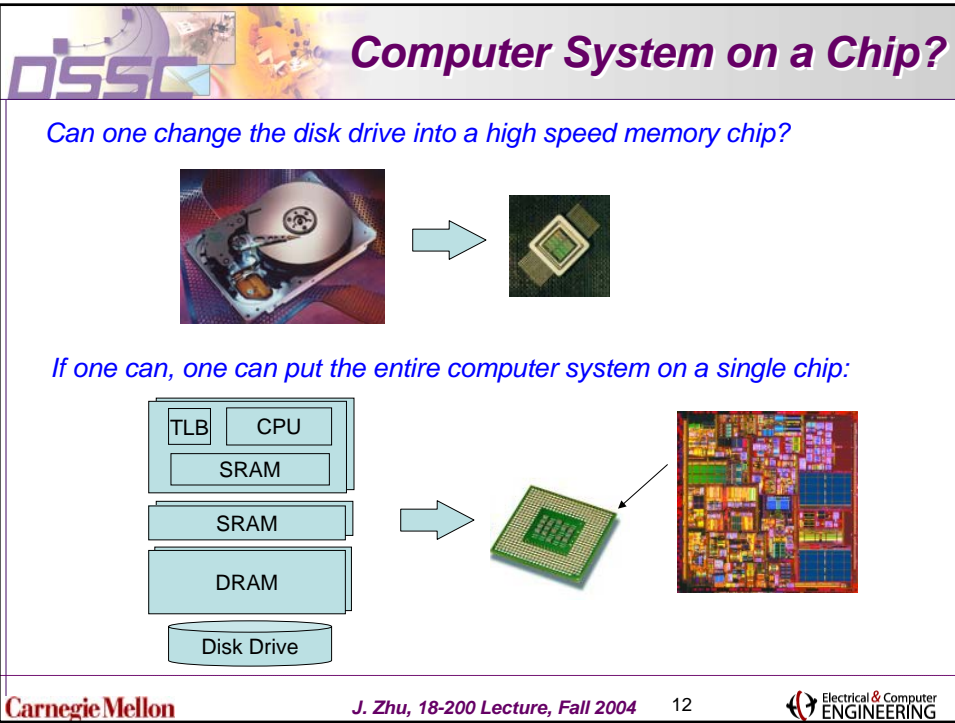
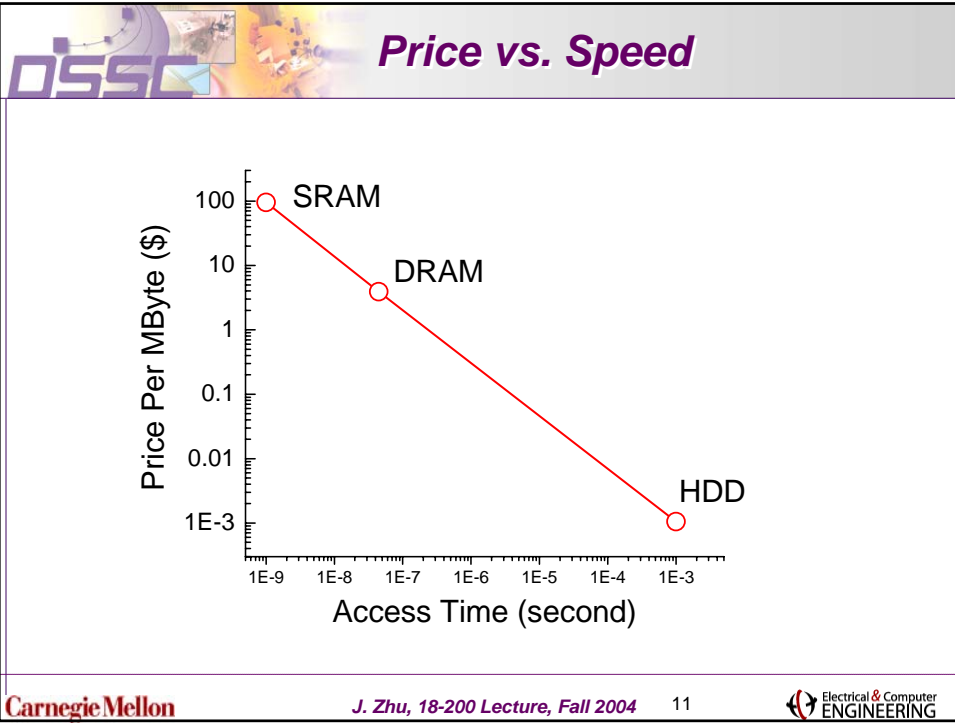
Magnetic Force Microscopy Image of A Disk Surface



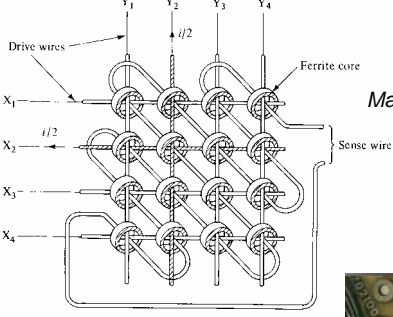
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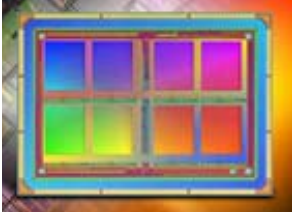




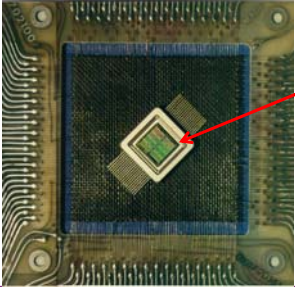
Magnetic RAM: Historical Perspective



Motorola
4Mbits MRAM Chip
Magnetic tunnel junction
2003



Honeywell
16Kbits MRAM Chip
AMR Technology 1994

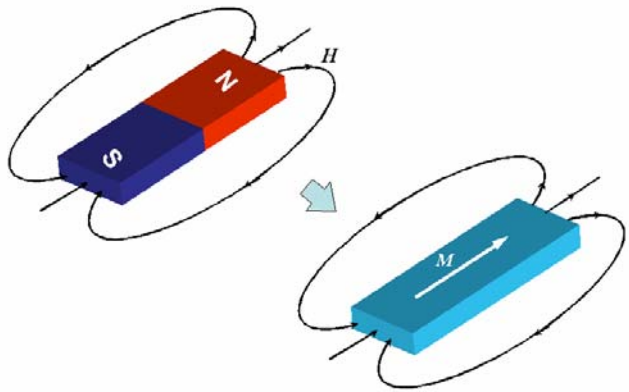


Control Data Corp.
1Kbits Ferrite Core Memory
1965


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Remember Magnet !

Magnetic moment can maintain its direction without power !

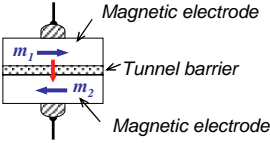


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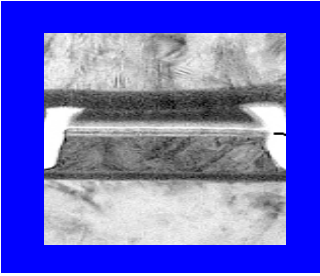


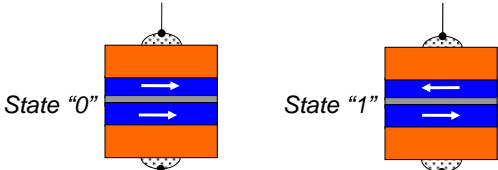
Memory Element

Magnetic Tunnel Junction (MTJ)

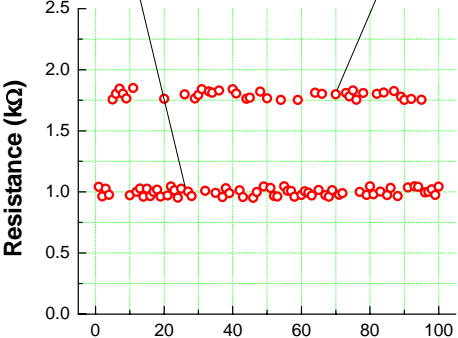


CoFe/Al₂O₃ (7-20Å)/Co






State "0" State "1"




Resistance (kΩ)


Data Bits



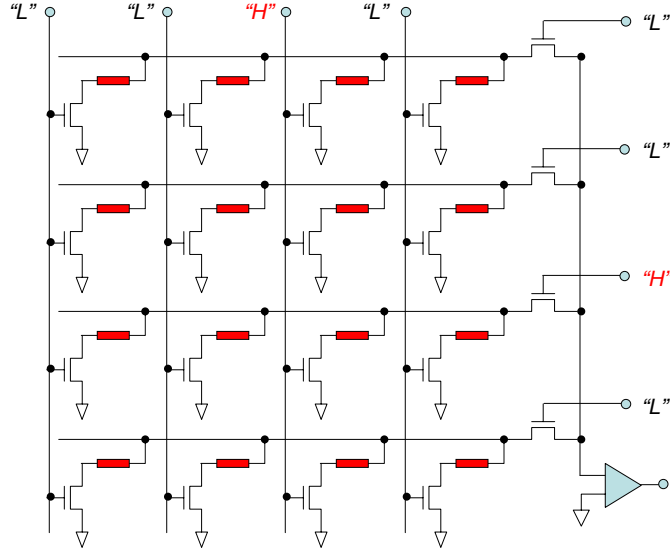
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Memory Array




"L" "L" "H" "L"

"L"

"L"


"H"

"L"



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DSSC **Detailed Structure**

The diagram shows two cross-sectional views of a magnetic tunnel junction. The layers from top to bottom are: storage layer (orange), Al_2O_3 tunnel barrier layer (grey), reference layer (blue), Ru 8Å (purple), flux compensation layer (green), and antiferromagnetic layer (orange). In State "0", the magnetic moments in the storage and reference layers are parallel (pointing right). In State "1", the magnetic moment in the storage layer is antiparallel to the reference layer (pointing left). A bracket on the left indicates that the magnetic moments in the reference, Ru, flux compensation, and antiferromagnetic layers are fixed.

Labels for the layers:

- storage layer
- Al_2O_3 tunnel barrier layer
- reference layer
- Ru 8Å
- flux compensation layer
- antiferromagnetic layer

Magnetic moments are fixed.

Only the magnetic moment of a storage layer is switched back and forth.

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DSSC **Writing Bits**

The diagram illustrates the writing mechanism. On the left, a 3D view shows a current I flowing through a wire and a magnetic field \vec{H} generated by the current. Below it is a 2D view of the magnetic field lines forming concentric circles around the wire. On the right, two cross-sectional views show the resulting magnetization states. State "0" is achieved with current I flowing out of the page (\odot), resulting in a magnetization \vec{M} pointing right. State "1" is achieved with current I flowing into the page (\otimes), resulting in a magnetization \vec{M} pointing left. A hysteresis loop graph at the bottom right shows magnetization M versus magnetic field H , with State "1" at the top and State "0" at the bottom.

State "0" $\odot I$ State "1" $\otimes I$

\vec{M} \vec{M}

State "1" M H

State "0"

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X-Point Addressing

The diagram illustrates the X-Point Addressing mechanism. On the left, a 3D view shows a bit cell structure with three horizontal layers (purple) and three vertical layers (orange) forming a central point. Currents $I_{write,x}$ and $I_{write,y}$ are applied to these layers. A transistor for read addressing is also shown. On the right, a 2D view shows the current flow through half-select elements, with current I flowing in opposite directions through adjacent lines. Below this, a graph plots the Y-Component Field (H_y) against the X-Component Field (H_x). The resulting field is a four-lobed shape centered at the origin, with the equation $H_z^{2/3} = H_x^{2/3} + H_y^{2/3}$ shown. The axes range from -1.0 to 1.0.

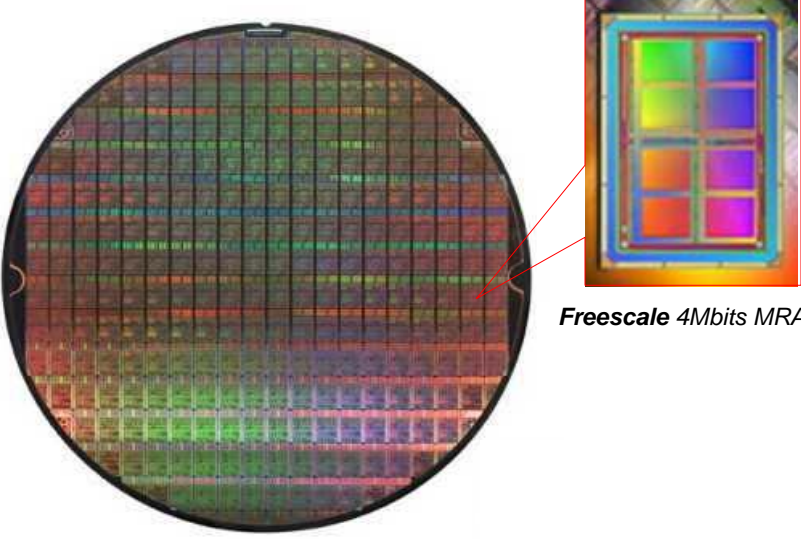
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MRAM Cell

The diagram shows a detailed cross-section of an MRAM cell. A Bit Cell is defined by a Word Line and a Bit Line. The structure includes a Silicon Substrate with N+ regions, a central S region, and D regions. The stack consists of layers M1, M2, M3, M4, and M5. A Bit Junction (BJ) is formed by M1, M2, and M3. A Magnetic Tunnel Junction (MTJ) is formed by M4 and M5. A Digit Line and Ground Line are also shown. A legend at the bottom identifies the layers: M1-3 (red brick), Via (cross-hatch), M4 (yellow brick), BC (blue brick), MTJ (blue grid), and M5 (blue diagonal lines). An inset image shows a microchip with the text "ERSOITRI" and another inset shows a close-up of metal layers labeled Metal 2, Metal 3, and Metal 4.

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DSSC **4 Mbits MRAM Chip**



Freescale 4Mbits MRAM Chip

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DSSC **MRAM: Dream Memory?**

Advantages of MRAM:

- ✓ **Nonvolatile** (No power needed to maintain memory states)
- ✓ **SRAM Speed** (~ 1 nanosecond)
- ✓ **DRAM Density** (~ 20 F²)
- ✓ **Endurance** (Infinitely rewritable)

MRAM has the potential to be an universal memory to replace SRAM, DRAM, FLASH, and disk drives in some applications to become the

Universal Solid-State Memory!

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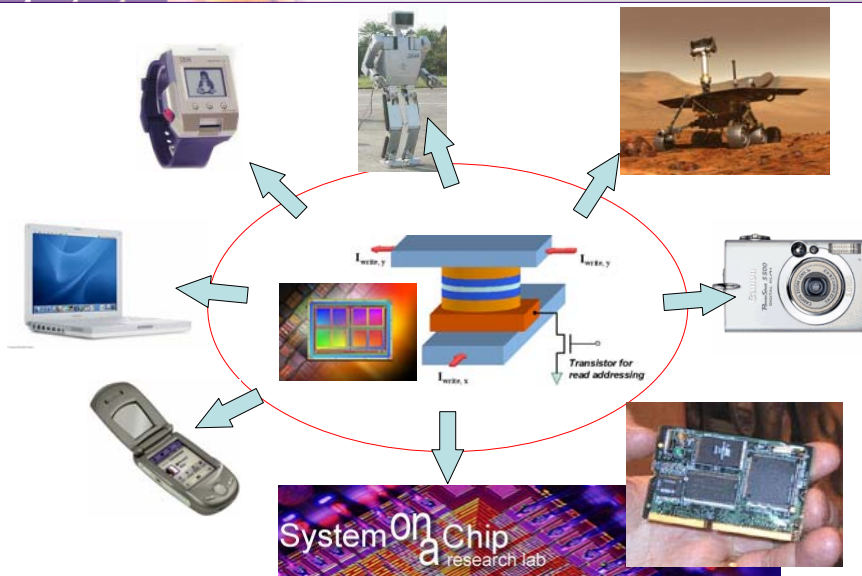
DSSC **A Potential Game Changer**

If MRAM replaces SRAM, DRAM or even disk drives:

- Instant on systems: No booting from disk drive
- Minimum stand-by power (Turn it off!)
- Enable computer system to be integrated on a single chip!

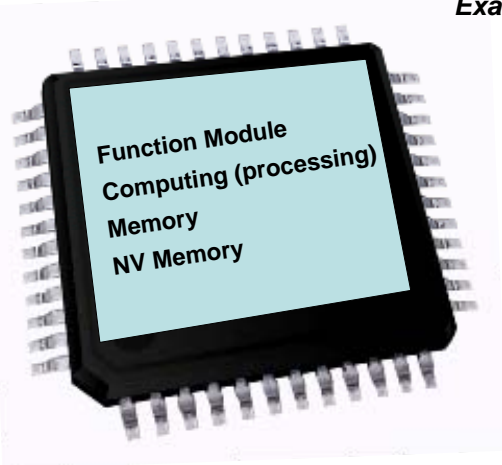


DSSC **Applications**



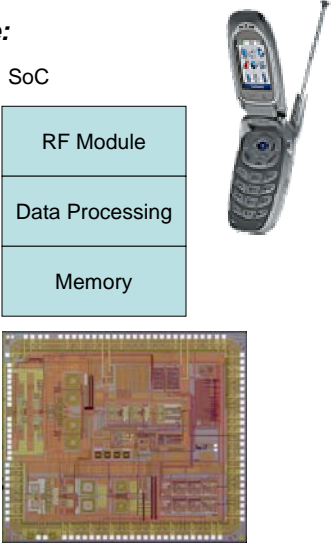
System on Chip (SoC)

Example:

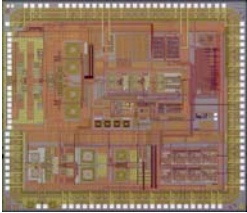


Function Module
Computing (processing)
Memory
NV Memory

SoC



RF Module
Data Processing
Memory




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MRAM: Dream Memory?

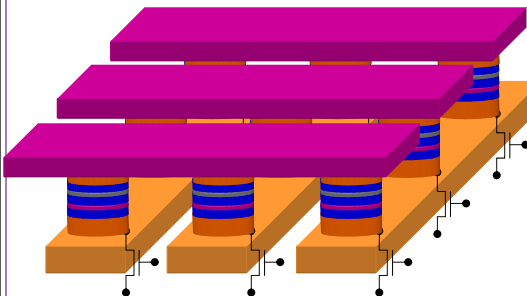
Present MRAM Technology Shortfalls:

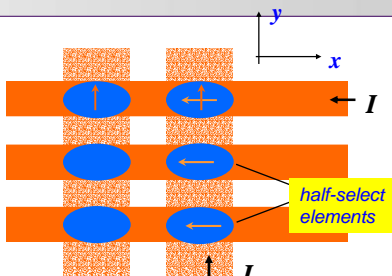
- *Relatively high power dissipation (high current)*
- *Down-size scaling not clear (thermal magnetic stability)*

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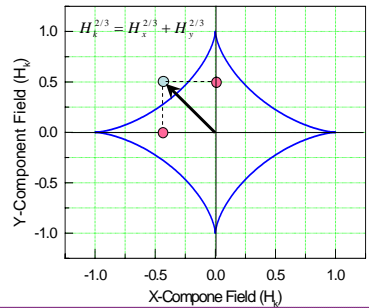
X-Point Addressing






half-select elements

99.999% of power is dissipated as I^2R on the write lines!




Y-Component Field (H_y)


X-Component Field (H_x)



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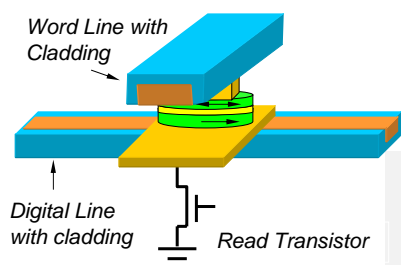
27





Magnetic Cladding

(18-303 Electromagnetics)

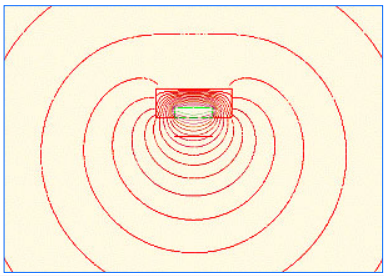


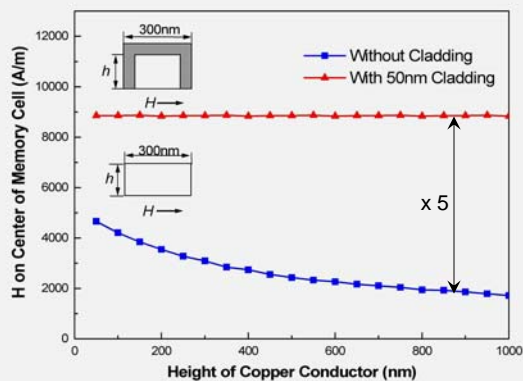
Word Line with Cladding

Digital Line with cladding

Read Transistor


➤ **The main power consumption arises from the ohmic dissipation, I^2R , in word/digital lines.**






H on Center of Memory Cell (A/m)

Height of Copper Conductor (nm)



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Thermally Activated Reversal

$H_x = 0.8H_x^0$

$\tau_{\text{rise}} = 0.3 \text{ ns}$

2 ns

Angle

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The Potential Universal Memory

	SRAM	DRAM	Disk Drive	FLASH	MRAM
Speed					
Density					
Cyclability					
Cost					
Non-volatility					
Power consumption					

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DSSC *Conclusions*

MRAM: The enabling technology for computer systems on a single chip!

Only Continued Innovation Will Ensure Future Competitiveness of MRAM

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DSSC *Data Storage Systems Track*

```

graph TD
    18-220 --- 18-303
    18-220 --- 18-316
    18-303 -.- 18-316
    18-303 --- 18-715
    18-316 --- 18-517
    18-396 --- 18-517
    18-517 --- 18-715
    18-715 --- 18-716
  
```

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18-517
Data Storage Systems Design

Building a Virtual Disk Drive using MATLAB/SIMULINK

Data to be recorded

Retrieved signal

Equalizer

Recovered data

Detector

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18-315 Fall 2004

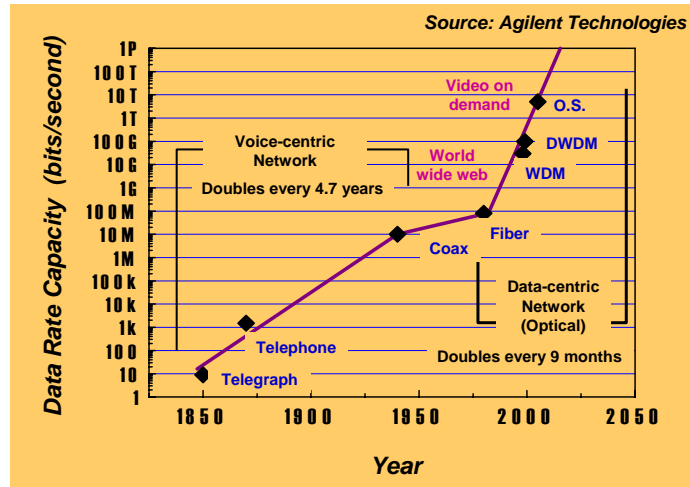
Introduction to Optical Communication Systems

Professor Jimmy Zhu
jzhu@ece.cmu.edu

Course Objective:
Provide a basic understanding of present optical communication systems and components, as well as future engineering challenges.



Bandwidth Explosion



Facts

A single optical fiber is capable of transmitting 2×10^{12} bits of data per **second**, which is equivalent to

simultaneously carry more than **30,000,000** phone conversations, or

200,000 users download (upload) information at **10 Mbits/second** data rate at same time, or

download all **380** CDs (each with 1 hour long music) in **1 second**, or

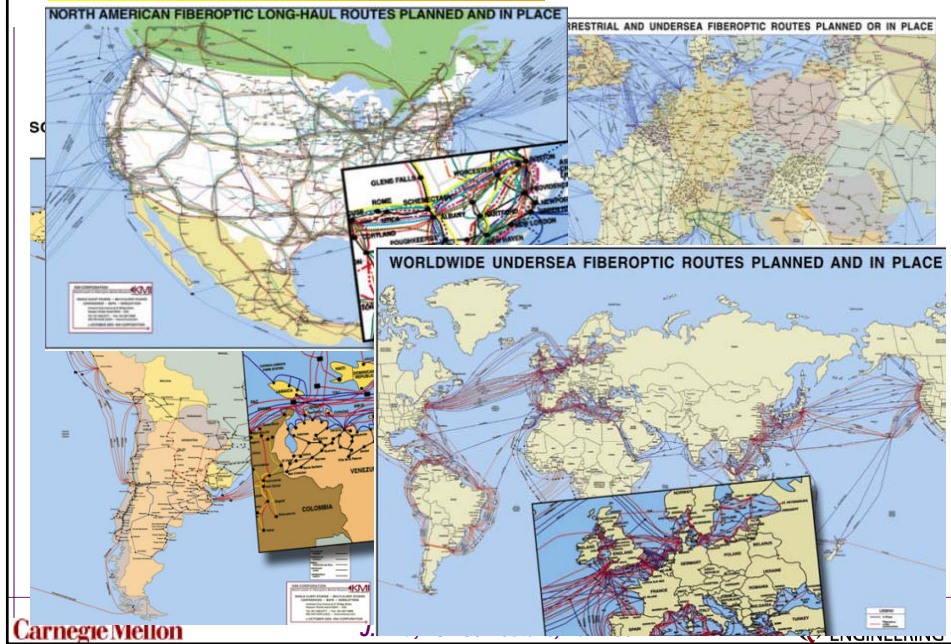
download **30** DVD movies in **1 second**.

Present dense wavelength division multiplexing (DWDM) technology is realizing the full potential of a single optical fiber !

A optical fiber cable may contain up to 200 fibers.

Fiber-Optical Long-Haul Routes

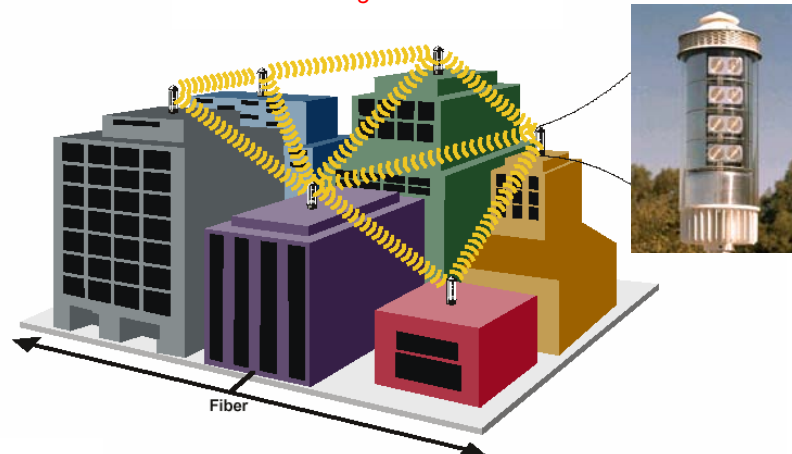
Source: KMI



Metro Optical Network

Source: Nortel Networks

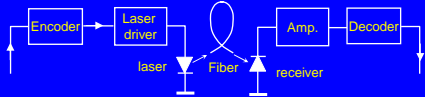
e.g. 10 Gbits Ethernet



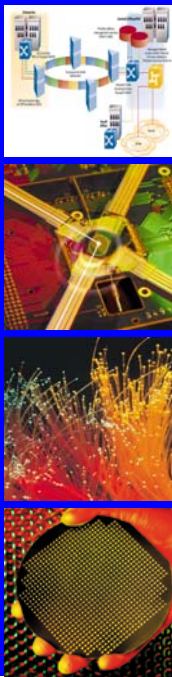



The optical wireless solution consists of a mesh network of short optical links that extend the fiber loop wirelessly to buildings outside the established fiber network.

18-315 Introduction to Optical Communication Systems

Course Coverage



- Light
 - ✓ How light carries information
 - ✓ Generation of light
 - ✓ Light traveling in a fiber
 - ✓ Amplification of Light
- Systems
 - ✓ Time Division Multiplexing (TDM)
 - ✓ Wavelength Division Multiplexing (WDM)
 - ✓ Optical networks
- Devices and Components
 - ✓ Fiber
 - ✓ LED
 - ✓ Semiconductor lasers
 - ✓ Fiber Amplifiers
 - ✓ Optical receivers
 - ✓ Optical modulators
 - ✓ Optical couplers and switches

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Careers

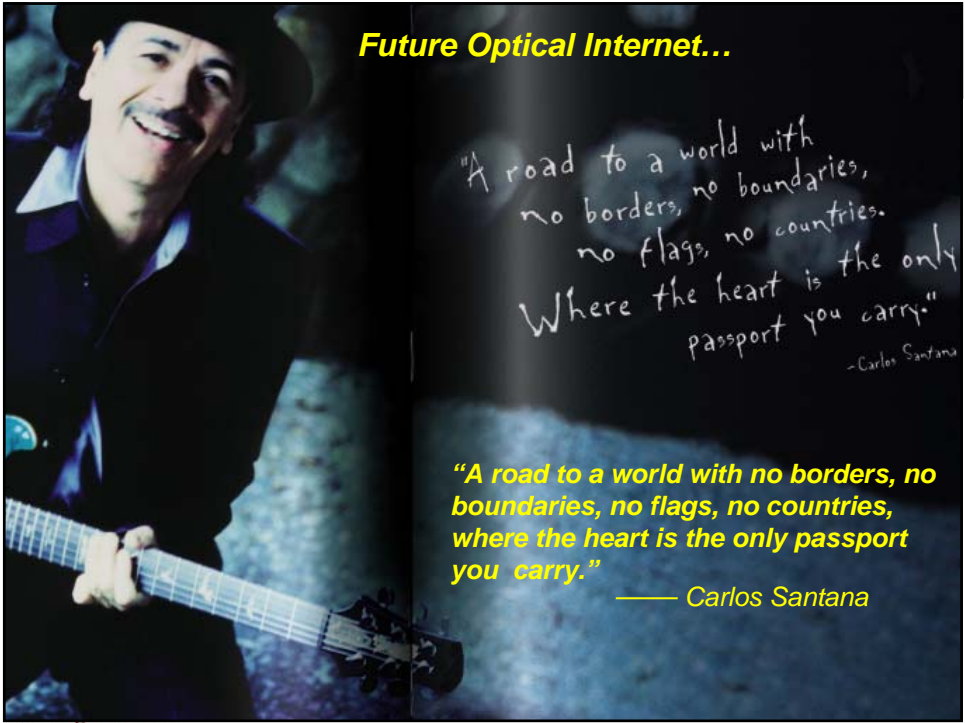




This course is designed to:

- ▶ prepare students with up-to-date education ready for the optical communication and network industry.
- ▶ Provide students sufficient background knowledge for further career development in optical communication systems and networks.
- ▶ Stimulate students' ability for innovation.
- ▶ Train students' problem analyzing and problem solving abilities.

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Future Optical Internet...

"A road to a world with
no borders, no boundaries,
no flags, no countries.
Where the heart is the only
passport you carry."
-Carlos Santana

**"A road to a world with no borders, no
boundaries, no flags, no countries,
where the heart is the only passport
you carry."**
— Carlos Santana