

SOI-CMOS-MEMS Electrothermal Micromirror Arrays

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**Dedicated to my wife Elizabeth and my daughters Corinna, Vivienne and Xanthe.
Their love and patience made this possible.**

**“Story telling ... is about the remembering, making and sharing of images that bind together
time, nature and people. ... [Stories] remind us that we do not stand alone”**

- Joan Halifax

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Abstract

A fabrication technology called SOI-CMOS-MEMS is developed to realize arrays of electrothermally actuated micromirror arrays with fill factors up to 90% and mechanical scan ranges up to $\pm 45^\circ$. SOI-CMOS-MEMS features bonding of a CMOS-MEMS folded electrothermal actuator chip with a SOI mirror chip. Actuators and micromirrors are separately released using Bosch-type and isotropic Si etch processes. A 1-D, 3 x 3 SOI-CMOS-MEMS mirror array is characterized at a 1 mm scale that meets fill factor and scan range targets with a power sensitivity of $1.9 \text{ deg}\cdot\text{mW}^{-1}$ and $-0.9 \text{ deg}\cdot\text{mW}^{-1}$ on inner and outer actuator legs, respectively. Issues preventing fabrication of SOI-CMOS-MEMS micromirror arrays designed for 1-D and 3-D motion at scales from $500 \mu\text{m}$ to $50 \mu\text{m}$ are discussed.

Electrothermomechanical analytic models of power response of a generic folded actuator topology are developed that provide insight into the trends in actuator behavior for actuator design elements such as beam geometry and heater type, among others. Adverse power and scan range scaling and favorable speed scaling are demonstrated. Mechanical constraints on device geometry are derived. Detailed material, process, test structure and device characterization is presented that demonstrates the consistency of measured device behavior with analytic models.

A unified model for aspect ratio dependent etch modulation is developed that achieves depth prediction accuracy of better than 10% up to $160 \mu\text{m}$ depth over a range of feature shapes and dimensions. The technique is applied extensively in the SOI-CMOS-MEMS process to produce deep multi-level structures in Si with a single etch mask and to control uniformity and feature profiles.

TiW attack during release etch is shown to be the driving factor in mirror coplanarity loss. The effect is due to thermally accelerated etching caused by heating of released structures by the exothermic reaction of Si and F. The effect is quantified using *in situ* infrared imaging. Models are developed that predict suspended device temperatures based on a power balance model using a single parameter, the proportion of etch heat carried away by volatile species, as the sole fitting parameter.

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Symbols and Abbreviations

<u>Symbol</u>	<u>Description</u>
$\{\bullet\}$	a set
$[\bullet]$	a vector
*	wildcard
α	coefficient of thermal expansion
β_m	m^{th} eigenvalue of a series solution to a differential equation
γ	electrothermal actuator thermal sensitivity
Γ	flux
δ	atomic, molecular or particle diameter
ΔH	change in enthalpy, or heat of formation of a chemical compound
ΔT	temperature difference with respect to some reference temperature
Δw	CD bias, i.e. actual width - layout width following release etch
Δy	width of a beam member in multimorph formulae
Δz	thickness of a beam member in multimorph formulae
ε	mechanical strain
ε_{IR}	infrared emissivity
ε_0	permittivity of free space
ζ	dimensionless axial coordinate
η	dimensionless radial coordinate
θ	angular displacement
θ_{sa}	angular self-assembly displacement
θ_{th}	thermally induced angular displacement
Θ	normalized angular displacement
κ	thermal conductivity
λ	fractional resistor placement in an electrothermal actuator
λ	mean free path
μ	mean
μ_p	microloading
ν	Poisson's ratio
ξ	Causing's simplification constant for vacuum conductance correction factor

ρ	cylindrical coordinate direction, or radial distance from a structure origin
ρ_c	radius of curvature of a structural element
ρ_d	material mass density
ρ_p	resistivity of embedded polysilicon film
σ	mechanical stress
σ_{SB}	Stefan-Boltzmann constant
σ_{ion}	collision cross-section of an ionic species in a plasma
τ	time
τ_{win}	window transmission in the context of IR imaging
υ	proportion of exothermic reaction heat absorbed by an etching structure
ϕ	azimuthal angle in a cylindrical or polar coordinate system
χ	ratio of limiting cases of ion driven and spontaneous thermal etching
ψ	sidewall profile angle of an etched feature
Ω_a	array pitch, the distance between equivalent points on adjacent devices in an array
a	plasma etch microloading scaling factor
A	Arrhenius' pre-exponential factor
AR	aspect ratio, depth:characteristic dimension, or length:width
$A_{surface}$	area of a surface, the subscript denotes the surface
b	length to width ratio of a rectangular feature
c	molar volume density
C	coefficients of fitted functions and general ODE solutions
C_p	heat capacity at constant pressure
C_{th}	thermal capacitance
$cond(\mathbf{M})$	condition number of matrix \mathbf{M}
d	diameter or characteristic dimension, specified in context
D	etch depth
D_{X-Y}	co-diffusivity of species X and Y in a mixture of both
e	enclosure of a structure by another structure in a physical layout
\mathbf{E}	vector of Young's moduli
E_A	activation energy
$(EI)_{eff}$	effective flexural rigidity
$E_{material}$	Young's modulus of a given material

E^{material}	biaxial modulus of a given material
ER_{mat}	etch rate of a given material
f	frequency
F	force
$f(\text{vars})$	a function of one or more variables
FF	fill factor, ratio of the functionally active area of a device to total device area
g	gap, or space, between two structural elements
g_{cam}	IR camera gain
$g_{\text{e}}(M_{\text{p}}; r; \theta)$	fitted function for the etch rate dependence on M_{p} , r and θ
h	generalized transport coefficient, exact definition depends on context
H	perimeter
i	an index
j	an index
k	an index
K	the probability that a particle passing through the orifice of a structure will reach the bottom of the structure
K'	first order chemical reaction rate constant
K''	second order chemical reaction rate constant
k_{B}	Boltzmann's constant
k_{coord}	spring constant of a structure for displacement in a given coordinate direction
$\mathbf{k}_{\text{coord}}$	vector of structure spring constants for displacement in a given coordinate direction
K_i	one of a series of constants
K_{n}	Knudsen number
k_x	spring constant for bending in the x -direction
k_y	spring constant for bending in the y -direction
k_z	spring constant for bending in the z -direction
l	length
L	physical layout function
m	mass, or eigenfunction index, depending on context
M_{source}	bending moment due to a particular source
M_{p}	etch macroloading
N	total count of a quantity or element

N_A	Avogadro's number
$N(\beta_m)$	norm of an eigenfunction corresponding to the m^{th} eigenvalue β_m
N_m	number of materials in the JAZZ 0.35 μm SiGe BiCMOS process
o	overlap of one layer by another layer
p	pressure
P	power
\tilde{P}	heat power dissipation density
q	electronic charge
Q_G	heat generation rate per unit volume
Q_L	heat sink rate per unit volume
r	radius, or radial distance from a defined structure origin
R	resistance
Ra	average roughness
R_c^2	least squares regression correlation coefficient
R_G	gas constant
RH	relative humidity
sd	standard deviation
S	reaction probability
S'	approximation to the true reaction probability based on fitting to experimental data
S_{XY}	etch selectivity of material X over material Y
t	thickness
T	temperature
T_{member}	geometric coefficient defining the contribution of a member of a multimorph beam to the spring constant of the beam
\mathbf{T}	matrix of geometric coefficients relating spring constants and Young's modulus
u	undercut
U	process uniformity, or range normalized to the average process output
v	velocity
V	voltage
w	width
W	microloading impulse response
x	coordinate direction, displacement in the x -direction, or a fractional quantity

y	coordinate direction, displacement in the y -direction, or a fractional quantity
y_{sa}	self-assembly displacement of a released beam
y_{th}	thermally induced displacement of a released beam
z	coordinate direction, or displacement in the z -direction
z_{sa}	vertical self-assembly displacement of a released beam
z_{th}	vertical thermally induced displacement of a released beam

<u>Abbrev.</u>	<u>Description</u>
1-D	1 dimensional
2-D	2 dimensional, can refer to translational or rotational degrees of freedom
3-D	3 dimensional, can refer to translational or rotational degrees of freedom
AA	Active Area, the doped region of a CMOS design where there is no field oxide
AR	Aspect Ratio (i.e. depth:width, or length:width, depending on context)
ARDE	Aspect Ratio Dependent Etching
ARDEM	Aspect Ratio Dependent Etch Modulation (or Modulated, depending on context)
ARDP	Aspect Ratio Dependent Passivation
ASE	Advanced Silicon Etch
BC_i	Boundary Condition of the i^{th} kind
BHF	Buffered HydroFluoric acid
BOX	Buried OXide layer of an SOI wafer
CD	Critical Dimension
CMOS	Complementary Metal-Oxide-Semiconductor
CTE	Coefficient of Thermal Expansion
DIP	Dual In-line Package
DOF	Degrees Of Freedom
DRIE	Deep Reactive Ion Etch
DSP	Double-Sided Polished
DUT	Device Under Test
DWL	Direct Write Lithography
EM	ElectroMagnetic
ES	ElectroStatic
ET	ElectroThermal

FFT	Fast Fourier Transform
FIB	Focussed Ion Beam
FLIR	Forward Looking InfraRed, refers to a company and an IR detection method
FSD	Full Scale Deflection
GDP	Gas Distribution Plate
ICP	Inductively Coupled Plasma
ILD	InterLayer Dielectric
IR	InfraRed
JAZZ process	JAZZ Semiconductor's 0.35 μ m SiGe BiCMOS process
jz60_index	a specific JAZZ process run ex. jz60_024 is the 24th JAZZ process run
LSR	Least Squares Regression
m#	the metal layer in the structure, # = 1, 2, 3, or 4
m#(# -1)-ILD	interlayer dielectric between metal layer # and metal layer (# -1)
m1a	beam on active area with top layer metal 1
m1f	beam on field oxide with top layer metal 1
m4321pf	beam on field oxide with metal 4 top layer and metal 3, metal 2, metal 1 and poly internal layers
MEMS	MicroElectroMechanical Systems
PI	Principal Investigator
poly	any form of polySilicon - doped, undoped, silicided, unsilicided etc.
QIR	Quantum Infra-Red, typically in context of QIR microscope
ROI	Region Of Interest
RTD	Resistance Temperature Detector
SEM	Scanning Electron Microscope
SOI	Silicon On Insulator
STS	Surface Technology Systems
SUT	Structure Under Test

1

SOI-CMOS-MEMS: An Opening

“Believe nothing ... unless it accords with your own reason and your own common sense.”

- Siddhartha Gautama

Implicit in the Buddha’s admonition is the necessity to hone one’s intellect, expand one’s knowledge, deepen one’s insight, eliminate one’s ignorance and move beyond one’s existing preconceptions. Experience is the best means for cultivating the requisite state of mind in which this counsel leads to valid judgment. So, throughout this dissertation, a premium is placed on theory and analysis backed up by experimental data.

The exacting nature of MEMS provides a rigorous test of the correspondence between conception and reality and is one of its most alluring aspects. A device must be well-conceived, meticulously designed, deliberately fabricated and insightfully tested, or, by its failure, bring into stark relief the opportunity for deeper learning and the potential for further improvement. And so it must be done: education must be wielded, pen put to paper, fingers to keyboards, wafers to equipment, die to packages and probes to pads to gain the experience that bestows valid judgment.

1.1 Micromirror Applications

Optical MEMS comprise lenses, gratings, single mirrors and mirror arrays. The work described here focuses on micromirror arrays actuated electrothermally. To introduce the topic, these devices are placed in the context of their position in the application space.

With the exception of lenses, optical MEMS components make use of their reflective effect on light. The reflective components were first investigated in the late 1960's and 1970's as arrays for use in displays [1][2] and as spatial light modulators (SLMs) [3] with the goal of using SLMs as the enabling component in coherent optical computing [4]. In these early devices, the reflective elements were deformed by electrostatic force. By the late 1970's, Si was demonstrated as a suitable material for fabrication of optical MEMS [5] and the first rigid mirror with flexible springs was reported [6], thus opening the way for the on-chip integration of reflective elements and electronics [7] that ultimately led to the extremely successful Digital Light Processing (DLP) chip from Texas Instruments [8].

SLMs are high density arrayed devices (characterized by fill factor $FF = \text{reflective area}/\text{pitch}^2$) either in a row-column matrix of mirrors with small full scale deflection ($FSD < 10^\circ$) [8] or as a linear array of reflective elements forming a deformable grating that requires rastering in the image plane [9]. In each case, the array element dimensions are on the order of the wavelength of the incident light and the speed of operation must be a minimum of video rate (i.e. 30 Hz) for square arrays, or, for linear arrays, a factor of the orthogonal array dimension higher in speed to account for rastering. The main application area for SLMs is in projection display technologies, like TI's DLP, which are being scaled into personal space [10] and extended to autostereoscopic displays [11]; however, SLM-type devices are also used for adaptive optics and scanning. In adaptive optics, known aberrations in electromagnetic wavefront are compensated by small variations in phase difference between different elements in the SLM [12] or, conversely, regular wavefronts are shaped to suit a particular function [13]. In SLM scanners [14], the SLM acts as a phased array or makes use of higher diffraction orders to achieve fast, small angle deflections ($\sim 3^\circ$). A SLM projection technology currently generating a lot of commercial interest is maskless lithography [15], where costly reticles are replaced by SLMs that hold the lithographic pattern. Not only are expensive reticles eliminated by maskless lithography but the manufacturing time lost in retooling expensive lithography equipment with new reticles is recovered to production.

At the other end of the optical MEMS application space are scanning applications such as biomedical imaging [16][17] and laser beam deflection [18]. The optically active component in these scanning applications is typically a rigid mirror with dimensions on the order of the width of the incident light beam (\sim mm). SLM-type scanners are not typically suitable for these applications because of their relatively small scan angles. The goal in single element devices is to have large deflection angles ($>10^\circ$) and large mirrors (\sim mm). These characteristics provide large scanned areas for a single device position and low signal loss. Single mirror display systems have also been demonstrated [19] and are now entering the market [20].

Between the mm-scale single mirror scanners and the μ m-scale mirrors arrayed in SLMs are optical networking applications, such as optical cross-connects (OCX) and wavelength-division multiplexers (WDM) [21]. Devices in this space are arrayed reflectors that require large scan angles to enable large channel counts but smaller mirrors ($\sim 100 \mu$ m) are acceptable because the free-space distance travelled by beams between reflective elements is typically at mm-scale [22].

A rich application space for single and arrayed micromirrors is illuminated in this sub-section and illustrates the opportunities available for a scalable device topology with the performance to span the space. This dissertation covers the development of a fabrication technology to realize high fill-factor mirror arrays starting at pitches of 1 mm with large deflection angles that can meet the needs of scanning applications and goes on to explore the scaling of the fabrication technology to meet the needs of optical network applications and ultimately SLMs. In the following sub-sections of this chapter the various actuation methods and fabrication concepts available to meet these goals are introduced.

1.2 Micromirror Actuation

The literature on micromirrors contains a diverse set of actuation methods such as electrostatic [23][21][15][24][25][13][14], electromagnetic [26][27][28][19], electrothermal [29][17][30][31][16],

electrowetting [32][33], pneumatic [34] and piezoelectric [18][35][36][37][38]. Each actuation method has its advantages and disadvantages and is strongly coupled to the fabrication method in which the actuator is formed. This sub-section briefly introduces electrothermal actuation for micromirrors and compares and contrasts it with other actuation methods.

Electrothermal actuation applies the bending moment induced by the mismatched thermal expansion of the different materials in a composite beam [39]. It was introduced to the MEMS community as an actuation concept in the late 1980's [40]. Since that time, electrothermally actuated micromirrors have become the device topology of choice for large angle scanning applications in which speed is not a critical parameter. For example, Wu [29] recently demonstrated an electrothermal, double-sided SOI mirror with a 360° optical scan range for endoscopic imaging applications, thus ending the race to the greatest scan range for a micromirror device, but it can only operate at 60 Hz. The preeminence of electrothermal actuators in this domain is owed to the simplicity of their mechanism (mismatched thermal expansion), their ease of integration in a given fabrication technology (only two mechanical layers of differing thermal coefficient of expansion (CTE) and a release layer are needed) and their freedom from the constraints of a counter electrode (only a single electrically resistive layer is needed for heating). These factors, in contrast, limit the implementation of electrostatic, electromagnetic, piezoelectric, pneumatic and electrowetting actuated devices for large scan range applications.

Electrothermal devices are the benchmark in low voltage operation, whereby, with suitably chosen electrical resistances, FSDs are achieved with ≤ 10 V compared to electrostatic devices that typically require far in excess of this (ex. 40 - 70 V) to achieve smaller ($\leq 10^\circ$) FSDs [23][21]. Electrostatic actuation is at a disadvantage in operating voltage and scan range because of the counter electrode, which requires the electrode separation, and hence the scan range, to decrease in order to reduce the operating voltage. Some researchers have overcome the scan range limitation imposed by electrode separation through the use of vertical combdrives [23], but the problem of high voltage operation is typically exacerbated by this approach.

Traditionally, where electrothermal devices falter in comparison to mirrors with other actuation methods is in their low FF , which made arraying them an impractical proposition, their high power consumption, due to a relatively inefficient and inherently irreversible transduction method, and their speed, which is limited by the need for the thermal energy to dissipate to the surroundings through paths of varying thermal conductance in order for the device to return to rest.

Electrothermal actuators and the reflective surfaces they service are laid out in the same plane typically [17][16][31][30], such that the actuator dimension, the key feature for increasing scan range, detracts from the reflective area [17]. This issue has been overcome ingeniously by several electrostatic designs to the effect that $FF = 95\%$ is routinely achieved through the fabrication of actuator electrodes under the reflective surface [21].

Electrothermal devices depend on the dissipation of electrical energy through Joule heating in resistive layers at any actuation angle except rest, so there is a power penalty for holding a position that is not paid by electrostatic and piezoelectric devices, which dissipate power only during the times that they are charging and discharging. In this respect, when power consumption is a critical performance parameter and voltage and scan range constraints are loose, electrothermal actuation cannot compete with electrostatic actuation. To reduce power consumption, greater thermal isolation is needed, however the consequent reduction in thermal dissipation negatively impacts the speed of the device. This power-speed trade-off must be finely balanced and the final application of the device must be known to make appropriate decisions.

The challenge for electrothermal micromirrors is clear: maintain large scan angles and low actuation voltage levels while achieving FF , power consumption and speeds that approach electrostatic micromirror performance. The performance benchmarks electrothermally actuated micromirrors must match are shown in Table 1.1 through a performance comparison with devices from the literature in which other actuation methods are applied. This dissertation discusses how these benchmarks can be

achieved for electrothermally actuated micromirrors and explores how their performance scales to SLM dimensions.

TABLE 1.1 Performance comparison of mirrors using exemplary cases of various actuation types

Researcher / PI	Actuation Method	Mirror Size (μm)	Scan Range (degrees)	Fill Factor (%)	Voltage for FSD (V)	Speed (Hz)	Power (mW)
Tsai / Wu [21]	electrostatic	100 x 100	8.8	96	90	13900	NR
Wu / Xie [29]	electrothermal	800 x 800	110	16	12	60	~800
Yalcinkaya / Straube [19]	electromagnetic	1500 x 1500	33	20	NR	2000	NR
Kang / Kim [32]	electrowetting	10000 x 10000	8	85	105	15	NR
Werber / Zappe [34]	pneumatic	1000 x 1500	10	17	30	< 1	1000
Tani / Toshiyoshi [37]	piezoelectric	1000 x 2000	17	13	20	1500	NR

*NR = Not Reported

1.3 Micromirror Fabrication Technologies

A MEMS mirror actuation method and the fabrication technology used to form the actuator are strongly coupled. Electrostatic devices that employ parallel plate electrode topologies require at least two conductive layers separated vertically by an insulating layer and a release layer [21]. Electrothermal devices require only two materials of differing CTE, provided one is resistive, and a release layer [40]. Electrowetting or pneumatic devices require the placement of mirrors on liquid drops [33] and the formation of reflective surfaces on hermetically sealed cavities [34], respectively. Electromagnetic devices often require assembly of the mirror device with a permanent magnet or a solenoid to produce an external magnetic field [28][19]. Piezoelectric devices [37][38] present challenges in the integration of reflective and piezoelectric materials with structural materials such as Si or polymers. In each case, the integration of electronics with the actuator and the structure being actuated is desirable because it reduces system complexity and size, improves speed and eliminates losses that can occur

between chips. However, if the actuator fabrication technology is not compatible with the drive and sense circuitry they must be fabricated on a separate chip.

Fabrication methods such as CMOS-MEMS [17][31][41], CMOS compatible custom MEMS processes [8] and hybrids of custom post-CMOS processing and CMOS-MEMS [42] allow single chip solutions. In CMOS-MEMS and its variants, the interconnect layers, interlayer dielectric (ILD), and sometimes the Si substrate, play functional roles in the final MEMS devices. In products like the TI DLP [8][7], custom release materials and metallization are added in the backend of the CMOS process to produce large-scale integrated MEMS and electronic devices. An example of a hybrid device is the transfer bonding of MUMPS mirrors to CMOS chips that contribute the control circuitry to the system [42]. Following transfer bonding, the mirrors are released in a CMOS-compatible process.

Vertical electrostatic combdrives and electrothermal actuators are readily formed in CMOS-MEMS and hybrid processes [43]. Multiple metal layers are available separated by high quality oxide and a polysilicon, or poly, layer is available for use as a resistive layer. For CMOS-MEMS mirror devices, the reflective surface is formed from one of the interconnect metal layers which requires that the actuator and the reflective surface be formed in the same plane [17]. This limits FF to a maximum of $\sim 60\%$ which trades-off with mechanical robustness, i.e. if the mirror is large compared to the total device area, the suspension must be small and hence weak. Electrostatic devices with $FF > 90\%$ [21][8][42] achieve this level by placing the actuators under the reflective surface in a hidden-actuator topology, allowing the suspension stiffness to be maximized without adversely effecting reflective area.

A goal of the research described in this dissertation is to develop a CMOS-compatible fabrication technology that combines the benchmark scan range capability of electrothermally actuated devices with the FF performance of hidden-actuator electrostatic mirrors.

1.4 Dissertation Outline

This dissertation covers the scope of the performance challenge for electrothermal micromirror arrays and details the design and fabrication of devices using a CMOS-MEMS foundry technology platform. Fabricated electrothermal micromirror arrays are characterized and compared to analytic models to assess how closely the challenges are met. To facilitate conciseness in this text the symbols and abbreviations used herein are defined in “Symbols and Abbreviations,” on page xv. The reader is referred to this list.

The contributions made by this work to the body of knowledge in the fields of MEMS fabrication and electrothermal actuator design are presented in this dissertation. The major contributions are:

1. A hybrid CMOS-MEMS fabrication technology that enables the independent optimization of CMOS electrothermal actuators and payloads fabricated in other material systems,
2. A 90% fill factor array of electrothermally actuated 1 mm square mirrors with a 90° mechanical scan range at voltages less than 5 V and power consumptions less than 50 mW,
3. Models of folded electrothermal bimorph and multimorph actuators with discrete and distributed heaters that are consistent with the behavior of characterized devices and test structures,
4. A DRIE etch rate model that incorporates spatial, pattern-based and aspect ratio dependent etch variation and is validated to within 10% against test structures of various shapes and scales,
5. A power balance model of suspended MEMS temperature during plasma release etch and its validation using test structure data collected with *in situ* infrared imaging.

In Chapter 2, the principles of operation and the design of electrothermally actuated, large angle mirrors are discussed. Analytical equations and finite element analyses are presented to describe the scaling behavior of these devices for power and scan range.

Chapter 3 provides detailed technical information about a hybrid CMOS-MEMS fabrication technology called Silicon-On-Insulator (SOI)-CMOS-MEMS used to achieve the performance benchmarks of high fill factor and high scan range. It covers the fabrication of the mirrors and the design and fabrication of a carrier chip needed to enable mirror FSD angles. CMOS processing is not discussed and it is assumed that a diced CMOS chip is the starting substrate.

The extensively used fabrication technique of Aspect Ratio Dependent Etch Modulation (ARDEM) is presented in Chapter 4. The theoretic foundation for this technique is established based on the literature and the plasma regime is determined to demonstrate the validity of the derived models of etch depth variation with feature size. The derived models are validated against experimental data collected from test structures and used to generate masks for use in SOI-CMOS-MEMS processing.

Chapter 5 discusses the issue of process driven selectivity and anisotropy loss that adversely impacts the electrical performance of large area released structures. The problem is shown to have its root in the increased temperatures that arise on the suspended structures during release etch due to their evolving thermal isolation. The temperatures of disc test structures during the release etch process are presented and used to fit a power balance model comprising power input from ion bombardment and reaction heat and power loss from suspension thermal conduction and radiation.

Chapter 6 presents experimental data showing the performance of the fabricated micromirrors and actuators along with key test structures for thermal sensitivity, Young's modulus and thermal coefficient of expansion. Micromirror performance data for 1 mm x 1 mm mirrors is given. Due to fabrication scaling issues micromirrors at smaller scales were not available for testing; however, actuators for 3-D mirrors on a 500 mm pitch and 1-D mirrors on 100 mm and 50 mm pitches are presented.

Chapter 7 discusses the impact of this work and the directions that can be followed to explore the design and fabrication space for arrays of electrothermally actuated mirrors.

2

Electrothermally Actuated Mirror Design and Operation

“If I had eight hours to chop down a tree, I’d spend six hours sharpening my ax.”

- Abraham Lincoln

The design of MEMS requires a mind open to the exploration of many scientific disciplines, appreciative of the role of beauty and symmetry and cognizant of the needs of society. The process of conceiving a device, analyzing it, predicting its performance, making it, testing its performance and feeding the acquired insight back into the beginning of the process also yields its own rewards. Each step requires design, informs design and drives design, while the results of testing provide the hard shot of reality that turns the wheel of design through yet another cycle.

The design options available for micromirrors are strongly coupled to the fabrication technology in which they are made. This is unavoidable. It has been the case that the reflective surface of electrothermally actuated micromirrors were formed in the same plane as the actuator [17] - [30], producing a trade-off between optical scan range θ_m and fill factor FF . The SOI-CMOS-MEMS fabrication technology described in Chapter 3 decouples θ_m and FF , enabling the optimization of both within the constraints of the mirror pitch Ω_m .

In this chapter, the relationship between geometric parameters and operational parameters are developed for 1-D and 3-D micromirrors that use folded electrothermal (FET) actuators. The objective is to clarify the interplay between the physical principles of operation, the fabrication technology and the design options. The issues of thermal isolation and speed and power scaling are discussed. The lim-

itations on device performance arising from the CMOS foundry technology are explained with reference to the physics describing the electrothermal actuation method. Following some preliminary definitions and statements of conventions, the principles of electrothermal actuation are explained and the practical issues of implementing an electrothermal actuator are presented. Electrothermally actuated micromirror topologies are listed and the design and geometric implications of each topology are discussed in.

2.1 SOI-CMOS-MEMS Mirror Design Parameters

The design of a device is defined through the parts and materials it is made of, the spatial and functional relationship between the parts and the geometric and material parameters of the parts. This section presents these for the micromirror devices analyzed in this chapter.

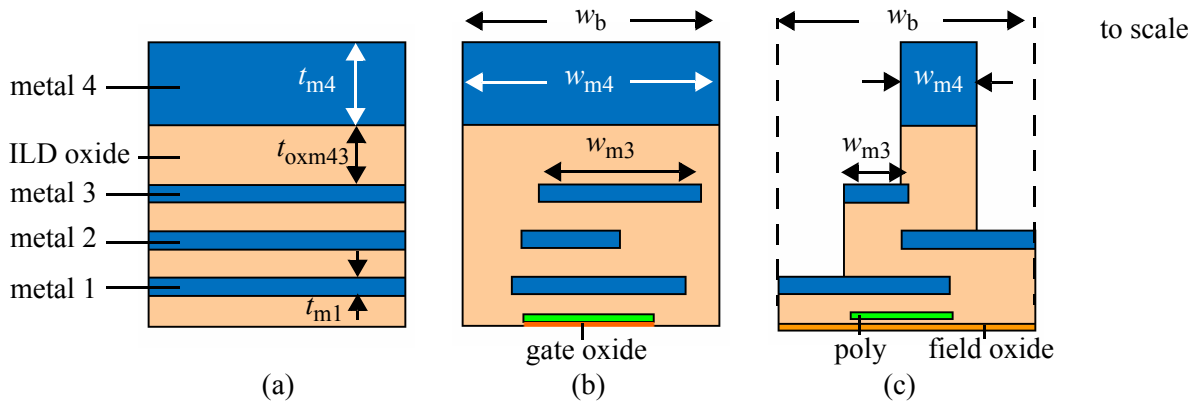
2.1.1 CMOS-MEMS Beam Types

The JAZZ 0.35 μm technology provides four metal interconnect layers and a conductive poly layer. A beam can be formed over active area, or “active” (i.e. gate oxide under poly) or on field oxide, or “field”. General CMOS-MEMS beam types are shown in Figure 2.1. CMOS-MEMS beams are typically analyzed for spring constant, effective mass and their contribution to the damping experienced by the device they are a part of. For the purpose of this dissertation, two broad classes of cross-sectional beam geometry are defined: 1. simple, as shown schematically in Figure 2.1 (a) and 2. complex, as shown schematically in Figure 2.1 (b) and Figure 2.1 (c). Mechanical behavior of a beam whose length l_b is much greater than its width w_b is largely independent of the beam type. The thermal behavior of a complex beam, on the other hand, can only be approximated by a simple beam in very restricted cases, so it is necessary to distinguish between the two types.

CMOS-MEMS beams with simple geometry consist of a fixed combination of metal layers in which all the metal layers have the same width equal to the beam width (i.e. $w_{\text{mx}} = w_b$, where

$x = 1, 2, 3, 4$ and/or p) and the overall cross-section is approximately rectangular. An additional complication is that each metal layer is actually a sandwich of refractory metals and aluminum; the implications of this are explained in Chapter 5 and Chapter 6. Between the metal layers there is interlayer dielectric (ILD), which is typically a form of silicon oxide. However, if beams whose composition and dimensions vary along their length can be decomposed into sections of uniform width and composition they can be analyzed independently as beams of simple geometry using energy methods and Euler-Bernoulli beam theory with appropriate boundary conditions [44] or through nodal simulation [45].

FIGURE 2.1 General MEMS beams geometry. (a) Simple. (b) Complex rectangular. (c) Complex non-rectangular. Note that in most CMOS processes gate oxide is only present under poly in the active area.

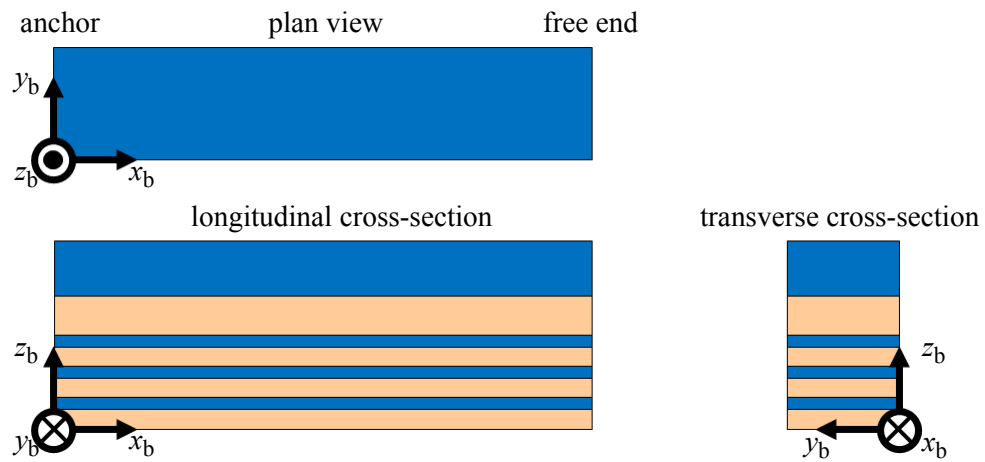


Complex beams, in contrast, are comprised of metal layers of unequal width (i.e. $w_{mx} \neq w_{my} \neq w_b$ where $x, y = 1, 2, 3, 4$ and/or p , but $x \neq y$) and may have non-rectangular cross-sections as shown schematically in Figure 2.1 (c). Complex beams are analyzed using composite beam theory [46] in which the location of a neutral bending axis is identified and the effective stiffness is calculated by summing the stiffness contribution of each homogeneous member with respect to the neutral axis [47]. The contribution of each member is dependent on its relative position in the beam. The resulting spring constant can be applied in a nodal simulation as though the beam had a simple geometry [48]. Composite beam theory, as applied to the thermomechanical behavior of complex CMOS-MEMS beams, is treated in greater detail in Section 2.2. The bending moments generated when the temperature is changed are a function of the members' geometry, their positions and their material properties. In this work, beams of both simple and complex geometry are considered.

2.1.2 CMOS-MEMS Beam Reference Directions

The equations reported in this chapter are given with respect to a reference direction shown in Figure 2.2. The mathematical expressions given in this chapter are derived with respect to this beam orientation. The convention is that the origin of the reference frame is at the anchor of the beam in the bottom right corner. The coordinates (x_b, y_b, z_b) are with respect to the beam origin.

FIGURE 2.2 Coordinate reference directions for MEMS beams and the mathematical expressions describing their behavior under electrothermal actuation. Directions exhibited using a m4321a beam. The beam origin is defined at the anchor, at the bottom right corner of the beam.



2.1.3 CMOS-MEMS Beam Descriptor

To describe the beams concisely a coded notation is adopted. A beam is referred to by the conductive layers it is comprised of and whether it is on active or field. For example, in Figure 2.1 (a) only the four metal layers are present and the beam is over active; this is a m4321a beam. This is subtly different, but equivalent to the binary code applied by Jing [45] and does not require the user to remember layer positions in the code or layer order. The beam in Figure 2.1 (b) has the same composition except that it includes poly; it is a m4321pa beam. Finally, the beam in Figure 2.1 (c) contains all conductive layers and it is formed on field; it is an m4321pf beam. The reader should note that the amount of oxide between the poly layer and the Si is less in a beam on active than it is in a beam on field and is also true for the amount of oxide between m1 and Si.

Information about whether the beam has a simple geometry or a complex geometry requires additional information about the widths of each of the metal layers and their offsets from a reference edge of the beam. This is explained further when composite beam theory is treated in detail in Section 2.2.2. While it is uncommon to use complex, non-rectangular beams in CMOS-MEMS structures there are some notable examples [49][50] that highlight the need for a more rigorous definition and treatment of beam configuration.

2.1.4 SOI-CMOS-MEMS Micromirror Topologies

SOI-CMOS-MEMS allows the realization of the device structures shown in Figure 2.3 for 1-D and 3-D micromirrors, respectively. 1-D mirrors rotate about a single axis, while 3-D rotate about two orthogonal axes and translate in the z -direction. The common features of the designs are a CMOS-MEMS folded electrothermal (FET) actuator and an SOI mirror bonded together through an SOI post and a CMOS-MEMS pedestal [51], a thermal ground and mechanical anchor and the struts that connect the elements together. The electrothermal actuator is comprised of a number of m1a or m1f beams and a discrete high resistance poly resistor as a heater, or m1pf beams in which a low resistance poly film embedded along the length of the beams serves as a distributed heater. In the case of m1pf actuator beams, a subset of the beams in the actuator are m1f beams reserved as electrical feedthroughs. In Figure 2.3, discrete resistors are shown in the actuators.

The 1-D and 3-D topologies differ only in the number, organization and placement of the design elements. The 1-D FET actuators come in several topological varieties that are explored in Section 2.5. The structural design parameters are listed with their definitions in Table 2.1. Figure 2.4 illustrates the relevant dimensions of the SOI and CMOS-MEMS elements of the micromirror. The fixed parameters, i.e. those that are defined by the foundry process or the post-CMOS process are given in Table 2.2.

TABLE 2.1 SOI-CMOS-MEMS micromirror structural design parameters. A device critical subset identified by * is shown in Figure 2.4.

Parameter	Symbol
array pitch*	Ω
mirror length*	l_m
mirror Si thickness	$t_{m,Si}$
mirror Al thickness	$t_{m,Al}$
SOI buried oxide (BOX) thickness	t_{BOX}
post width*	w_p
post thickness*	t_p
pedestal width*	w_{ped}
pedestal length	l_{ped}
gap between pedestal and anchor*	g_{ped}
Si thickness under pedestal*	$t_{ped,Si}$
anchor width*	w_{anc}
width of thermal isolation unit	w_{iso}
length of thermal isolation unit	l_{iso}
number of thermal isolation units in parallel	$N_{p,v}$
number of thermal isolation units in series	$N_{s,v}$
strut width*	w_s
strut length	l_s
gap between strut and anchor*	g_s
strut extender length	l_e
actuator beam width*	w_b
actuator beam length*	l_b
number of actuator beams in parallel*	$N_{p,b}$
gap between adjacent actuator beams*	g_b
actuator length	l_a
heater width*	w_h
heater length	l_h
heater poly width*	w_p
heater poly enclosure	e_p
fractional heater position	λ

Parameter	Symbol
Si undercut of CMOS-MEMS structure*	u
via enclosure	e_v
metal overlap by upper metal (x,y = 1, 2, 3)	o_{mxy}

TABLE 2.2 *SOI-CMOS-MEMS fixed micromirror structural design parameters. Beam thicknesses are constrained by the thicknesses of the layers from which they are made.*

Parameter	Symbol
metal x layer thickness	t_{mx}
oxide ILD thickness between metal y and metal x	t_{oxmyx}
minimum mirror gap	$g_{m,min}$
pedestal thickness	t_{ped}
minimum gap between pedestal and anchor	$g_{ped,min}$
minimum anchor width	$w_{anc,min}$
strut thickness	t_s
minimum gap between strut and anchor	$g_{s,min}$
minimum actuator beam thickness	$w_{b,min}$
actuator beam thickness	t_b
minimum gap between adjacent actuators	$g_{a,min}$
heater thickness	t_h
minimum poly enclosure by upper metal layers	$e_{p,min}$
minimum via enclosure by upper metal layers	$e_{v,min}$
minimum m1 width	$w_{m1,min}$
minimum m1 spacing	$g_{m1,min}$
minimum poly width	$w_{p,min}$

FIGURE 2.3 Conceptual plan-view and cross-sectional schematics of SOI-CMOS-MEMS electrothermally actuated (a) 1-D and (b) 3-D micromirrors for arrayed devices. images not to scale

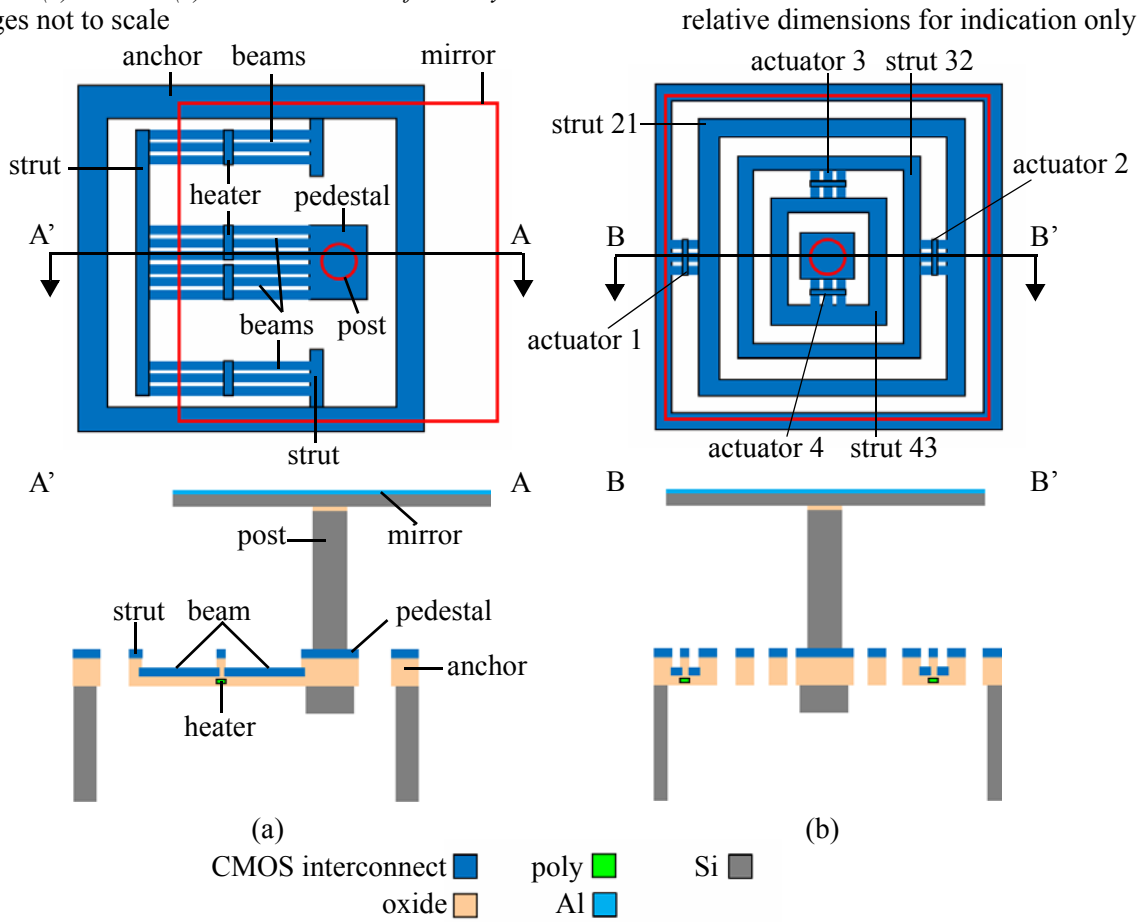
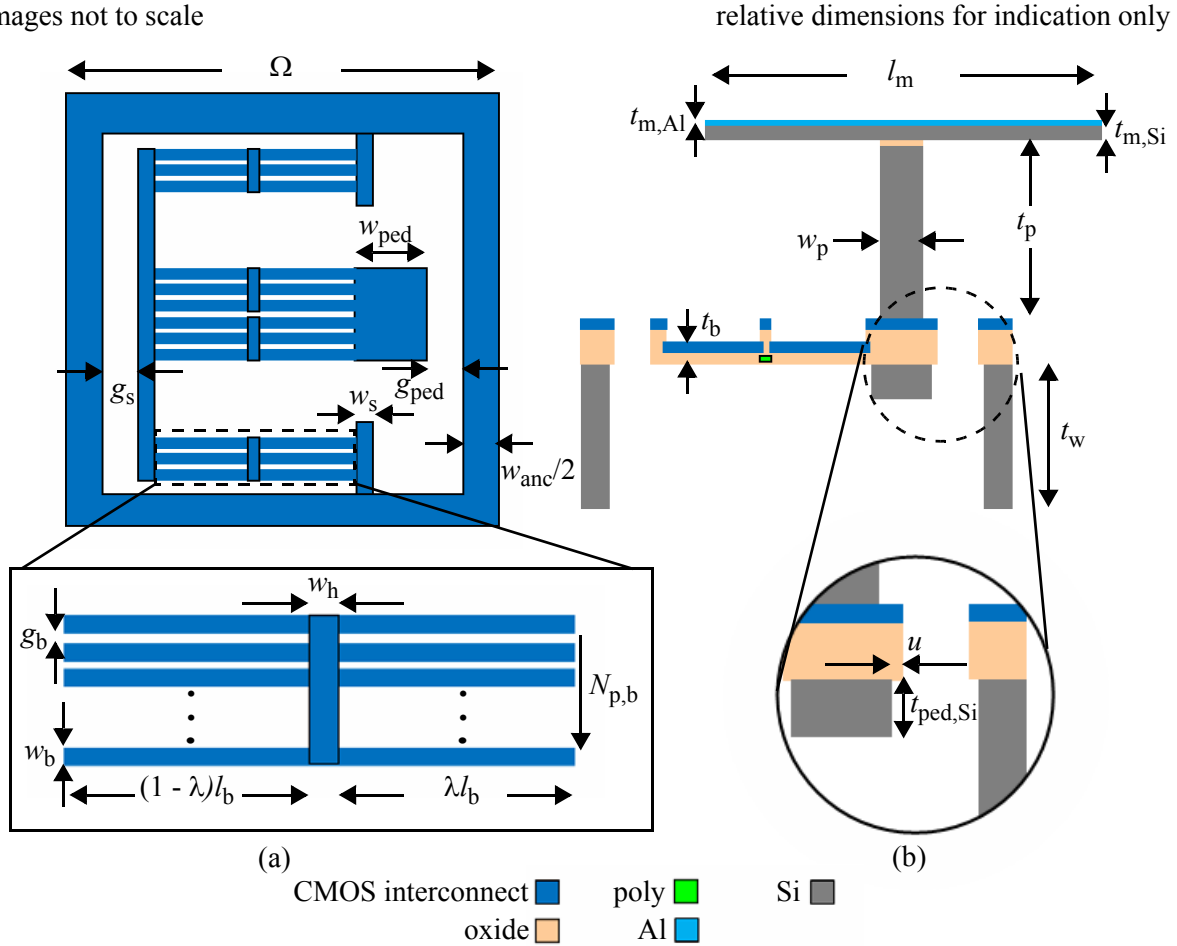


FIGURE 2.4 Design dimensions illustrated using (a) a CMOS-MEMS plan-view schematic and blow-up view of an actuator and (c) a cross-sectional view of the SOI mirror and post and a blow-up of the pedestal.

images not to scale



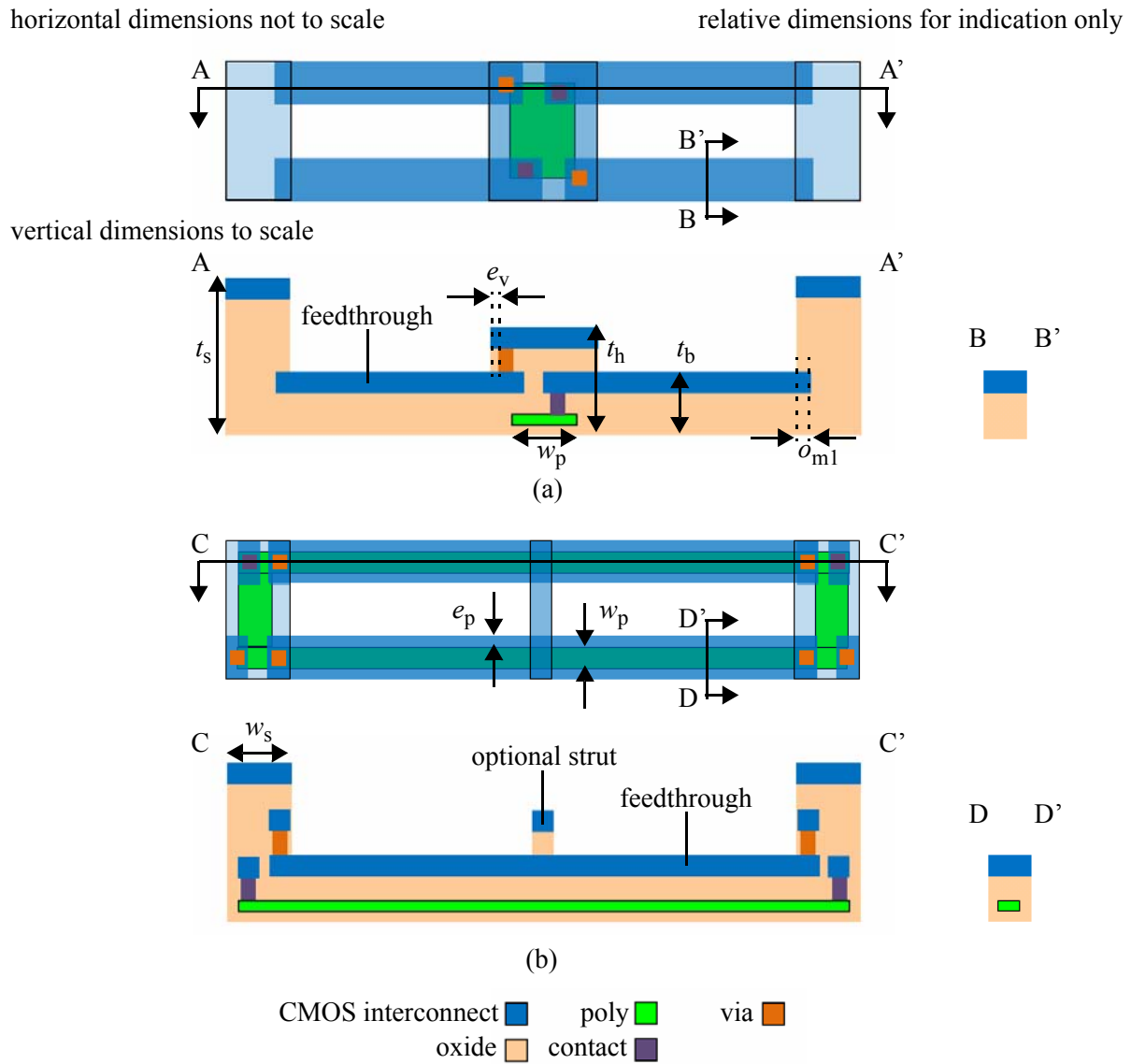
2.1.5 Actuator and Heater Types

Joule heating in discrete poly resistors or in low-resistance poly films embedded along the length of the beams in an actuator provides the electrical energy dissipation into the thermal domain that increases the beam temperature. In Figure 2.5, the two heater types are shown in plan view and cross-sectional schematic. The interconnect configuration for external connectivity is not shown.

For mirrors with large Ω that use discrete resistor heating, the values of parameters such as the heater width, w_h , poly enclosure, e_p , and via enclosure, e_v , do not significantly impact the design. However, it is shown in Section 2.4.3 that a trade-off occurs in actuator angular thermal sensitivity (i.e. the angular displacement per degree change in temperature [30]) as Ω_m decreases and the proportion

of the beam length taken up by the heater width increases. A point is reached when the intrinsically higher sensitivity of the m1a and m1f beams is outweighed by the less sensitive m1pf beam which does not give up valuable length to the essential m2 cover of the poly resistor. Furthermore, the heater type constrains the strut width w_s as Ω decreases because it must accommodate contacts and vias that have a minimum enclosure requirement for reasons that are explained in Chapter 5.

FIGURE 2.5 Electrothermal actuator plan-view and cross-sectional schematics for (a) discrete poly-Si resistors and (b) poly-Si film embedded along the length of the beam.



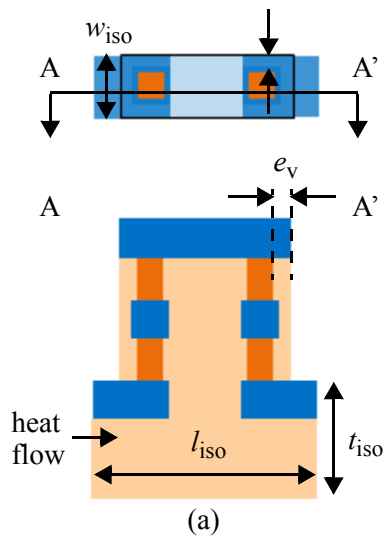
2.1.6 Thermal Isolation Design

The final component of the design is the thermal isolation. It is shown in Section 2.3 that the thermal isolation design is critical to the performance of the devices because the mirror scan angle in each direction depends on the difference in the average temperature of the actuators. When one actuator is heated by either a discrete resistor, or embedded poly film, a temperature field is developed. The actuator should be designed such that the maximum temperature in the field occurs somewhere in the powered actuator. The thermal isolation serves to create large temperature gradients between the powered and unpowered actuators, the pedestal and the anchor. The larger the gradients between the heated actuator and the elements it is connected to, the more efficient the device. However, the trade-off is that more thermal isolation, characterized by a lumped thermal resistance $R_{th,iso} = l_{iso}/\kappa_{eff,iso}w_{iso}t_{iso}$, increases the thermal time constant and reduces the speed of the device.

FIGURE 2.6 Plan-view and cross-sectional schematics for (a) via thermal isolation unit for low electrical resistance but “high” thermal resistance and (b) strut thermal isolation for high mechanical stiffness and high thermal resistance.

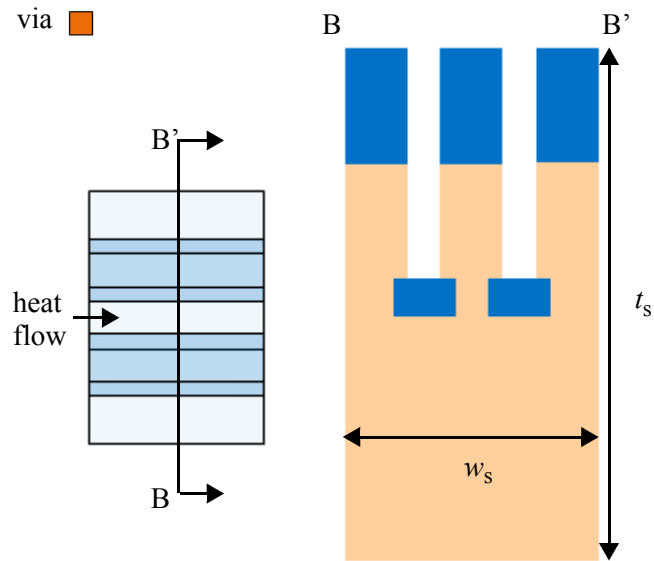
vertical dimensions to scale

CMOS interconnect ■ oxide ■ via ■



(a)

horizontal dimensions not to scale



(b)

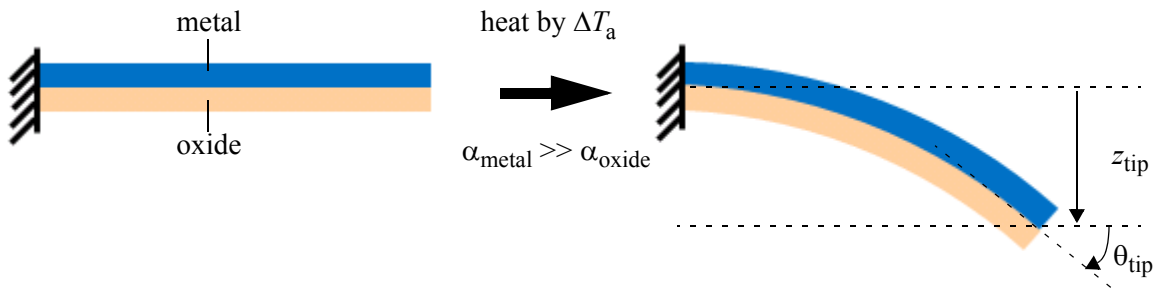
To achieve high thermal isolation the length of the isolation l_{iso} can be increased, the width w_{iso} and thickness t_{iso} can be decreased and/or materials can be chosen with lower thermal conductance κ . The downside to the geometric approach to improving thermal isolation is that the mechanical strength

decreases and the device becomes subject to breakage, or it can bend under the action of residual and thermal stresses, which introduces non-linearities [43]. The thermal isolation solutions used in this work are shown in Figure 2.6. They represent a compromise between thermal resistance and electrical resistance in the via thermal isolation case and thermal resistance and mechanical strength in the isolation strut case. The finite element analysis (FEA) of these structures is presented in Section 2.3.

2.2 Principles of Electrothermal Actuation

Beams made of materials with dissimilar coefficients of thermal expansion (CTE) bend when they are heated due to the thermally generated moments arising from stresses whose lines of action are a finite distance from the neutral bending axis of the beam. The bending leads to changes in the angle and displacement of the free end of the beam as shown in Figure 2.7. This is the fundamental principle of electrothermal actuation. The magnitude of the bending and the temperature changes that cause it are examined in this section.

FIGURE 2.7 Longitudinal beam cross-sections showing the principle of electrothermal actuation. A beam of two, or more materials of dissimilar coefficients of thermal expansion α bends when heated and the tip moves through a distance z_{tip} and an angle θ_{tip} .



The actuator beam is broken into discrete elements of rectangular cross-section that are henceforth called beam "members". For the purpose of analysis and simulation, beam members are assumed to be linearly elastic, homogeneous and to have isotropic properties. The thermal sensitivity of the actuators is described using Euler-Bernoulli beam theory, subject to the principle of superposition and the assumption of temperature uniformity across the width and thickness of the beam. For the first part of

the analysis, the beam temperature change ΔT_a is assumed constant, but this is relaxed in Section 2.2.3 to analyze the displacement behavior for expected temperature distributions. Although, for micromirror applications, rotational displacement and not translational displacement, is of primary concern, translation of the mirror has implications for optical signal processing due to its impact on phase, and so, translational displacement is also covered.

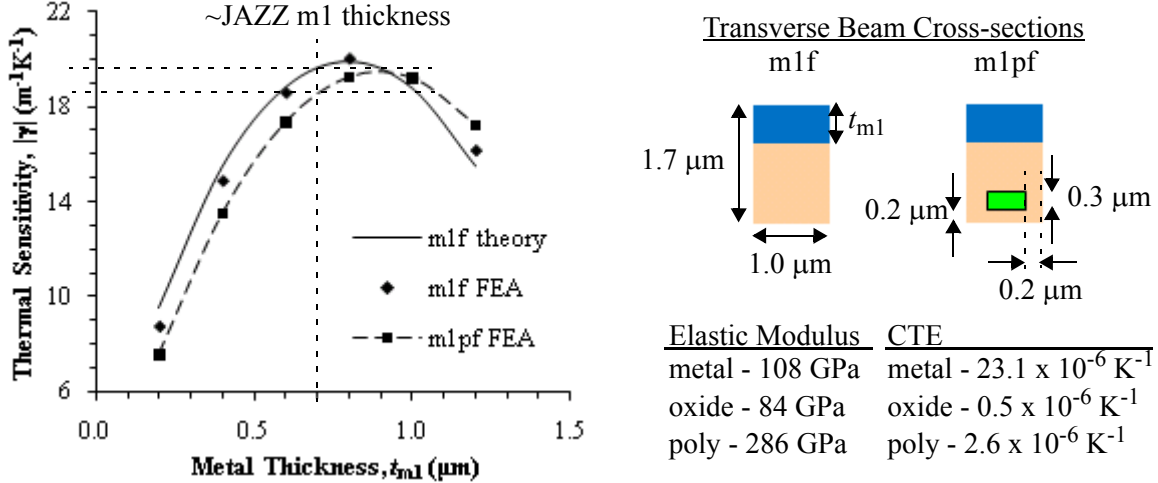
2.2.1 Bimorph Thermomechanical Response

Timoshenko's theory of the bimetal thermostat [39] is used extensively to describe the thermomechanical behavior of composite MEMS beams made of two materials [30][40] like those of the cross-section in Figure 2.5 (a), but has also been applied in the analysis of beams made with three materials [53] like those of the cross-section in Figure 2.5 (b). Timoshenko showed that the radius of curvature $\rho_{c,th}$ of a bimorph subject to a thermally induced stress difference between the two materials is

$$\frac{1}{\rho_{c,th}} = -\frac{M_{y,th}}{(EI)_{eff,y}} = -\frac{6t_b(\alpha_{m1} - \alpha_{ox})\Delta T_a}{4t_{m1}^2 + 4t_{oxm1Si}^2 + 6t_{m1}t_{oxm1Si} + \frac{t_{m1}^3 E'_{m1}}{t_{oxm1Si} E'_{ox}} + \frac{t_{oxm1Si}^3 E'_{ox}}{t_{m1} E'_{m1}}} = \gamma \Delta T_a, \quad (2.1)$$

where $M_{y,th}$ is the thermally generated internal moment about the y -axis, $(EI)_{eff,y}$ is the effective flexural rigidity for bending about the y -axis, α_{m1} and α_{ox} are the CTEs of the m1 layer and the oxide, respectively, and E'_{m1} and E'_{ox} are the biaxial moduli of the m1 layer and the oxide, respectively. The parameter γ is the thermal sensitivity, or curvature per unit change in temperature, and is used to simplify (2.1) and provide the means by which the response of different types of beams can be compared. Positive values of γ indicate the beam bends such that the center of curvature moves in the positive z -direction when heated, while negative values of γ indicate the beam bends such that the center of curvature moves in the negative z -direction when heated. For graphical purposes, only the magnitude of γ is plotted in the following graphs.

FIGURE 2.8 Comparison of γ from Timoshenko's theory of the bimorph and γ determined from FEA for m1f and m1pf beams of fixed total thickness t_b and varying t_{m1} . The elastic moduli and CTEs for the FEA come from Comsol Multiphysics Material Library [52]. The biaxial modulus is used for metal and oxide, while the triaxial modulus is used for poly.



A comparison of γ from theory and FEA for an actuator of fixed thickness t_b and varying metal thickness t_{m1} is shown in Figure 2.8. For a simple beam made of two homogeneous materials, like the actuators with discrete resistors of Figure 2.5 (a) (ex. a m1f beam), the theory provides excellent agreement to FEA. However, as the beam becomes complex, like the m1pf beam in Figure 2.5 (b), Figure 2.8 shows the predictive power of the bimetal theory diminishes (max. error of 26% over the range of metal thicknesses, which increases as w_p increases relative to w_b). An analytic model is needed that can better approximate the behavior of complex multimorph structures.

The angle at a position x along the length of a bimorph when it is uniformly heated through a temperature ΔT_a is

$$\theta(x) = \int \frac{M_{y,th}}{(EI)_{eff,y}} dx = \gamma x \Delta T_a + \theta_0, \quad (2.2)$$

where θ_0 is the angle at the origin of the bimorph. With the small angle approximation that the incremental distance along the beam equals the incremental distance from the anchor, the z -displacement of the bimorph is

$$z(x) = \int \theta(x) dx = \gamma \frac{x^2}{2} \Delta T_a + \theta_0 x + z_0 \quad (2.3)$$

where z_0 is the z -displacement at the origin of the bimorph. For the case of a cantilevered bimorph anchored at its origin, $\theta_0 = 0$ and $z_0 = 0$ and the angle and the z -displacement at the free end are

$$\theta_{\text{tip}} = \gamma l_b \Delta T_a. \quad (2.4)$$

and

$$z_{\text{tip}} = \gamma \frac{l_b^2}{2} \Delta T_a, \quad (2.5)$$

respectively.

For beams long enough to invalidate the small-angle approximation, the z -displacement of the beam at a distance x from the anchor is the solution of

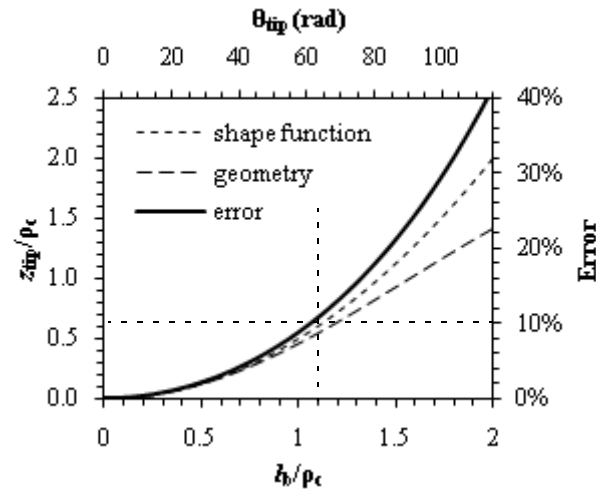
$$\frac{d^2 z}{dx^2} - \gamma \Delta T_a \left[1 + \left(\frac{dz}{dx} \right)^2 \right]^{1.5} = 0 \quad [57]. \quad (2.6)$$

Equation (2.6) has no simple solution, but for beams with a constant radius of curvature ρ_c the tip z -displacement is

$$z_{\text{tip}} = \rho_c \left(1 - \cos \frac{l_b}{\rho_c} \right). \quad (2.7)$$

Comparing z_{tip} from (2.5) and (2.7) normalized to ρ_c in Figure 2.9 demonstrates an error that exceeds 10% when $l_b > 1.1\rho_c$, which corresponds to a tip angle $\theta_{\text{tip}} \sim 60^\circ$. The application of (2.3) results in an error that is reasonable given the benefit in analytic tractability it provides. In the following analyses, the error doesn't effect the relative differences between m1a- and m1pf-based actuators, but should an exact value of z_{tip} be needed, (2.6) can be solved numerically.

FIGURE 2.9 Comparison of the normalized beam tip z -displacement z_{tip}/ρ_c as a function of the beam length normalized to ρ_c and as a function of the tip angle θ_{tip} from shape function and geometry. The error in the shape function is shown on the secondary y -axis.



2.2.2 Multimorph Thermomechanical Response

The thermomechanical response of a multimorph depends on the thickness, width, position and material properties of each beam member. This makes the analytic formulation more involved, but a systematic approach makes it tractable for beams of many members. The theory is equivalent to Timoshenko's for a bimorph but has a different flow of analysis. In contrast to Timoshenko's bimorph theory, the multimorph theory [46][47] requires the determination of the position ($y_{\text{na}}, z_{\text{na}}$) of a neutral bending axis with respect to the beam origin (y_b, z_b) = (0,0). Although other authors, such as Todd et al. [54] assumed that bimorph theory provides a sufficient approximation to the angular and tip displacements of multimorph beams, particularly metal-oxide beams with poly layers embedded in the beam, it is shown in this sub-section that the error due to this assumption can be significant. The extension of Timoshenko's approach to trimorph beams, derived by Lammell et al [30], is an improvement, but their derivation is not easily extended to beams for which one member does not span the entire width of the beam and the error can be significant.

The neutral axis is the modulus weighted centroid of the beam. Its position is important to the behavior of the beam as it defines the position from which the beam's radius of curvature is taken and

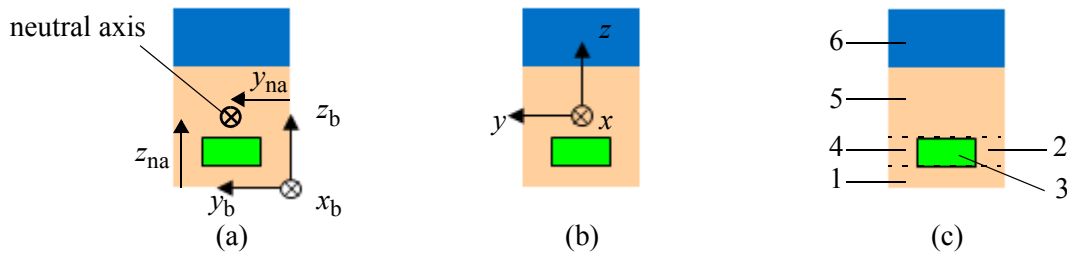
it locates the longitudinal fiber for which the strain under bending is zero. The total strain in the heated electrothermal actuator is the sum of the thermal strain, the strain due to bending and flexural rigidity, and the axial deformation. When the moments due to these strains are calculated about the neutral axis, there is no net contribution from the axial deformation, which simplifies the equation of moment equilibrium. This is the point of departure from Timoshenko's theory and must be noted because it leads to a change in the familiar form of the expression for curvature, while retaining mathematical equivalence. The different approach is taken to simplify the multimorph analytic expressions and to aid intuitive understanding of the optimization of the actuator.

The neutral axis is defined by the intersection of the neutral surfaces for bending about the y and z axes. Its placement in z , z_{na} , is shown schematically for a mlpf beam in Figure 2.10 and is calculated through the condition

$$\int_{-y_{na}}^{y_b - y_{na}} \int_{-z_{na}}^{z_b - z_{na}} E^* z dz dy = 0, \quad (2.8)$$

where y and z are coordinates with respect to the neutral axis and E^* is an elastic modulus whose exact definition depends on the type of stress being considered. The assumption of homogeneity allows that the elastic modulus be treated as constant within a member.

FIGURE 2.10 Transverse beam cross-sections showing (a) the neutral axis location in a mlpf beam, (b) the coordinate axis for moment and flexural rigidity calculations defined on the neutral axis and (c) the decomposition of a mlpf beam into a set of members.



By performing a coordinate transformation, $y = y_b - y_{na}$, the distance of the neutral axis from the beam origin can be found in terms of the material properties and beam geometry using

$$z_{na} = \frac{\sum_{\text{members}} \int_{y_{b,i}}^{y_{b,i} + \Delta y_i} \int_{z_{b,i}}^{z_{b,i} + \Delta z_i} E_i^* z_b dz_b dy_b}{\sum_{\text{members}} \int_{y_{b,i}}^{y_{b,i} + \Delta y_i} \int_{z_{b,i}}^{z_{b,i} + \Delta z_i} E_i^* dz_b dy_b} \quad (2.9)$$

where $(y_{b,i}, z_{b,i})$ are the coordinates of the i^{th} member with respect to the beam origin, and $\Delta y_{b,i}$ and $\Delta z_{b,i}$ are the member width and thickness, respectively. Equation (2.9) evaluates to

$$z_{na} = \frac{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left(z_{b,i} + \frac{\Delta z_i}{2} \right)}{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i} \quad (2.10)$$

where the various values of the elements of the summation for the decomposed m1pf beam in Figure 2.10 (b) are given in Table 2.3.

TABLE 2.3 Dimensions of the elements of the summation in (2.10) for the m1pf beam in Figure 2.10 (b).

Member #	$z_{b,i}$	Δz_i	Δy_i
1	0	t_{oxpSi}	w_b
2	t_{oxpSi}	t_p	e_p
3	t_{oxpSi}	t_p	$w_b - 2e_p$
4	t_{oxpSi}	t_p	e_p
5	$t_{\text{oxpSi}} + t_p$	t_{oxm1p}	w_b
6	$t_b - t_{m1}$	t_{m1}	w_b

An analogous equation exists for the distance of the neutral axis from the beam origin in the y -direction but because of the beam symmetry about the z -axis, the neutral axis is located at $w_b/2$. The deformation due to thermal expansion occurs in all directions and the actuator structure constrains this expansion in two dimensions, so the stress in each member is not uniaxial. To account for this, the biaxial modulus of the i^{th} member, $E'_i = E_i / (1 - \nu_i)$, is used in (2.9). However, the poly member is constrained in 3-D due to the surrounding material, so the triaxial modulus $E''_i = E_i / (1 - 2\nu_i)$ is

used, which is generalized for all such fully encapsulated members. For partially encapsulated members, the biaxial modulus is a practical compromise.

With the position of the neutral axis identified, the bending moment about the y -axis, M_y , due to an in-plane stress distribution $\sigma_i(z)$ in the i^{th} member is determined using

$$M_y = \sum_{\text{members}} \int_{y_i}^{y_i + \Delta y_i} \int_{z_i}^{z_i + \Delta z_i} \sigma_i(z) z dz dy, \quad (2.11)$$

which, if $\sigma_i(z)$ is constant throughout the member, evaluates to

$$M_y = \sum_{\text{members}} \sigma_i \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right). \quad (2.12)$$

The effective flexural rigidity about the y -axis is

$$(EI)_{\text{eff},y} = \sum_{\text{members}} \int_{y_i}^{y_i + \Delta y_i} \int_{z_i}^{z_i + \Delta z_i} E_i^* z^2 dz dy \quad (2.13)$$

which, if $E_i^*(z)$ is constant throughout the member, evaluates to

$$(EI)_{\text{eff},y} = \sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left[\Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{3} \right) + (z_{b,i} - z_{na})^2 \right]. \quad (2.14)$$

The radius of curvature of the multimorph due to the in-plane stresses is

$$\frac{1}{\rho_c} = -\frac{M_y}{(EI)_{\text{eff},y}} = -\frac{\sum_{\text{members}} \sigma_i \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right)}{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left[\Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{3} \right) + (z_{b,i} - z_{na})^2 \right]}. \quad (2.15)$$

In the case of stresses due to thermal expansion

$$\sigma_{\text{th}} = \alpha E^* \Delta T, \quad (2.16)$$

which, when substituted into (2.15), with the assumption of equal temperature change ΔT_a for all members, gives

$$\frac{1}{\rho_{c,\text{th}}} = -\frac{M_{y,\text{th}}}{(EI)_{\text{eff},y}} = -\frac{\sum_{\text{members}} \alpha_i E_i^* \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right)}{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left[\Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{3} \right) + (z_{b,i} - z_{na})^2 \right]} \Delta T_a = \gamma \Delta T_a. \quad (2.17)$$

Equation (2.17) allows γ to be calculated analytically for a CMOS-MEMS beam of any level of complexity and with γ in hand, (2.2) and (2.3) are used to calculate θ_{tip} and z_{tip} , respectively. As a comparison with the use of the bimorph theory to describe an actuator with an embedded poly layer (see Figure 2.8), the multimorph theory agrees with FEA to better than 4% across the range of metal thicknesses shown in Figure 2.11 (a). The variation in γ with t_{m1} for m1pf beams of varying width is presented in Figure 2.11 (b). While narrower beams have greater sensitivity, the difference is less than 4%. The multimorph theory has been shown to match experiment for beams more complex than m1pf [55] and can be used to design new actuator types like the one shown in Figure 2.12 in which the heater is a stiff, resistive metal such as nichrome. The theory also highlights the advantage of scaling down thickness as shown in Figure 2.13 to offset some of the negative scaling of θ_{tip} with l_b . The difference in thermal sensitivity between an m1f and an m1a beam is $\sim 8\%$ as its magnitude increases from $19.5 \text{ m}^{-1}\text{K}^{-1}$ to $21 \text{ m}^{-1}\text{K}^{-1}$, respectively. Such a change is not possible for the m1pf beam as the thicker field oxide is needed to protect the poly from the etchant during release etch.

The final insight for actuator design provided by the multimorph theory is relevant for custom fabrication technologies for which the metal:oxide ratio can be defined by the user. In each of the graphs from Figure 2.8 to Figure 2.12, a maximum is observed in the magnitude of the sensitivity. This condition occurs when stiff, high CTE materials are confined to one side of the neutral axis and the rela-

tively pliable, low CTE materials are confined to the other side of the neutral axis. For a JAZZ m1f beam only an additional 2% sensitivity would be gained from optimizing layer thicknesses, but for an m1pf beam the gain would be 6%.

FIGURE 2.11 (a) Comparison of the multimorph theory prediction of γ for a m1pf beam and the value extracted from FEA over a range of t_{m1} for a fixed t_b . The prediction using Timoshenko's bimorph theory is shown for contrast. The geometry and material parameters of the beam are the same as used for the graph in Figure 2.8. (b) Thermal sensitivity variation of a m1pf beam for a range of w_b but fixed $e_p = 0.2 \mu\text{m}$.

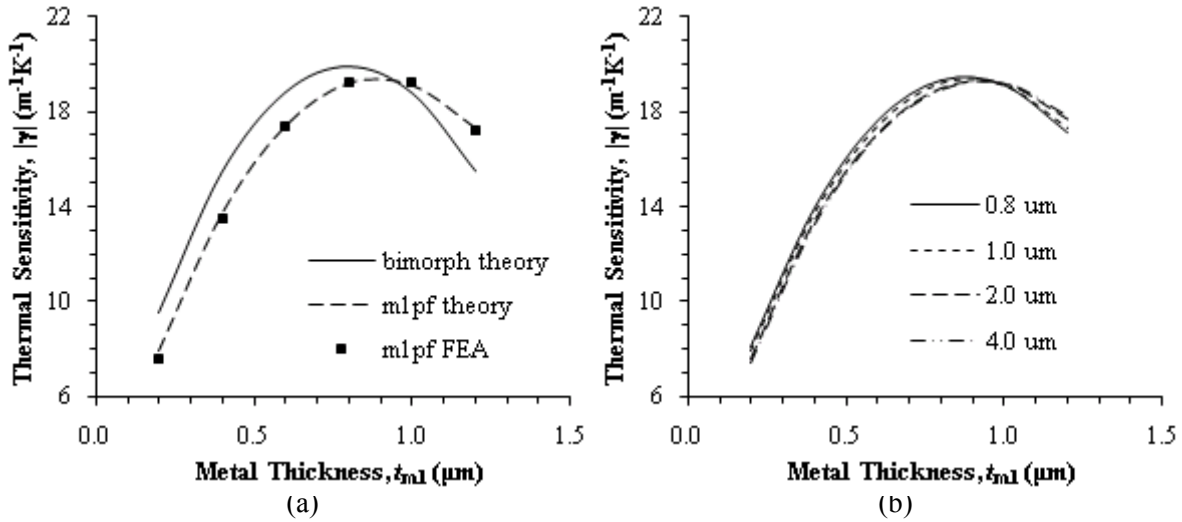


FIGURE 2.12 Comparison of m1pf beam sensitivity over a range of t_{m1} with the sensitivity of electrothermal actuators of various thickness t_b with a nichrome heater above the metal layer.

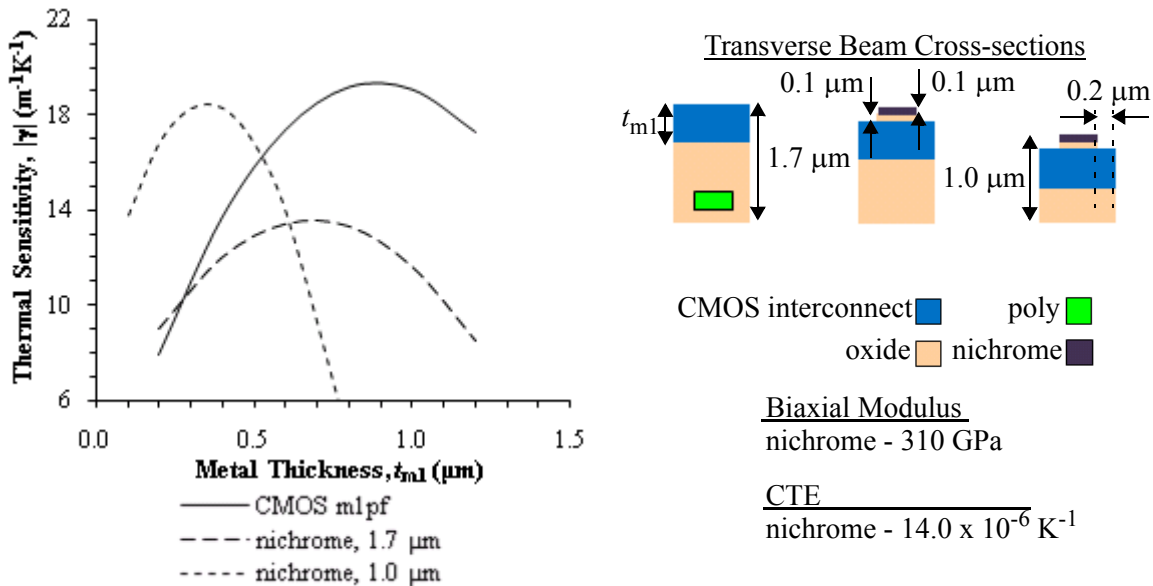
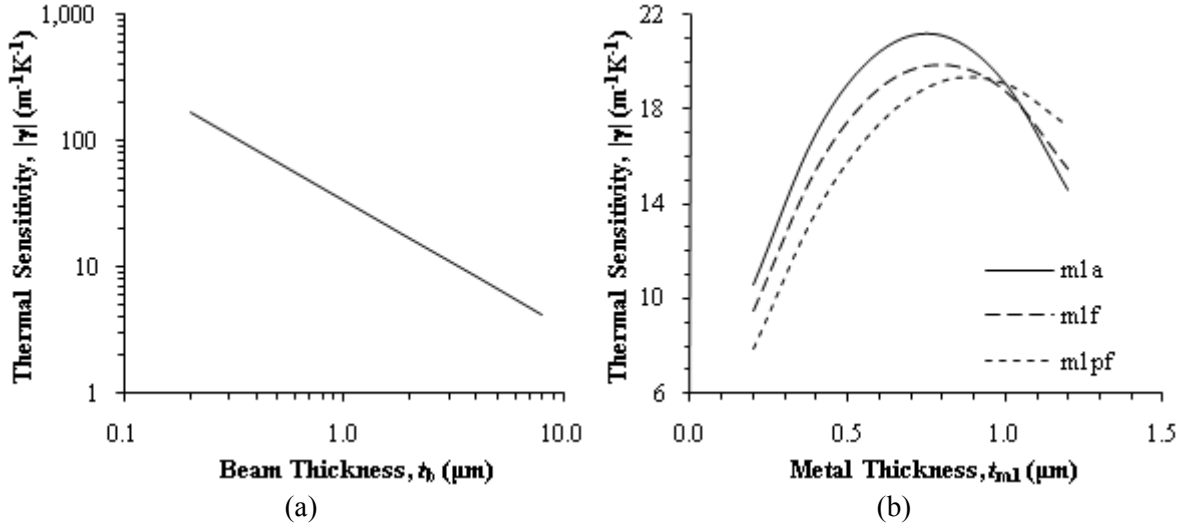


FIGURE 2.13 (a) Variation in γ as t_b is reduced showing the advantage of scaling thickness. (b) The sensitivity gain in changing from a 1 μm wide, 1.7 μm thick mlf beam to a mla beam is a result of a 0.1 μm reduction in t_b . The thermal sensitivity variation of an mlpf beam of equivalent dimensions is shown for comparison.



2.2.3 Impact of Temperature Distributions

One of the assumptions in deriving (2.2) and (2.3) is constant beam temperature along its length but this is not practically achievable in real devices. Xie et al. [53] showed that θ_{tip} is dependent on the average temperature change $\Delta\bar{T}_a$. For single electrothermal actuators this is sufficient, however, for arrayed mirrors with folded actuators, the rotation angle and the translation of the mirror must be known to avoid collisions between adjacent array elements. Given a temperature change distribution $\Delta T_a(x)$ along the actuator length, the thermally generated moment about the y-axis is

$$M_{y,\text{th}}(x) = \sum_{\text{members}} \alpha_i E_i^* \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right) \Delta T_a(x). \quad (2.18)$$

Equation (2.18) replaces the numerator in (2.17) to give

$$\frac{1}{\rho_c} = \frac{\sum_{\text{members}} \alpha_i E_i^* \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right) \Delta T_a(x)}{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left[\Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{3} \right) + (z_{b,i} - z_{na})^2 \right]} \Delta T_a(x) = \gamma \Delta T_a(x), \quad (2.19)$$

which is integrated to obtain θ_{tip} and z_{tip} for a given temperature distribution.

In the steady-state, neglecting convection into the surrounding air and conduction to the substrate, the heat equation is solved to give temperature change distributions for m1pf beams and m1f beams.

The temperature change distribution in the m1f beam is

$$\Delta T_{\text{a,m1f}}(x) = C_{1,1,\text{m1f}}x + C_{0,1,\text{m1f}} \text{ for } x \leq \lambda l_b, \quad (2.20)$$

$$\Delta T_{\text{a,m1f}}(x) = C_{1,1,\text{m1f}}\lambda l_b + C_{0,1,\text{m1f}} \text{ for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.21)$$

and

$$\Delta T_{\text{a,m1f}}(x) = C_{1,2,\text{m1f}}(x - w_h) + C_{0,2,\text{m1f}} \text{ for } x > \lambda l_b + w_h. \quad (2.22)$$

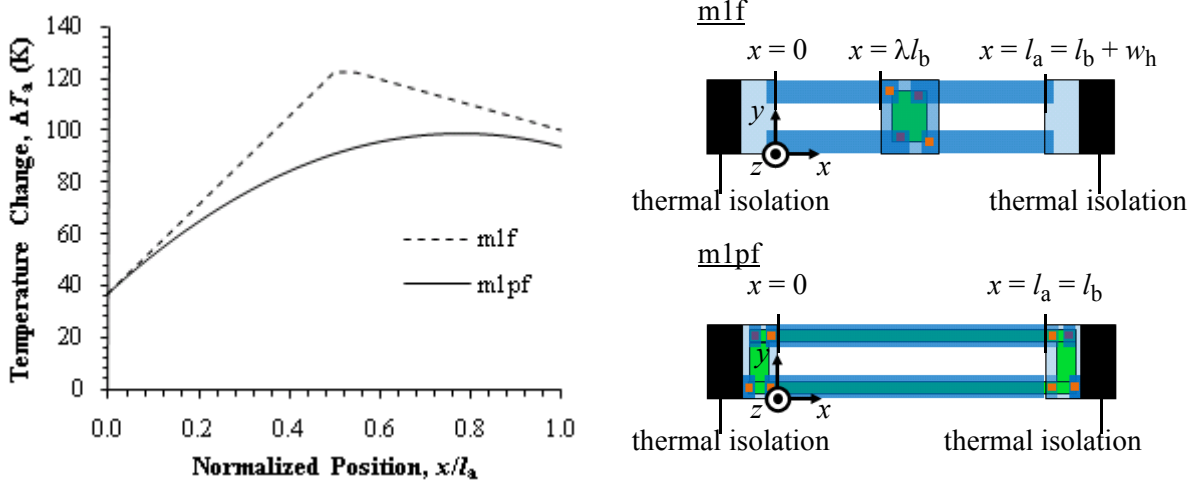
The temperature distribution in the m1pf beam is

$$\Delta T_{\text{a,m1pf}}(x) = C_{2,\text{m1pf}}x^2 + C_{1,\text{m1pf}}x + C_{0,\text{m1pf}}. \quad (2.23)$$

The coefficients C_i , derived in Section 2.3, depend on the power dissipated in the actuator, the geometry of the beam and the thermal isolation used to manage the thermal dissipation of the device.

For example, typical temperature distributions are shown in Figure 2.14 for a m1f beam with discrete resistors and a m1pf beam. The temperature distributions are generated with equivalent thermal isolation configurations, actuator geometry and power dissipations to provide a direct comparison of each beam type. For this comparison, convection and conduction to the substrate are equivalent for each beam type, so neglecting them for the sake of analytic simplicity does not affect the conclusions.

FIGURE 2.14 Typical temperature distributions for a mlf bimorph ($|\gamma| = 18.9 \text{ m}^{-1}\text{K}^{-1}$) with discrete resistors and a mlpf multimorph ($|\gamma| = 18.1 \text{ m}^{-1}\text{K}^{-1}$) with embedded poly film shown in plan view schematic. The dissipated power ($P_h = 0.5 \text{ mW}$) and beam geometry ($l_a = 100 \text{ }\mu\text{m}$, $w_b = 2 \text{ }\mu\text{m}$) are the same for each beam type and $\lambda = 0.5$ for the resistor in the mlf beam. The thermal isolation is shown as a black box because its detailed treatment is not covered until Section 2.3. The temperature is assumed constant within the heater.



For the mlf beam, the angle along the beam $\theta_a(x)$ is

$$\theta_{a,\text{mlf},1}(x) = \int \gamma_{\text{mlf}} \Delta T_{a,\text{mlf}}(x) dx = \gamma_{\text{mlf}} \left(\frac{C_{1,1,\text{mlf}}}{2} x^2 + C_{0,1,\text{mlf}} x \right) \text{ for } x \leq \lambda l_b, \quad (2.24)$$

$$\theta_{a,\text{mlf},2}(x) = \gamma_{\text{mlf}} \lambda l_b \left(\frac{C_{1,1,\text{mlf}}}{2} \lambda l_b + C_{0,1,\text{mlf}} \right) \text{ for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.25)$$

and

$$\begin{aligned} \theta_{a,\text{mlf},3}(x) = & \gamma_{\text{mlf}} \left(\frac{C_{1,2,\text{mlf}}}{2} (x - w_h)^2 + C_{0,2,\text{mlf}} (x - w_h) \right) \text{ for } x > \lambda l_b + w_h, \quad (2.26) \\ & + \frac{(C_{1,1,\text{mlf}} - C_{1,2,\text{mlf}})}{2} \lambda^2 l_b^2 + (C_{0,1,\text{mlf}} - C_{0,2,\text{mlf}}) \lambda l_b \end{aligned}$$

assuming $\theta_{a,\text{mlf},1}(0) = 0$ and a rigid heater and noting that $\theta_{a,\text{mlf},1}(\lambda l_b) = \theta_{a,\text{mlf},3}(\lambda l_b + w_h)$. Integrating $\theta_{a,\text{mlf}}(x)$ along the length of the beam yields the z -displacement

$$z_{a,\text{mlf},1}(x) = \frac{\gamma_{\text{mlf}}}{2} \left(\frac{C_{1,1,\text{mlf}}}{3} x^3 + C_{0,1,\text{mlf}} x^2 \right) \text{ for } x \leq \lambda l_b, \quad (2.27)$$

$$z_{a,m1f,2}(x) = \frac{\gamma_{m1f}}{2} \left(\frac{C_{1,1,m1f}}{3} (\lambda l_b)^3 + C_{0,1,m1f} (\lambda l_b)^2 \right) \quad \text{for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.28)$$

$$+ (x - \lambda l_b) \sin \theta_{a,m1f}(\lambda l_b)$$

and

$$z_{a,m1f,3}(x) = \gamma_{m1f} \left(\frac{C_{1,2,m1f}}{6} (x - w_h)^3 + \frac{C_{0,2,m1f}}{2} (x - w_h)^2 \right) \quad \text{for } x > \lambda l_b + w_h, \quad (2.29)$$

$$+ \left(\frac{(C_{1,1,m1f} - C_{1,2,m1f})}{2} \lambda^2 l_b^2 + (C_{0,1,m1f} - C_{0,2,m1f}) \lambda l_b \right) (x - w_h)$$

$$- \frac{(C_{1,1,m1f} - C_{1,2,m1f})}{3} \lambda^3 l_b^3 - \frac{(C_{0,1,m1f} - C_{0,2,m1f})}{2} \lambda^2 l_b^2$$

$$+ w_h \sin \theta_{a,m1f}(\lambda l_b)$$

assuming $z_{a,m1f}(0) = 0$ and noting that $z_{a,m1f,3}(\lambda l_b + w_h) = z_{a,m1f,1}(\lambda l_b) + w_h \sin \theta_b(\lambda l_b)$ for a rigid heater.

For the m1pf beam, the angle

$$\theta_{a,m1pf}(x) = \int \gamma_{m1pf} \Delta T_{a,m1pf}(x) dx = \gamma_{m1pf} \left(\frac{C_{2,1,m1pf}}{3} x^3 + \frac{C_{1,1,m1pf}}{2} x^2 + C_{0,1,m1pf} x \right), \quad (2.30)$$

assuming $\theta_{a,m1pf}(0) = 0$. Integrating $\theta_{a,m1pf}(x)$ along the length of the beam yields the z -displacement

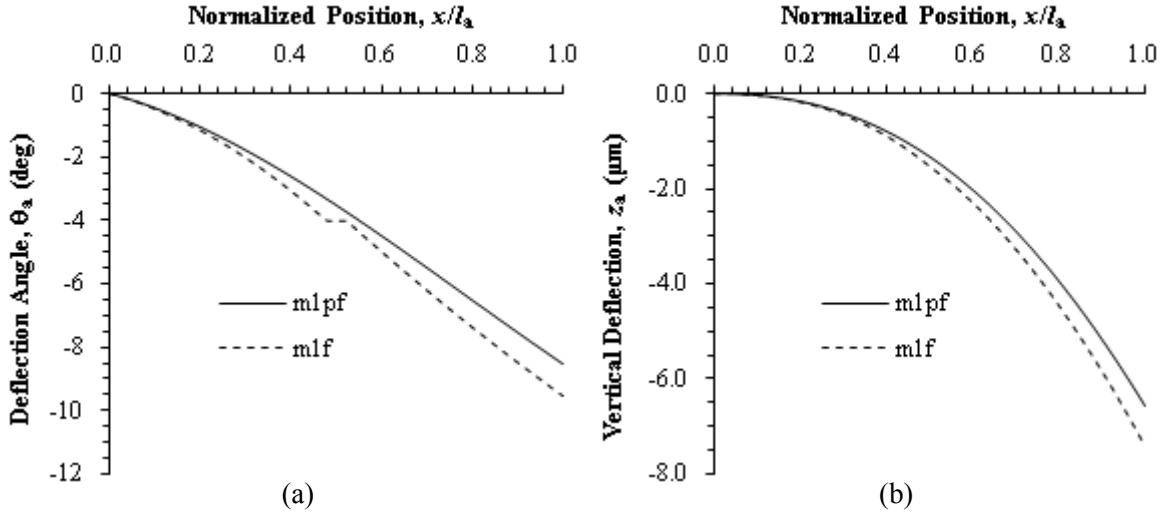
$$z_{a,m1pf}(x) = \gamma_{m1pf} \left(\frac{C_{2,1,m1pf}}{12} x^4 + \frac{C_{1,1,m1pf}}{6} x^3 + \frac{C_{0,1,m1pf}}{2} x^2 \right), \quad (2.31)$$

assuming $z_{a,m1pf}(0) = 0$.

The angular and z -displacements for the beams and temperature distributions shown in Figure 2.14 are shown in Figure 2.15. Only 4% of the 16% difference in the angle at the free end of the beams, $\theta_{tip} = \theta_a(l_a)$, is due to the difference in the thermal sensitivities of the two beam types because $w_{mp} = 0.4 \mu\text{m}$ for $w_b = 2 \mu\text{m}$. The remainder of the difference in θ_{tip} for the two beams comes from the

difference in the temperature distribution in the beams. Similarly, 14% of the 18% difference in tip displacement, $z_{\text{tip}} = z_a(l_a)$, is due to the difference in temperature distribution.

FIGURE 2.15 Graphs of (a) angular displacement $\theta_a(x)$ and (b) z -displacement $z_a(x)$ for the beams and temperature distributions shown in Figure 2.14.



The shape functions of the beam for angular and z -displacement are necessary for an understanding of the behavior of the actuator, but it is the θ_{tip} and z_{tip} of the free end of the beam that are ultimately the parameters of interest as they directly translate to the position of the mirror. The tip angle of the m1f beam with discrete heater resistors is

$$\theta_{\text{tip,m1f}} = \gamma_{\text{m1f}}(l_a - w_h) \left(\frac{C_{1,2,\text{m1f}} + (C_{1,1,\text{m1f}} - C_{1,2,\text{m1f}})\lambda^2}{2} (l_a - w_h) \right. \\ \left. + C_{0,2,\text{m1f}} + (C_{0,1,\text{m1f}} - C_{0,2,\text{m1f}})\lambda \right) \quad (2.32)$$

and the tip displacement is

$$z_{\text{tip,m1f}} = \frac{\gamma_{\text{m1f}}(l_a - w_h)^2}{2} \left(\frac{C_{1,2,\text{m1f}} + (C_{1,1,\text{m1f}} - C_{1,2,\text{m1f}})(3 - 2\lambda)\lambda^2}{3} (l_a - w_h) \right. \\ \left. + C_{0,2,\text{m1f}} + (C_{0,1,\text{m1f}} - C_{0,2,\text{m1f}})(2 - \lambda)\lambda \right) + w_h \sin \theta_{a,\text{m1f}}(\lambda l_b) \quad (2.33)$$

The tip angle of the m1pf beam is

$$\theta_{\text{tip,m1pf}} = \gamma_{\text{m1pf}} l_a \left(\frac{C_{2,1,\text{m1pf}}}{3} l_a^2 + \frac{C_{1,1,\text{m1pf}}}{2} l_a + C_{0,1,\text{m1pf}} \right) \quad (2.34)$$

and the tip displacement is

$$z_{\text{tip,m1pf}} = \frac{\gamma_{\text{m1pf}} l_a^2}{2} \left(\frac{C_{2,1,\text{m1pf}}}{6} l_a^2 + \frac{C_{1,1,\text{m1pf}}}{3} l_a + C_{0,1,\text{m1pf}} \right). \quad (2.35)$$

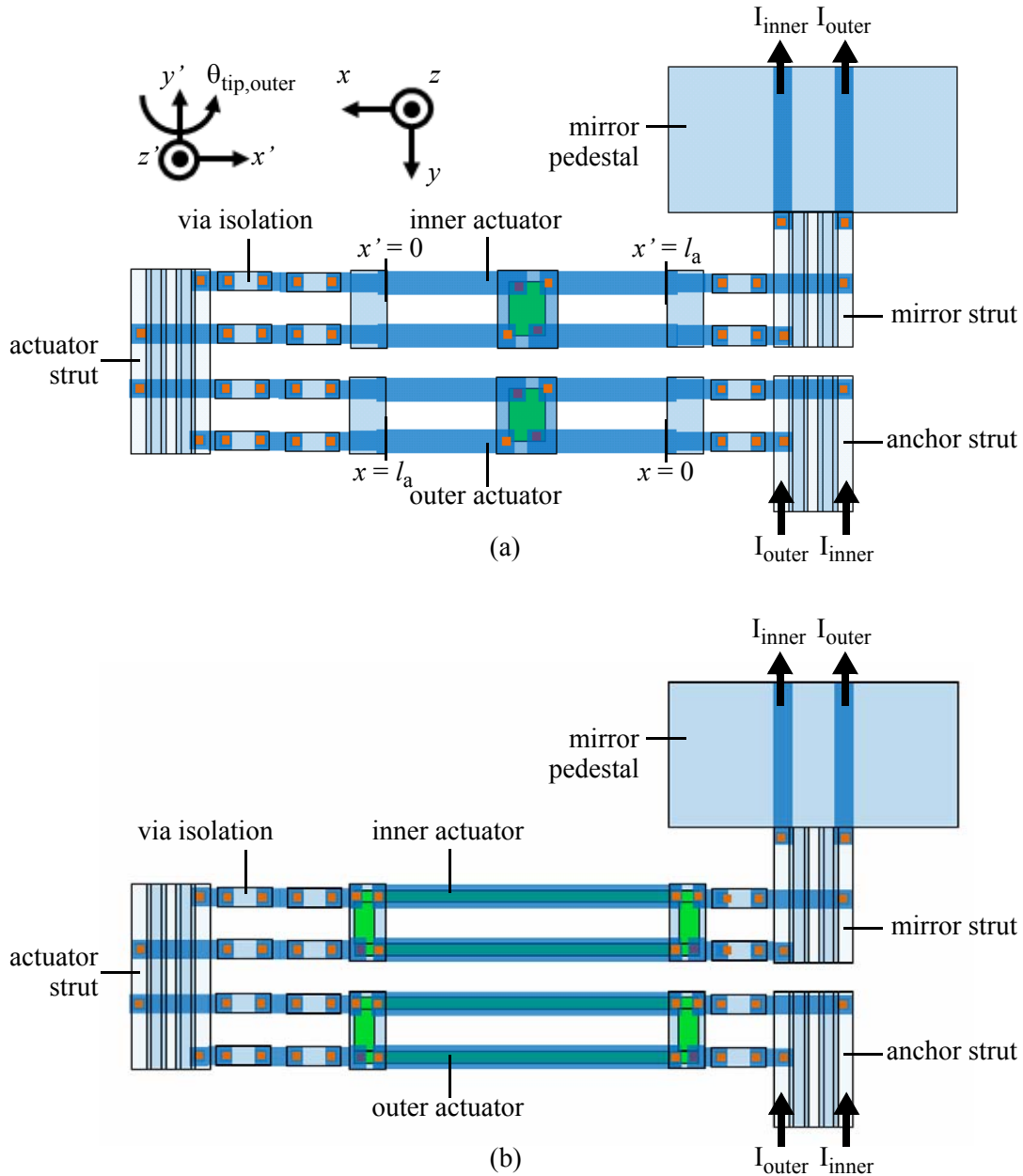
This section raises many questions related to the temperature distribution in the beams. They are answered in the next section when the thermal design is analyzed. But this section demonstrates how to assess electrothermal actuator compositions of two or more members using Timoshenko's bimorph theory and a multimorph theory, respectively. The common types of vertical electrothermal actuator available to the MEMS designer are examined. It is shown that there are two advantages to using the m1f beam with discrete heaters as opposed to an m1pf beam: 1. an inherently better thermal sensitivity γ and 2. a temperature distribution with a higher maximum temperature for a given input power. It is also shown that an m1a beam can be substituted for an m1f beam to produce an 8% higher γ than the m1f beam. However, the issue of the heater width in an m1f or m1a beam becomes significant as the actuator scales down. This is addressed in the following section.

2.3 Actuator Thermal Design

As shown above, electrothermal actuation occurs when the temperature of a bimorph or multimorph of suitable configuration and material properties is heated. In this section, the thermal properties of a folded electrothermal actuator and the mirror it actuates are analyzed to derive an expression for the temperature change distribution in terms of the geometry, material properties and configuration of the elements. The power scaling of the two actuator beam types is derived and the optimal placement of the heater resistor along the m1f beam is determined. The goal in this section is to highlight

the design trade-offs between the m1a/m1f beams with discrete heater resistors and m1pf beams as the micromirrors are scaled down and to demonstrate how the different thermal isolation elements contribute to overall device performance.

FIGURE 2.16 Detailed plan-view schematics of the elements considered in the thermal analysis of the micromirror system for (a) a m1a-based actuator with discrete heater resistors and (b) a m1pf-based actuator.



2.3.1 *Folded Electrothermal Actuator Thermal Model*

A schematic of a folded electrothermal actuator is shown in Figure 2.16. There are two legs to the actuator, identified as “outer”, which is connected to the anchor and “inner” which is connected to the mirror pedestal. The convention for reference directions is shown in Figure 2.16. The reader should note that for the purposes of analysis, the origin of the inner actuator is taken from the end at which it is joined to the outer actuator, and its reference frame (x', y', z') rotates with the tip of the outer actuator. In this way, the equations derived in this section can be applied equally to both inner and outer legs of the actuator. The elements considered in the thermal analysis are the struts connecting the actuators to each other, the mirror and the anchor, the via isolation units designed to increase the localization of the temperature gradients, the bimorph/multimorph beams, the resistive heater and the pedestal being actuated.

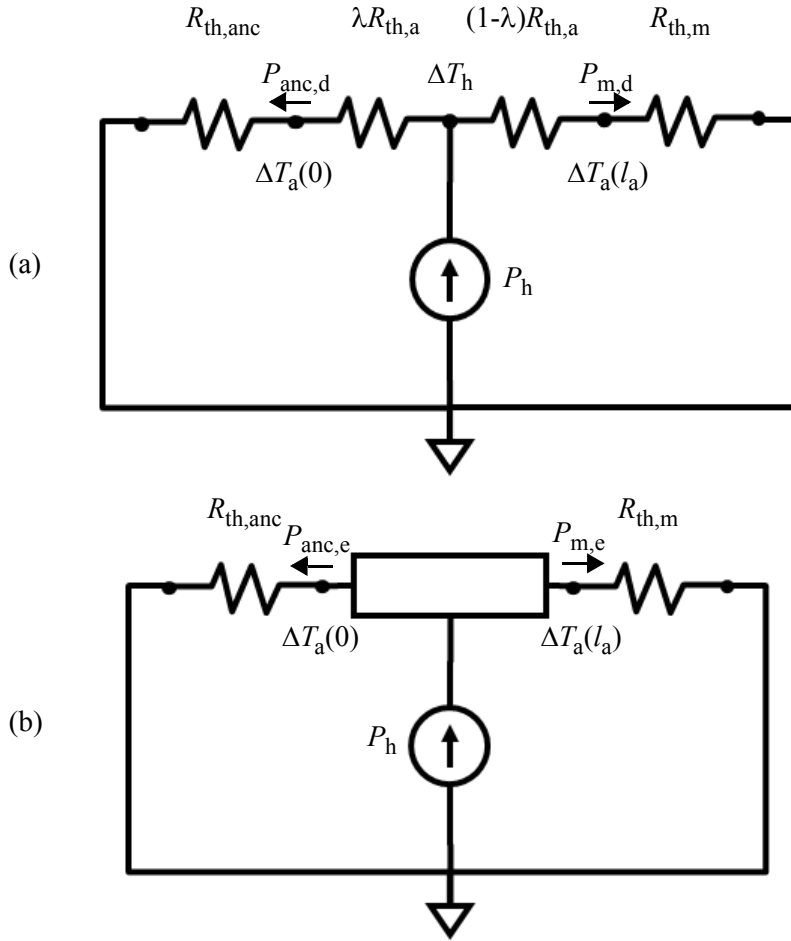
In general, convection and conduction through air to the substrate occurs for each element in the device, however a detailed 2-D analysis of an electrothermally actuated mirror by Lammel et al. [30] that considered these factors, found only 2% of heat in their device was lost to free convection from the actuator (for convection coefficient $h_{\text{conv}} = 10 \text{ Wm}^{-2}\text{K}^{-1}$). Exact analytic solutions exist for the temperature distribution in a thermally conducting beam due to heat loss from its surface [56]. Examination of these exact analytic distributions find agreement with Lammel’s observation. For example, the temperature drop along a cantilever whose base is maintained at $100 \text{ }^\circ\text{C}$ increases from $0.1 \text{ }^\circ\text{C}$ to $2.6 \text{ }^\circ\text{C}$ as the general thermal transport coefficient h_{th} increases from $10 \text{ Wm}^{-2}\text{K}^{-1}$ to $250 \text{ Wm}^{-2}\text{K}^{-1}$ (h_{th} is defined to encompass all surface loss mechanisms). However, Lammel et al. found that convection and conduction through air to the substrate by the mirror did contribute a significant heat loss to the device (10%) due to its relatively large area. More importantly, Lammel et al.’s analysis showed that the modeled shapes of the temperature distributions in their device were not altered by changing the values of the parameters describing free convection and air conduction, only the magnitudes were affected. In effect, air conduction and convection represent a distributed load that globally suppresses

the temperature response of the various elements of the device. In light of this, a 1-D analysis of all the elements, with the exception of the pedestal, is deemed sufficient to first order, to understand the effect on θ_{tip} and z_{tip} of varying thermal isolation, heater placement and pedestal size as the devices are scaled down. Air conduction and free convection from the pedestal to the substrate and surrounding air are modeled as a single thermal resistance. The reader should note that the convection and air conduction losses scale with area, so their impact reduces as the device scales down, however, the surface area to volume ratio increases and convection losses increase, as shown in Section 2.3.4, proportional to conduction losses through the solid. This effect could bear further scrutiny but is beyond the scope of this work.

With the exception of the beams, in which a true temperature distribution is desired, only the temperature drops across the other thermal elements of the device are needed and they are treated as lumped elements. The lumped, 1-D thermal resistance of the elements are $R_{\text{th},v}$ for a bank of via isolation units (i.e. a number $N_{p,v}$ in parallel), $R_{\text{th},s,a}$, $R_{\text{th},s,m}$ and $R_{\text{th},s,anc}$ for the struts joining the actuators, connected to the mirror and connected to the anchor, respectively, and $R_{\text{th},ped}$ for the pedestal. The lumped resistance of each leg of the actuator, $R_{\text{th},a}$, is also a necessary quantity as shown below.

With respect to a particular actuator, inner or outer, the 1-D lumped thermal resistances of all the thermal elements between the actuator and ground can be grouped into two parameters: $R_{\text{th},anc}$, the thermal resistance to the anchor side and $R_{\text{th},m}$, the thermal resistance to the mirror side, which allows each actuator to be represented as the equivalent circuits shown in Figure 2.17. The exact value of each thermal resistance depends on which part of the actuator is considered.

FIGURE 2.17 Equivalent steady state thermal circuit schematics for (a) the mI^* type actuator and (b) the mI_{pf} type actuator.



For the outer actuators in Figure 2.16 (a) and (b)

$$R_{th,anc,outer} = N_{s,v}R_{th,v} + R_{th,s,anc}, \quad (2.36)$$

and

$$R_{th,m,outer} = N_{s,v}R_{th,v} + R_{th,a} + R_{th,s,a} + R_{th,s,m} + R_{th,ped}. \quad (2.37)$$

Similarly, for the inner actuator

$$R_{th,anc,inner} = N_{s,v}R_{th,v} + R_{th,a} + R_{th,s,a} + R_{th,s,anc}, \quad (2.38)$$

and

$$R_{\text{th,m,inner}} = N_{\text{s,v}} R_{\text{th,v}} + R_{\text{th,s,m}} + R_{\text{th,ped}}, \quad (2.39)$$

where $N_{\text{s,v}}$ is the number of thermal isolation banks in series in any particular heat path.

The heat power dissipated in the actuator in both cases for an applied voltage V is

$$P_{\text{h}} = \frac{N_{\text{p,e}} V^2}{N_{\text{s,e}} R_{\text{h}}}, \quad (2.40)$$

where, $N_{\text{s,e}}$ and $N_{\text{p,e}}$ are the number of heaters electrically connected in series and parallel, respectively.

Equations (2.36) to (2.39) embody the crux of the problem in optimizing the thermal performance of the folded electrothermal actuator: the resistance to heat flow is not the same in each direction and are not equivalent for the inner and outer actuators. Values for each parameter are determined analytically or by FEA in Section 2.3.4, but the next step is to apply the above equations to determine the temperature distributions by solving the heat equations for the inner and outer actuators and for m1a/m1f and m1pf beams. The reader should note that R_{h} is also dependent on temperature and its treatment as a constant is an approximation. Todd et al [54] and Lammel et al. [30] addressed this issue and it is felt its inclusion in this analysis would not significantly change the conclusions but would add considerable complexity to the analytic expressions.

2.3.2 Multimorph Actuator Response with Discrete Heaters

It is shown in Section 2.2.3 how the shape functions of the actuator beams depend on the coefficients of the temperature change distributions in the beam. The general form of the distributions arise from the heat equation for isotropic media,

$$(\rho_{\text{d}} C_{\text{p}})_{\text{eff,b}} \Delta \dot{T}_{\text{a,d}} = \kappa_{\text{eff,b}} \nabla^2 \Delta T_{\text{a,d}} + Q_{\text{G}} - Q_{\text{L}}, \quad (2.41)$$

where ρ_d is material density, C_p is specific heat capacity at constant pressure, $(\rho_d C_p)_{\text{eff},b}$ is the effective heat capacity of the beam per unit volume, $\kappa_{\text{eff},b}$ is the effective thermal conductivity of the beam, Q_G is the rate of heat generation in the beam per unit volume and Q_L is the rate of heat loss in the beam per unit volume.

The analysis here is steady-state so $\Delta \dot{T}_{a,d} = 0$. For multimorph beams with discrete resistor heaters, there is no heat source, or heat sink, in the beam so both Q_G and Q_L are zero. Convection and air conduction are assumed negligible in the beam, so only conduction along the length of the beam is considered. Therefore,

$$\frac{d^2 \Delta T_{a,d}}{dx^2} = 0 \quad (2.42)$$

and the distribution is linear, such that $\Delta T_{a,d}(x) = C_1 x + C_0$.

The beam is divided into two sections by the heater. The coefficients of the temperature change distribution must be found for each section. This is done by determining ΔT_h through thermal circuit analysis:

$$\Delta T_h = P_h R_{th} = P_h \cdot \frac{(\lambda R_{th,a} + R_{th,anc})((1 - \lambda)R_{th,a} + R_{th,m})}{R_{th,anc} + R_{th,a} + R_{th,m}}. \quad (2.43)$$

The denominator of (2.43) recurs frequently enough in this chapter that it is replaced by $R_{th,\text{sum}}$ (i.e. the sum of all the thermal resistances in the system). ΔT_h is consequently the maximum temperature change ΔT_{max} in the discrete resistor heater actuator. Similarly,

$$P_{\text{anc},d} = \frac{\Delta T_h}{\lambda R_{th,a} + R_{th,anc}} = P_h \cdot \frac{(1 - \lambda)R_{th,a} + R_{th,m}}{R_{th,\text{sum}}} \quad (2.44)$$

and

$$P_{m,d} = \frac{\Delta T_h}{(1-\lambda)R_{th,a} + R_{th,m}} = P_h \cdot \frac{\lambda R_{th,a} + R_{th,anc}}{R_{th,sum}}, \quad (2.45)$$

which are needed to determine the angular displacement of the non-powered actuator.

The heat power flowing to the anchor and mirror determines the temperatures at the ends of the beam:

$$\Delta T_{a,d}(0) = P_{anc,d} R_{th,anc} = P_h \cdot \frac{((1-\lambda)R_{th,a} + R_{th,m})R_{th,anc}}{R_{th,sum}} \quad (2.46)$$

and

$$\Delta T_{a,d}(l_a) = P_{m,d} R_{th,m} = P_h \cdot \frac{(\lambda R_{th,a} + R_{th,anc})R_{th,m}}{R_{th,sum}}. \quad (2.47)$$

The known temperatures, ΔT_h , $\Delta T_a(0)$ and $\Delta T_a(l_a)$ are used to determine the coefficients of the temperature change distributions in the beam so (2.20) and (2.22) are re-written as

$$\Delta T_{a,d}(x) = P_h \cdot \frac{(1-\lambda)R_{th,a} + R_{th,m}}{R_{th,sum}} \left(\frac{R_{th,a}}{l_a - w_h} x + R_{th,anc} \right) \text{ for } x \leq \lambda l_b, \quad (2.48)$$

$$\Delta T_{a,d}(x) = P_h \cdot \frac{(\lambda R_{th,a} + R_{th,anc})((1-\lambda)R_{th,a} + R_{th,m})}{R_{th,sum}} \text{ for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.49)$$

and

$$\Delta T_{a,d}(x) = P_h \cdot \frac{\lambda R_{th,a} + R_{th,anc}}{R_{th,sum}} \left(-\frac{R_{th,a}}{l_a - w_h} x + R_{th,a} + R_{th,m} \right) \text{ for } x > \lambda l_b + w_h. \quad (2.50)$$

Equations (2.24) to (2.29), (2.32) and (2.33) are now presented in their general forms:

$$\theta_{a,d}(x) = \gamma P_h \cdot \frac{(1-\lambda)R_{th,a} + R_{th,m}}{R_{th,sum}} \left(\frac{R_{th,a}}{2(l_a - w_h)} x^2 + R_{th,anc} x \right) \text{ for } x \leq \lambda l_b, \quad (2.51)$$

$$\theta_{a,d}(x) = \gamma P_h \lambda l_b \cdot \frac{[(1-\lambda)R_{th,a} + R_{th,m}] \left[\frac{\lambda R_{th,a}}{2} + R_{th,anc} \right]}{R_{th,sum}} \quad \text{for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.52)$$

$$\theta_{a,d}(x) = \gamma P_h \cdot \left[\frac{\lambda R_{th,a} + R_{th,anc}}{R_{th,sum}} \left(-\frac{R_{th,a}}{2(l_a - w_h)} (x - w_h)^2 \right. \right. \\ \left. \left. + (R_{th,a} + R_{th,m})(x - w_h) \right) - \lambda^2 \frac{R_{th,a}(l_a - w_h)}{2} \right] \quad \text{for } x > \lambda l_b + w_h, \quad (2.53)$$

$$z_{a,d}(x) = \gamma \frac{P_h}{2} \cdot \frac{(1-\lambda)R_{th,a} + R_{th,m}}{R_{th,sum}} \left(\frac{R_{th,a}}{3(l_a - w_h)} x^3 + R_{th,anc} x^2 \right) \quad \text{for } x \leq \lambda l_b, \quad (2.54)$$

$$z_{a,d}(x) = \gamma \frac{P_h (\lambda l_b)^2}{2} \cdot \frac{[(1-\lambda)R_{th,a} + R_{th,m}] \left[\frac{\lambda R_{th,a}}{3} + R_{th,anc} \right]}{R_{th,sum}} \quad \text{for } \lambda l_b < x \leq \lambda l_b + w_h, \quad (2.55)$$

$$+ (x - \lambda l_b) \sin \theta_{a,d}(\lambda l_b)$$

$$z_{a,d}(x) = \gamma \frac{P_h}{2} \cdot \left[\frac{\lambda R_{th,a} + R_{th,anc}}{R_{th,sum}} \left(-\frac{R_{th,a}}{3(l_a - w_h)} (x - w_h)^3 \right. \right. \\ \left. \left. + (R_{th,a} + R_{th,m})(x - w_h)^2 \right) - \lambda^2 R_{th,a}(l_a - w_h) \left((x - w_h) - \frac{\lambda(l_a - w_h)}{3} \right) \right] \quad \text{for } x > \lambda l_b + w_h, \quad (2.56)$$

$$+ w_h \sin \theta_{a,d}(\lambda l_b)$$

$$\theta_{tip,d} = \gamma (l_a - w_h) \cdot \frac{P_h R_{th,a}}{2 R_{th,sum}} \left[R_{th,anc} (1 + \lambda)(1 - \lambda) + R_{th,a} \lambda (1 - \lambda) \right. \\ \left. + R_{th,m} \lambda (2 - \lambda) + \frac{2 R_{th,anc} R_{th,m}}{R_{th,a}} \right] \quad (2.57)$$

and

$$z_{\text{tip,d}} = \frac{\gamma(l_a - w_h)^2}{2} \cdot \frac{P_h R_{\text{th,a}}}{3R_{\text{th,sum}}} \left[R_{\text{th,anc}}(2 - 3\lambda^2 + \lambda^3) + R_{\text{th,a}}(2\lambda - 3\lambda^2 + \lambda^3) \right. \\ \left. + R_{\text{th,m}}(3\lambda - 3\lambda^2 + \lambda^3) + \frac{3R_{\text{th,anc}}R_{\text{th,m}}}{R_{\text{th,a}}} \right] + w_h \sin \theta_{\text{a,d}}(\lambda l_b) \quad (2.58)$$

Equations (2.51) to (2.58) are used directly to analyze the electrothermomechanical response of a multimorph beam with discrete heater resistors for any combination of thermal isolation. Additionally, (2.57) contains the average temperature change of the beam

$$\Delta \bar{T}_{\text{a,d}} = \frac{P_h R_{\text{th,a}}}{2R_{\text{th,sum}}} \left[R_{\text{th,anc}}(1 + \lambda)(1 - \lambda) + R_{\text{th,a}}\lambda(1 - \lambda) + R_{\text{th,m}}\lambda(2 - \lambda) + \frac{2R_{\text{th,anc}}R_{\text{th,m}}}{R_{\text{th,a}}} \right], \quad (2.59)$$

which is used later to compare the shape functions of beams with different temperature distributions.

2.3.3 Multimorph Actuator Response with Distributed Heaters

The heat equation

$$(\rho_d C_p)_{\text{eff,b}} \Delta \dot{T}_{\text{a,e}} = \kappa_{\text{eff,b}} \nabla^2 \Delta T_{\text{a,e}} + Q_G - Q_L \quad (2.60)$$

for beams with isotropic members and resistive films embedded along their length has a different solution than that for discrete resistor heaters. With the conditions of steady-state operation and no internal heat sinks and the assumption of no losses from the surface of the beam, the heat equation simplifies to

$$\frac{d^2 \Delta T_{\text{a,e}}}{dx^2} = -\frac{Q_G}{\kappa_{\text{eff,b}}}, \quad (2.61)$$

where

$$Q_G = \frac{P_h}{N_{\text{p,b}} w_b t_b l_b} \quad (2.62)$$

is the heat generation in the beam per unit volume.

Integrating (2.61) twice gives the polynomial temperature distribution in (2.23) for which the coefficients must be determined, $\Delta T_{a,e}(x) = C_{2,e}x^2 + C_{1,e}x + C_{0,e}$. $C_{2,e}$ is found directly from the integration, but derivation of $C_{1,e}$ and $C_{0,e}$ is more involved. From the conservation of energy

$$P_h = P_{anc,e} + P_{m,e}. \quad (2.63)$$

From thermal circuit analysis,

$$\Delta T_{a,e}(0) = P_{anc,e}R_{th,anc} = C_{0,e} \quad (2.64)$$

and

$$\Delta T_{a,e}(l_a) = P_{m,e}R_{th,m}. \quad (2.65)$$

Together, (2.64) and (2.65) are used to derive an expression for $C_{1,e}$ which is substituted into (2.23) to give

$$\Delta T_{a,e}(x) = -\frac{Q_G}{2\kappa_{eff,b}}x^2 + \left(\frac{P_{m,e}R_{th,m}}{l_a} - \frac{P_{anc,e}R_{th,anc}}{l_a} + \frac{Q_G l_a}{2\kappa_{eff,a}} \right)x + P_{anc,e}R_{th,anc}. \quad (2.66)$$

Fick's law is then used to derive expressions for the boundary conditions for the first derivative of $\Delta T_{a,e}$ at $x = 0$ and $x = l_a$ that provide the additional equations to solve for $P_{anc,e}$ and $P_{m,e}$ which lead to

$$P_{anc,e} = P_h \cdot \frac{\frac{R_{th,a}}{2} + R_{th,m}}{R_{th,sum}} \quad (2.67)$$

and

$$P_{m,e} = P_h \cdot \frac{R_{th,anc} + \frac{R_{th,a}}{2}}{R_{th,sum}}. \quad (2.68)$$

Further, it is noted that for an m1pf beam $l_b = l_a$ which leads to

$$\frac{Q_G}{\kappa_{\text{eff},b}} = \frac{P_h}{\kappa_{\text{eff},b} N_{p,b} w_b t_b l_b} = P_h \frac{l_a}{\kappa_{\text{eff},b} N_{p,b} w_b t_b} \cdot \frac{1}{l_a^2} = \frac{P_h R_{\text{th},b}}{l_a^2 N_{p,b}} = \frac{P_h R_{\text{th},a}}{l_a^2}. \quad (2.69)$$

These expressions are substituted into (2.66) to produce

$$\Delta T_{a,e}(x) = P_h \left(-\frac{R_{\text{th},a}}{2l_a^2} x^2 + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},a}}{l_a R_{\text{th},\text{sum}}} x + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},\text{anc}}}{R_{\text{th},\text{sum}}} \right). \quad (2.70)$$

The maximum temperature in the beam is found by differentiating (2.70) and equating it to zero to obtain

$$\Delta T_{\text{max},e} = \frac{P_h \left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right)}{R_{\text{th},\text{sum}}} \left(\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) \frac{R_{\text{th},a}}{2} + R_{\text{th},\text{anc}} R_{\text{th},\text{sum}} \right). \quad (2.71)$$

The coefficients of (2.70) are substituted into equations (2.30), (2.31), (2.34) and (2.35) to obtain:

$$\theta_{a,e}(x) = \gamma P_h \left(-\frac{R_{\text{th},a}}{6l_a^2} x^3 + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},a}}{2l_a R_{\text{th},\text{sum}}} x^2 + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},\text{anc}}}{R_{\text{th},\text{sum}}} x \right), \quad (2.72)$$

$$z_{a,e}(x) = \gamma P_h \left(-\frac{R_{\text{th},a}}{24l_a^2} x^4 + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},a}}{6l_a R_{\text{th},\text{sum}}} x^3 + \frac{\left(\frac{R_{\text{th},a}}{2} + R_{\text{th},m}\right) R_{\text{th},\text{anc}}}{2R_{\text{th},\text{sum}}} x^2 \right), \quad (2.73)$$

$$\theta_{\text{tip},e} = \gamma l_a \frac{P_h R_{\text{th},a}}{R_{\text{th},\text{sum}}} \left(\frac{R_{\text{th},\text{anc}}}{3} + \frac{R_{\text{th},a}}{12} + \frac{R_{\text{th},m}}{3} + \frac{R_{\text{th},m} R_{\text{th},\text{anc}}}{R_{\text{th},a}} \right) \quad (2.74)$$

and

$$z_{\text{tip,e}}(x) = \frac{\gamma l_a^2 P_h R_{\text{th,a}}}{2 R_{\text{th,sum}}} \left(\frac{5R_{\text{th,anc}}}{12} + \frac{R_{\text{th,a}}}{12} + \frac{R_{\text{th,m}}}{4} + \frac{R_{\text{th,m}} R_{\text{th,anc}}}{R_{\text{th,a}}} \right). \quad (2.75)$$

Equations (2.72) to (2.75) are used directly to analyze the electrothermomechanical response of a multimorph beam with embedded resistive layers along the beam length for any combination of thermal isolation. Additionally, (2.57) contains the average temperature of the beam

$$\Delta \bar{T}_{\text{a,e}} = \frac{P_h R_{\text{th,a}}}{R_{\text{th,sum}}} \left(\frac{R_{\text{th,anc}}}{3} + \frac{R_{\text{th,a}}}{12} + \frac{R_{\text{th,m}}}{3} + \frac{R_{\text{th,m}} R_{\text{th,anc}}}{R_{\text{th,a}}} \right), \quad (2.76)$$

which is used later to compare the shape functions of beams with different temperature distributions.

2.3.4 Thermal Resistance of Device Elements

To use the equations in Section 2.3.2 and Section 2.3.3, the thermal resistances of the various elements must be known. This subsection details how these quantities are calculated analytically, approximated using FEA or inferred based on the literature.

The thermal resistance to heat conduction through a piece of homogeneous solid material of length l , width w , thickness t and thermal conductivity κ is

$$R_{\text{th,cond}} = \frac{l}{\kappa w t}. \quad (2.77)$$

When N_p such elements are arrayed in parallel, such that the temperature difference across each is equal, the thermal resistance becomes

$$R_{\text{th,cond}} = \frac{l}{N_p \kappa w t}, \quad (2.78)$$

and similarly if N_s of the N_p parallel elements are arrayed in series, such that the same heat flux flows in each,

$$R_{\text{th,cond}} = \frac{N_s l}{N_p \kappa w t} \quad (2.79)$$

The lumped thermal resistance of the mirror pedestal is calculated using an effective heat transfer coefficient h_{th} that models two surface heat loss mechanisms. For a structure of surface area A , the thermal resistance to heat loss from the surface is

$$R_{\text{th,surf}} = \frac{1}{h_{\text{th}} A} \quad (2.80)$$

The heat transfer coefficient h_{th} comprises heat transfer through convection (h_{conv}) and heat transfer by conduction through the air surrounding the structure to the substrate (h_{cond}), such that

$$h_{\text{th}} = h_{\text{conv}} + h_{\text{cond}} \quad (2.81)$$

The value of h_{conv} is found analytically using the Nusselt number of the structure [56], assuming a shape and orientation dependent correlation function, and lies in the range from $5 \text{ Wm}^{-2}\text{K}^{-1}$ to $15 \text{ Wm}^{-2}\text{K}^{-1}$ for MEMS structures from micron to mm scale. However, 3-D heat transfer through air is a problem that can only be solved analytically for a narrow set of structures. In this work, h_{cond} is analyzed through FEA.

For the purposes of analysis, the substrate is assumed to have a constant temperature $T_0 = 273 \text{ K}$. As shown in Figure 2.18 (a), the model comprises a square hole of width $\Omega - w_{\text{anc}}$ representing the etch pit around a folded electrothermal actuator and a square plate of width w_{ped} and thickness t_{ped} at the center of the upper plane of the hole represents the pedestal. The pedestal is given a fixed temperature $T_{\text{ped}} = 373 \text{ K}$. The symmetry of the structure allows it to be modeled using a quarter section to reduce the DOF. The temperature distribution and heat flux results from a COMSOL Multiphysics 3-D heat transfer simulation are shown in Figure 2.18 (b) to (e) for two cases: 1. $\Omega - w_{\text{anc}} > w_{\text{ped}}$ (Figure 2.18 (b) and (c)) and 2. $\Omega - w_{\text{anc}} < w_{\text{ped}}$ (Figure 2.18 (d) and (e)). The heat flux in case 1 is predominantly vertical. In case 2, there is significant lateral heat conduction from the pedestal to the

anchor and as Ω decreases lateral conduction through the air from the sidewalls of the pedestal increases in dominance.

FIGURE 2.18 FEA of heat transfer through air from a suspended plate in an etch pit. (a) The model geometry. (b) Temperature distribution in the air in an quarter section of the structure for a large lateral gap between the plate and the sidewall. (c) Heat flux from the plate to the sidewall for a large lateral gap. The length of the arrow represents the magnitude of the heat flux. (d) Temperature distribution in the air for a narrow lateral gap. (e) Heat flux for a narrow lateral gap.

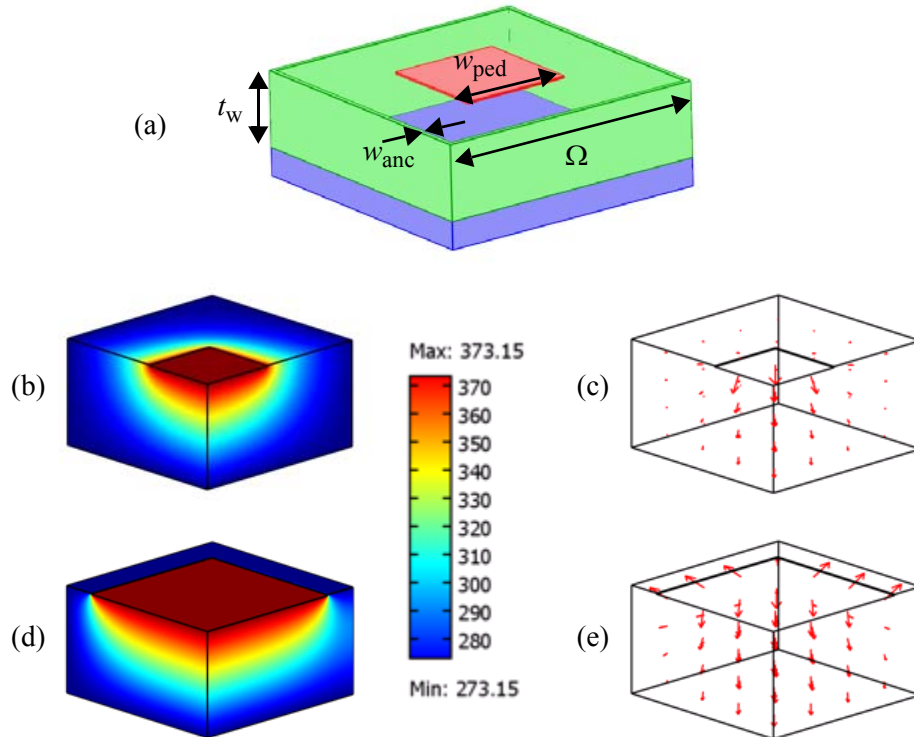
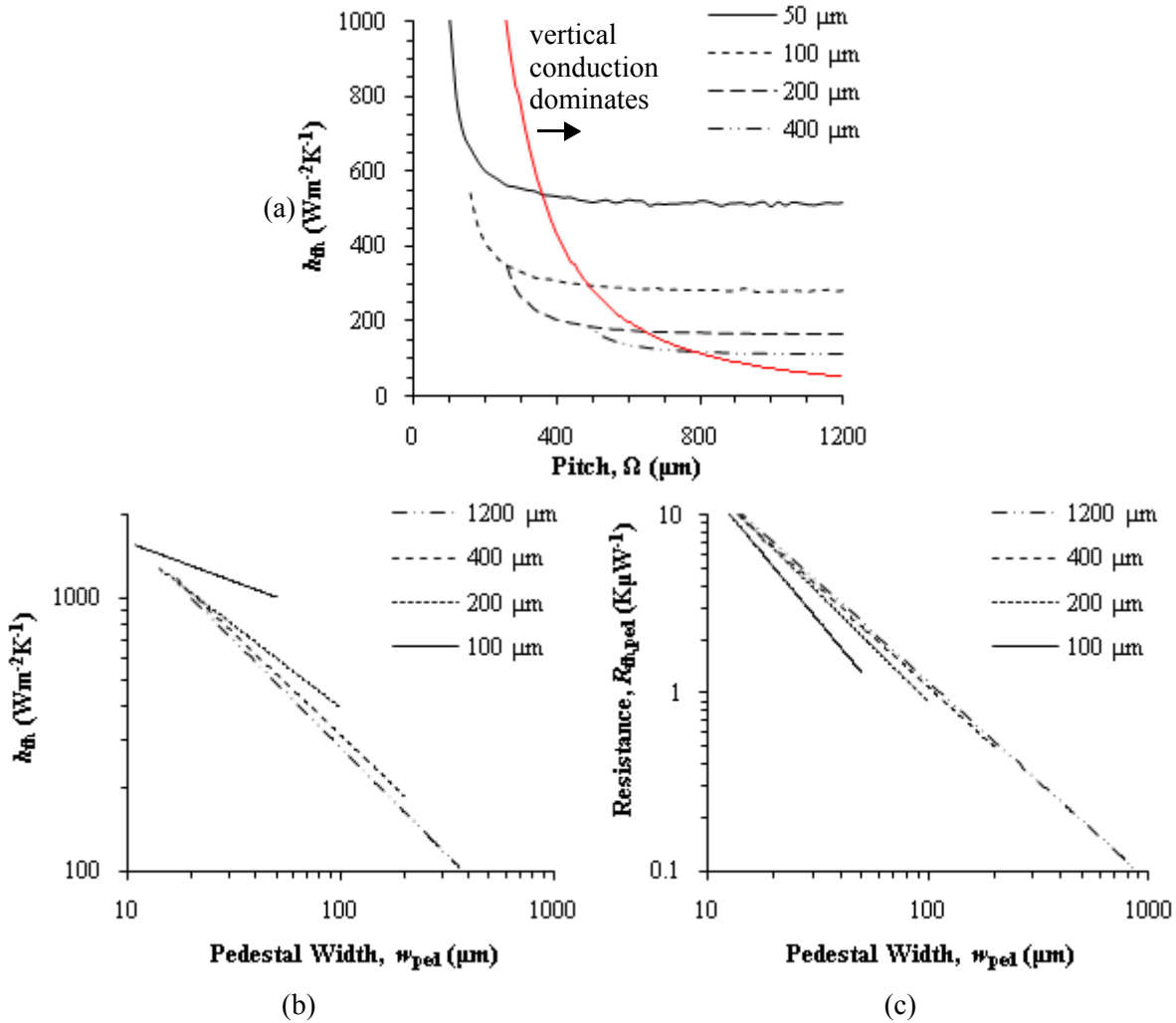


FIGURE 2.19 Trends of h_{th} and $R_{th,ped}$ extracted from FEA simulation over a range of $\Omega - w_{anc}$ and w_{ped} . (a) h_{th} variation with Ω for a number of w_{ped} . The red line is the locus of 5% increase in h_{th} from the constant value at large pitch. (b) h_{th} variation with w_{ped} for a number of Ω (c) $R_{th,ped}$ variation with w_{ped} for a number of Ω



Simulations are performed over a range of $\Omega - w_{anc}$ and w_{ped} and values of h_{cond} are extracted by integrating the heat flux over the pedestal surface and dividing by $T_{ped} - T_0$ and the total pedestal surface area. Values of $R_{th,ped}$ and h_{th} are calculated using (2.80) and (2.81), respectively. Graphs of the trends in these parameters are shown in Figure 2.19. In Figure 2.19 (a), h_{th} is constant over a wide range of Ω for which vertical heat flux dominates. The red line is the locus of 5% change in h_{th} from the constant value at large pitch. It represents the transition from a region of the design space in which vertical air conduction dominates. As t_w decreases, the locus moves towards smaller values of Ω . As w_{anc} increases, the locus moves toward larger values of Ω . As t_{ped} increases, the locus moves towards

higher value of Ω . For values of Ω for which vertical conduction dominates, $R_{\text{th,ped}}$ is approximated using the function $R_{\text{th,ped}} = 38w_{\text{ped}}^{-1.1}$ fitted to the simulation data shown in Figure 2.19 (a).

For a multimorph beam the effective thermal conductivity

$$\kappa_{\text{eff}} = \frac{\sum_{\text{members}} \kappa_i w_i t_i}{\sum_{\text{members}} w_i t_i} \quad (2.82)$$

is used to calculate the effective thermal conductivities of the actuator beams and the struts. For beams comprising only members whose widths equal the beam width, (2.82) simplifies to the thickness weighted average

$$\kappa_{\text{eff}} = \frac{\sum_{\text{members}} \kappa_i t_i}{t_b} \quad (2.83)$$

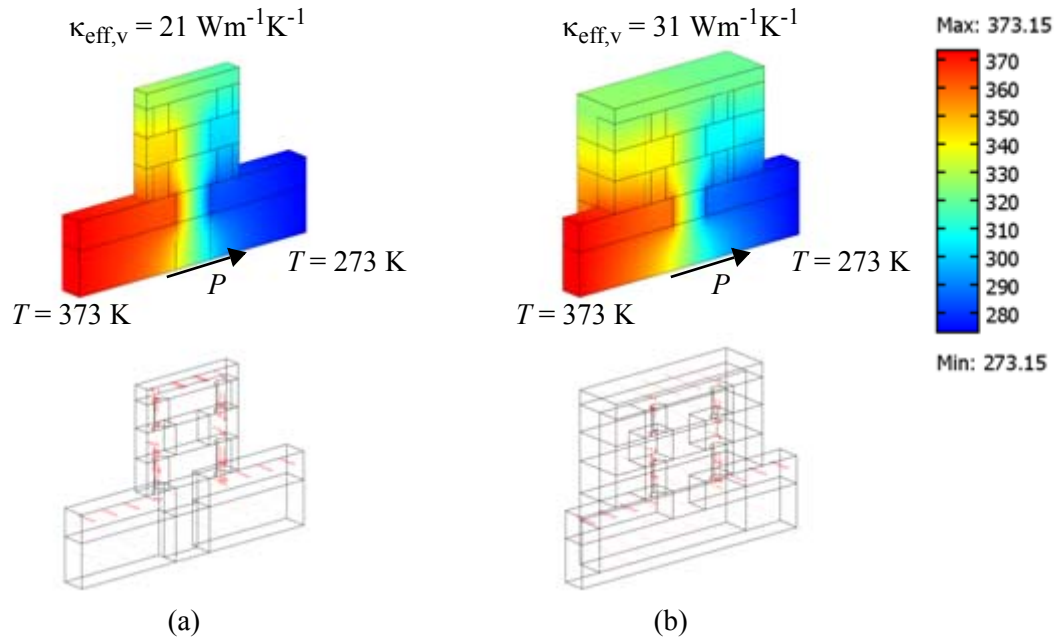
The via isolation structures have a complex 3-D structure as shown in Figure 2.6 and the heat flux lines are not parallel in the structure. This requires the use of FEA to determine κ_{eff} and is done by generating a 3-D model of the structure and applying a known temperature difference ΔT across the ends. By extracting the heat flow through one end, κ_{eff} is calculated using Fick's law:

$$\kappa_{\text{eff}} = -\frac{P_{\text{in}} l}{wt \Delta T} \quad (2.84)$$

Temperature fields and heat flux from a Comsol Multiphysics 3.5 FEA are shown in Figure 2.20 and demonstrate how the heat flow is contained within the via chain. The thermal conductivity values for the simulation are taken from the Comsol Multiphysics Materials Library [52]. The extracted values of $\kappa_{\text{eff,v}}$ for two values of via enclosure are shown in Table 2.4. It is clear that via enclosure limitations are a constraint on the achievement of higher thermal isolation, for example, reducing e_v from

0.9 μm to 0.2 μm reduces $\kappa_{\text{eff},v}$ by 30%. In the CMOS-MEMS technology used for this work, the structures become very hot during release etch (see Chapter 5) and the etch rate of the TiW barrier metals and W vias is accelerated, necessitating larger via enclosures. If this effect could be prevented by sidewall encapsulation by oxide, or some other material, the thermal isolation of the devices could be enhanced and better performance could be achieved.

FIGURE 2.20 Thermal FEA on via isolation structure of the type shown in Figure 2.6 (a) to extract $\kappa_{\text{eff},v}$ for (a) $e_v = 0.2 \mu\text{m}$ and (b) $e_v = 0.9 \mu\text{m}$. The upper image shows the temperature field for a fixed $\Delta T = 100 \text{ K}$ across the length and the lower image shows an arrow plot of the heat flux. The length of the red arrows is proportional to the heat flux.



The effective thermal conductivities of various CMOS-MEMS beam types are given in Table 2.4. The values are calculated using (2.82) with $\kappa_{\text{SiO}_2} = 21.4 \text{ Wm}^{-1}\text{K}^{-1}$, $\kappa_{\text{met}} = 191 \text{ Wm}^{-1}\text{K}^{-1}$, $\kappa_{\text{poly}} = 34 \text{ Wm}^{-1}\text{K}^{-1}$ [52]. The thicknesses used in the calculations are mean values of JAZZ layer thicknesses taken over a number of runs. The thermal sheet resistances are also given because the layer thicknesses are fixed for a given beam type and this gives a better comparison of the relative amount of thermal isolation provided by each beam type.

TABLE 2.4 *Effective thermal conductivities and thermal sheet resistances of various CMOS-MEMS multimorph beams based on statistical, measured JAZZ layer thicknesses.*

Beam Type	κ_{eff} in $\text{Wm}^{-1}\text{K}^{-1}$	Thermal Sheet Resistance in $\text{KW}^{-1}/\text{square}$
m1a	71	8961
m1f	67	8950
m1pf	72	8256
m2f	46	6843
m21f	78	4054
m3f	39	5536
m32f	51	4246
m321f	81	2698
m4f	68	1578
m4321f	98	1095
m43 strut	34	3143
via isolation, $e_v = 0.9 \mu\text{m}$	31	-
via isolation, $e_v = 0.2 \mu\text{m}$	21	-

The values of κ_{eff} for each device element are used with the geometric parameters to calculate their thermal resistances. The heaters in m1*-based actuators are treated as thermal shorts as they have a continuous layer of m2 and almost continuous layers of m1 and poly. The thermal resistances are

$$R_{\text{th,a}} = \frac{R_{\text{th,b}}}{N_{\text{p,b}}} = \frac{l_{\text{b}}}{N_{\text{p,b}}\kappa_{\text{eff,b}}w_{\text{b}}t_{\text{b}}}, \quad (2.85)$$

$$R_{\text{th,v}} = \frac{R_{\text{th,iso}}}{N_{\text{p,v}}} = \frac{l_{\text{iso}}}{N_{\text{p,v}}\kappa_{\text{eff,v}}w_{\text{iso}}t_{\text{iso}}}, \quad (2.86)$$

$$R_{\text{th,ped}} = \frac{1}{2h_{\text{th}}l_{\text{ped}}(l_{\text{ped}} + 2t_{\text{ped}})}, \quad (2.87)$$

$$R_{\text{th,s,a}} = \frac{2N_{\text{p,b}}(w_{\text{b}} + g_{\text{b}}) - g_{\text{b}}}{\kappa_{\text{eff,s}}w_{\text{s}}t_{\text{s}}} \quad (2.88)$$

and

$$R_{th,s,anc} = R_{th,s,m} = \frac{N_{p,b}(w_b + g_b)}{\kappa_{eff,s} w_s t_s}. \quad (2.89)$$

An example of the thermal resistances for the topology shown in Figure 2.16 with $l_a = 100 \mu\text{m}$, $w_b = 2 \mu\text{m}$, $g_a = 2 \mu\text{m}$ and $l_{ped} = 50 \mu\text{m}$ are given in Table 2.5. For this set of device parameters the struts contribute 1% at most to the thermal resistance, with the exception of the anchor strut, for which it is $\sim 3.5\%$.

TABLE 2.5 Examples of thermal resistances for the device topology in Figure 2.16.

Device Element	Dimensions (μm)	R_{th} ($\text{K}\mu\text{W}^{-1}$)
m1a actuator, $R_{th,a}$	$l_b = 95.5 \mu\text{m}$, $w_b = 2 \mu\text{m}$, $t_b = 1.57 \mu\text{m}$, $N_{p,b} = 2$, $w_h = 4.5 \mu\text{m}$,	224
m1pf actuator, $R_{th,a}$	$l_b = 100 \mu\text{m}$, $w_b = 2 \mu\text{m}$, $t_b = 1.68 \mu\text{m}$ $N_{p,b} = 2$	207
anchor strut, $R_{th,s,anc}$	$w_s = 11.8 \mu\text{m}$, $g_b = 2 \mu\text{m}$, $t_s = 9.36 \mu\text{m}$	2
actuator strut, $R_{th,s,a}$	as above	4
mirror strut, $R_{th,s,m}$	as above	2
via isolation, $R_{th,v}$	$l_{iso} = 6.6 \mu\text{m}$, $w_{iso} = 1.2 \mu\text{m}$, $t_{iso} = 1.57 \mu\text{m}$, $N_{p,v} = 2$	57
pedestal, $R_{th,ped}$	$w_{ped} = 50 \mu\text{m}$, $t_{ped} = 4.37 \mu\text{m}$	2046
$R_{th,anc,inner}$ for m1a		515
$R_{th,anc,inner}$ for m1pf		498
$R_{th,m,inner}$		2105
$R_{th,anc,outer}$		59
$R_{th,m,outer}$ for m1a		2555
$R_{th,m,outer}$ for m1pf		2538

2.4 Folded Actuator Electrothermomechanical Response

The coupling of two electrothermal actuators to make a folded electrothermal actuator like those shown in Figure 2.16 results in a pedestal motion that depends on the temperature distribution in both

legs of the actuator. This section explores the optimization of the actuator, the angular scan range and the power scaling of the folded electrothermal actuator.

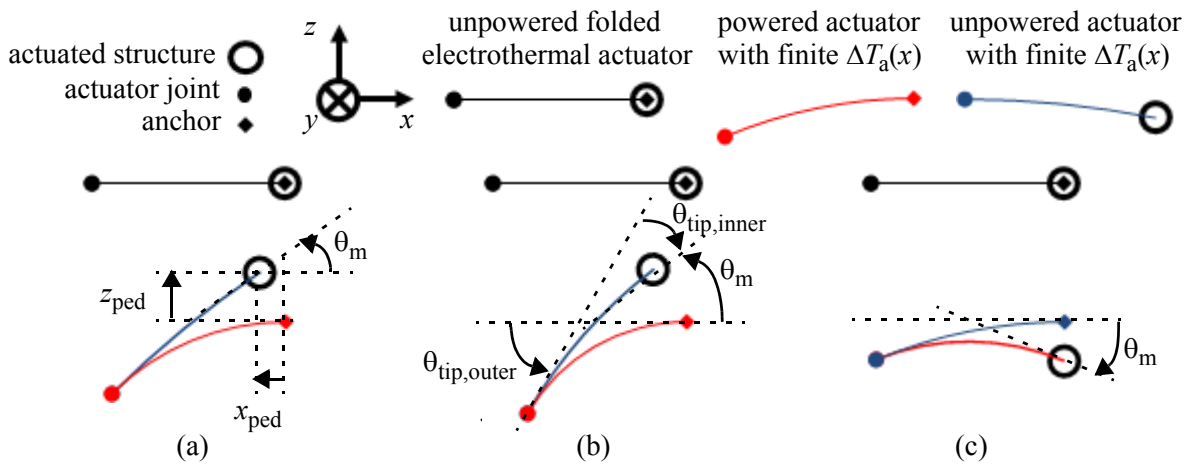
2.4.1 Pedestal Displacement

The devices in Figure 2.16 are abstracted to the line drawings shown in Figure 2.21 to demonstrate the geometric dependence of the angular displacement θ_m , z -displacement z_{ped} and x -displacement x_{ped} of the mirror pedestal on the tip displacements θ_{tip} and z_{tip} of each beam. The “ped” subscripts for the x - and z -displacements reflect that the pedestal and mirror translations are not the same, as shown in Section 2.5.3. The diagrams are conceptual and the reader should note that although they have been drawn using elements of constant curvature, in reality the curvature varies along the length of the beam. The angular displacement of the mirror pedestal as shown in Figure 2.21 (b) when the outer actuator is powered, or in Figure 2.21 (c) when the inner actuator is powered, is

$$\theta_m = \theta_{tip,outer} - \theta_{tip,inner} . \quad (2.90)$$

This formulation is a consequence of the alternate axes for the inner actuator shown in Figure 2.16.

FIGURE 2.21 Abstraction of the folded electrothermal actuator shown in Figure 2.16. The powered actuator is shown in red, while the unpowered actuator is shown in blue. Constant curvature beams are used for indication only. (a) Definition of mirror pedestal angular displacement θ_m and translational displacements x_{ped} and z_{ped} in the x - and z - directions, respectively. (b) Demonstration of θ_m relation to the angular displacements of each actuator in the folded structure with the outer actuator powered. (c) Angular displacement when the inner actuator is powered.



The temperature distribution in the unpowered actuator results from the heat flux from the powered actuator. It is valid for the two actuation cases i.e. inner actuator powered, outer actuator unpowered and vice versa. θ_{tip} for the powered actuators is given by (2.57) and (2.74) and the expressions for θ_{tip} for the unpowered actuators are derived below. A more general form for θ_m would relate all the angles back to the anchor using a single coordinate axis and θ_m would be given by the sum of all tip angles. However, due to the small number of beams and their simple interconnection, (2.90) is acceptable. The author made a cursory investigation of the forward and inverse kinematic problems in the field of robotics for a solution to the problem of many beams with arbitrary interconnections, but could not find an analytic treatment applicable to members of varying curvature. This should be investigated further.

The temperature distribution in the unpowered actuator is derived from Fick's law using the known input heat flows P_{in} taken from (2.44), (2.45), (2.67) and (2.68), the temperature at the nearest end of the powered actuator $\Delta T_{\text{a,near}}$ and the temperature drop across the thermal isolation joining the two actuators. The temperature distribution is

$$\Delta T_{\text{a,un,inner}}(x) = -\frac{P_{\text{in}}}{\kappa_{\text{eff,b}} w_b t_b} x + \Delta T_{\text{a,near}} - P_{\text{in}} (R_{\text{th,v}} N_{\text{s,v}} + R_{\text{th,s,a}}) \quad (2.91)$$

for the inner unpowered inner actuator and

$$\Delta T_{\text{a,un,outer}}(x) = \frac{P_{\text{in}}}{\kappa_{\text{eff,b}} w_b t_b} x + \Delta T_{\text{a,near}} - P_{\text{in}} (R_{\text{th,v}} N_{\text{s,v}} + R_{\text{th,s,a}} + R_{\text{th,a}}) \quad (2.92)$$

for the outer actuator, where $N_{\text{s,v}}$ is the number of via isolation units in series. For actuators with discrete resistor heaters, when the inner actuator is powered $P_{\text{in}} = P_{\text{anc,d,inner}}$ and $\Delta T_{\text{a,near}} = \Delta T_{\text{a,d,inner}}(0)$ and when the outer actuator is powered $P_{\text{in}} = P_{\text{m,d,outer}}$ and $\Delta T_{\text{a,near}} = \Delta T_{\text{a,d,outer}}(l_a)$. Similarly, for actuators with embedded resistive films along their lengths, when the inner actuator is powered

$P_{in} = P_{anc,e}$ and $\Delta T_{a,near} = \Delta T_{a,e,inner}(0)$ and when the outer actuator is powered $P_{in} = P_{m,e}$ and $\Delta T_{a,near} = \Delta T_{a,e,outer}(l_a)$.

The displacement angle and the z -displacement of the tip of the unpowered actuators are found by integrating (2.91) and (2.92) to obtain

$$\theta_{tip,un} = \gamma l_b \left[\Delta T_{a,near} - P_{in} \left(\frac{R_{th,a}}{2} + R_{th,v} N_{s,v} + R_{th,s,a} \right) \right] \quad (2.93)$$

for both the inner and outer actuators,

$$z_{tip,un,inner} = \frac{\gamma l_b^2}{2} \left[\Delta T_{a,near} - P_{in} \left(\frac{R_{th,a}}{3} + R_{th,v} N_{s,v} + R_{th,s,a} \right) \right], \quad (2.94)$$

for the inner actuator and

$$z_{tip,un,outer} = \frac{\gamma l_b^2}{2} \left[\Delta T_{a,near} - P_{in} \left(\frac{2R_{th,a}}{3} + R_{th,v} N_{s,v} + R_{th,s,a} \right) \right] \quad (2.95)$$

for the outer actuator. In the case of actuators with discrete resistors, (2.94) and (2.95) have additional z -displacement terms of $w_h \sin \theta_{a,d} (\lambda l_b)$ to account for the rigid heater resistor.

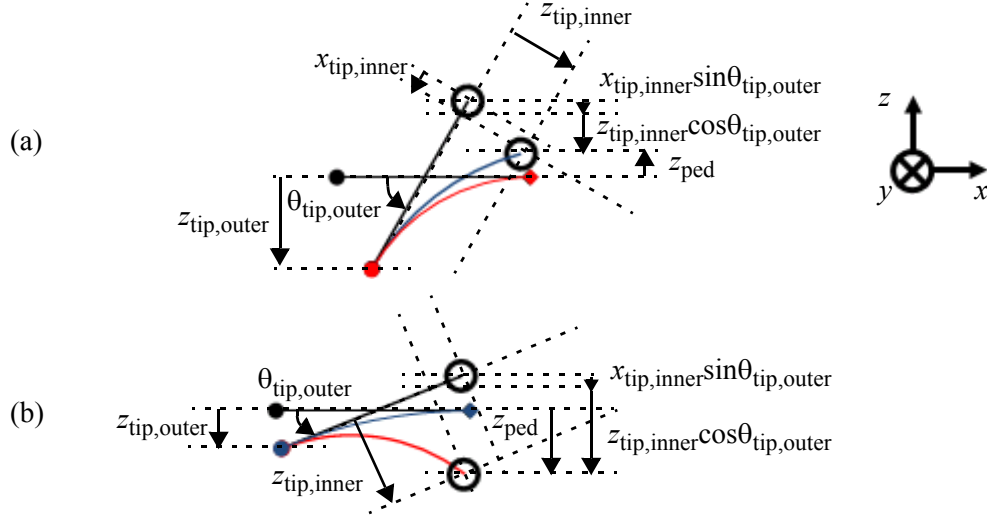
Analysis of the translational displacements of the mirror pedestal is shown in Figure 2.22. The mirror pedestal displacement in the z -direction is approximated geometrically by assuming the curvature of both actuators is constant so that $x_{tip,inner} = -l_a(1 - \text{sinc}\theta_{inner})$, while retaining the exact expressions for the tip angles and z -displacements, which leads to

$$z_{ped} \approx z_{tip,outer} + z_{tip,inner} \cos \theta_{tip,outer} - l_a \text{sinc} \theta_{tip,inner} \sin \theta_{tip,outer} \quad (2.96)$$

The mirror pedestal displacement in the x -direction is approximated by

$$x_{ped} \approx l_a [\text{sinc} \theta_{tip,outer} - \text{sinc} \theta_{tip,inner} \cos \theta_{tip,outer}] - z_{tip,inner} \sin \theta_{tip,outer} \quad (2.97)$$

FIGURE 2.22 Analysis of mirror pedestal translational displacement using abstracted line drawings of the folded electrothermal actuator for (a) powered outer actuator and (b) powered inner actuator.



At this point all the equations are in hand to describe the rotational and translational motion of the mirror pedestal when a voltage V is applied to either leg of the actuator. The angular displacement in the negative rotational sense is

$$\theta_{m-} = \theta_{tip,outer} - \theta_{tip,inner,un} \quad (2.98)$$

and in the positive rotational sense

$$\theta_{m+} = \theta_{tip,outer,un} - \theta_{tip,inner} \quad (2.99)$$

The angular displacement range is

$$\theta_R = \theta_{m+,max} - \theta_{m-,max} \quad (2.100)$$

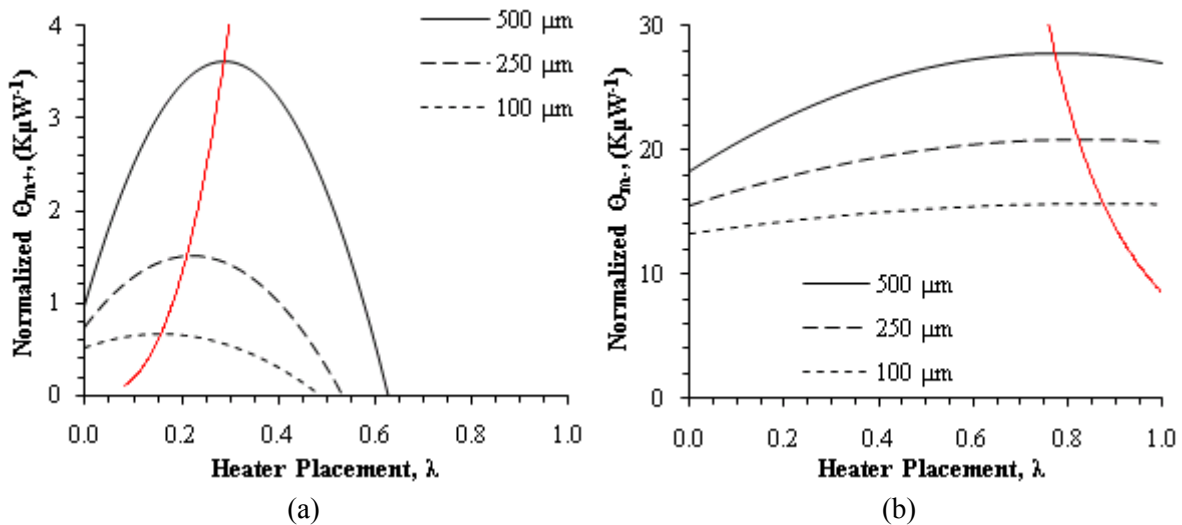
where the “max” subscript denotes the angle achieved at the power that leads to the maximum reliable temperature of operation ΔT_{max} at some point in the actuator beams. A similar set of equations can be formed for the positive and negative z -displacements and the z -displacement range.

2.4.2 Optimal Resistor Position for Reduced Power Consumption

The optimal resistor position for the discrete heater resistor actuator is that position λ which leads to the maximum rotation angle θ_m for a given heater power P_h . For the purposes of exposition, the device shown in Figure 2.16 with a m1a beam and the geometric parameters and thermal resistances listed in Table 2.5 is considered. For the embedded poly film actuator, the beam must be on field to protect the poly from the release etch processes. However, for the discrete heater resistor actuator field is not needed and the thermomechanical advantage of the thinner m1a beam can be exploited.

As laid out in Section 2.3 the temperature distribution and the power necessary to reach a given heater temperature are dependent on the position of the resistor. For each leg of the actuator, heat dissipated by the resistive elements flows to the anchor through $R_{th,anc}$ and to the mirror pedestal through $R_{th,m}$. If the heater is placed at the anchor end of the outer leg of the actuator more dissipated heat flows to the anchor than if it is placed at the joint end. However, if the heater of the outer leg is placed at the joint end, the temperature of the inner actuator is higher and the overall angular displacement is lower. So, two factors are in opposition, the need to reduce power consumption and the need to have a large difference in the average temperatures of the two legs of the actuator.

FIGURE 2.23 Normalized angular displacement Θ_m variation with discrete resistor heater position λ for various actuator lengths l_a of (a) the outer leg of the actuator and (b) the inner leg. In each graph the red line is the locus of maxima of Θ_m with respect to λ .



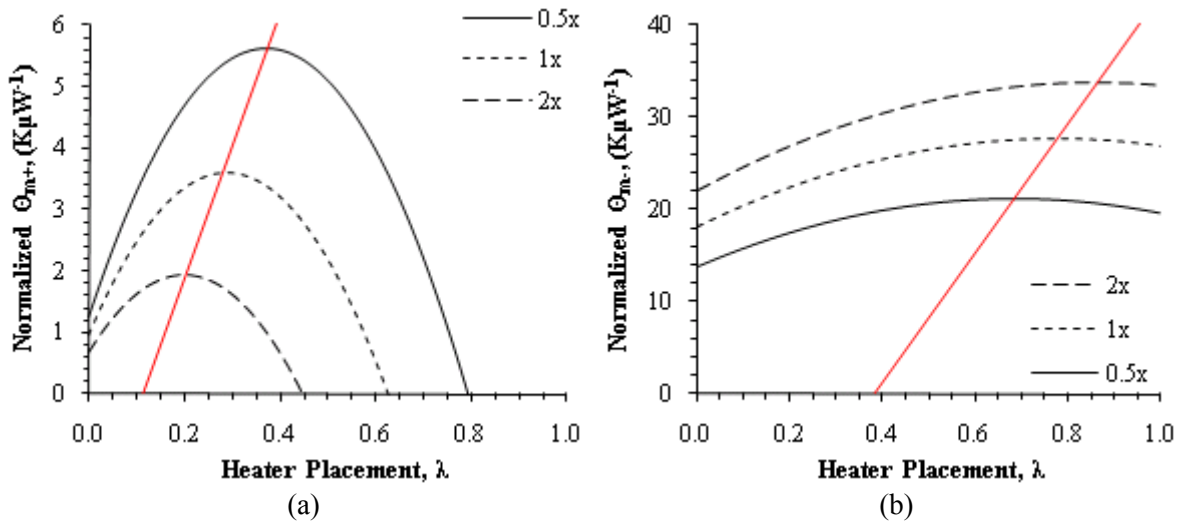
The optimal position of the heater in each leg is established by considering the normalized mirror pedestal angular displacement

$$\Theta_m = \frac{\theta_m}{\gamma(l_a - w_h)P_h} \quad (2.101)$$

as a function of the heater placement for a range of actuator lengths. The graphs in Figure 2.23 show the trends of Θ_m with λ for a range of l_a for the inner and outer actuator and the loci of maxima to guide the designer in the placement of the resistor. For the set of thermal resistances and geometries in Table 2.5, $0.16 < \lambda_{opt,outer} < 0.34$ and $0.73 < \lambda_{opt,inner} < 0.87$ over the range $100 \mu\text{m} < \Omega < 1000 \mu\text{m}$.

As the trends in Figure 2.23 are particular to a given design of thermal resistances, the variation in Θ_m with λ for various multiples of $R_{th,ped}$ and $l_a = 500 \mu\text{m}$ is shown in Figure 2.24 for both actuator legs to demonstrate the sensitivity and design implications of varying elements of the thermal isolation. Figure 2.24 highlights the opportunity the pedestal thermal resistance presents for equalizing the response of the actuator legs. For example, ARDEM (see Chapter 4) could be used to create fins on the backside of the pedestal that would increase surface area and reduce $R_{th,ped}$.

FIGURE 2.24 Normalized angular displacement Θ_m variation with discrete resistor heater position for various multiples of $R_{th,ped}$ and an actuator length $l_a = 500 \mu\text{m}$ for (a) the outer leg of the actuator powered and (b) the inner leg of the actuator powered.



2.4.3 Scan Range Scaling

The scaling of the scan range θ_R is analyzed for the m1a- and m1pf-based actuators over a range of device pitches Ω . The heater positions $\lambda_{\text{outer}} = 0.25$ and $\lambda_{\text{inner}} = 0.80$ for the m1a-based actuator are set to values in the middle of their range for the range of Ω considered. Figure 2.25 (a) shows the scaling comparison between the m1a- and the m1pf-based actuators. The better performance of the m1a-based actuator is a result of the higher thermal sensitivity ($\gamma_{\text{m1a}} = 20.6 \text{ m}^{-1}\text{K}^{-1}$ cf. $\gamma_{\text{m1pf}} = 18.4 \text{ m}^{-1}\text{K}^{-1}$) and the ability to control the position of the maximum temperature ΔT_{max} along the actuator beams. The graph in Figure 2.25 (b) shows the scaling of θ_R with Ω for various multiples of $R_{\text{th,ped}}$. The increase in θ_R with decreasing $R_{\text{th,ped}}$ is counterintuitive on its face because lower thermal resistance is associated with lower temperature changes and tip displacements, however, in the case of the folded actuator, a lower $R_{\text{th,ped}}$ means that proportionately less heat flows through the unpowered actuator, which consequently has a lower $\Delta \bar{T}$, a lower θ_{tip} and hence a smaller negative impact on θ_m . For comparison, the scan range scaling for Tsai and Wu's gimbal-less electrostatic mirror [21] is included. On the basis of this comparison, electrothermal actuation should be applied when $\Omega > 180 \mu\text{m}$ for discrete heater devices and $\Omega > 200 \mu\text{m}$ for distributed heater devices.

FIGURE 2.25 (a) Scaling of m1a- and m1pf-based folded electrothermal actuator scan range θ_R with device pitch Ω . The scan range scaling of Tsai and Wu's gimbal-less electrostatic mirror is shown for comparison. (b) Scaling of m1a-based actuator scan range θ_R with device pitch Ω for various multiples of $R_{\text{th,ped}}$.

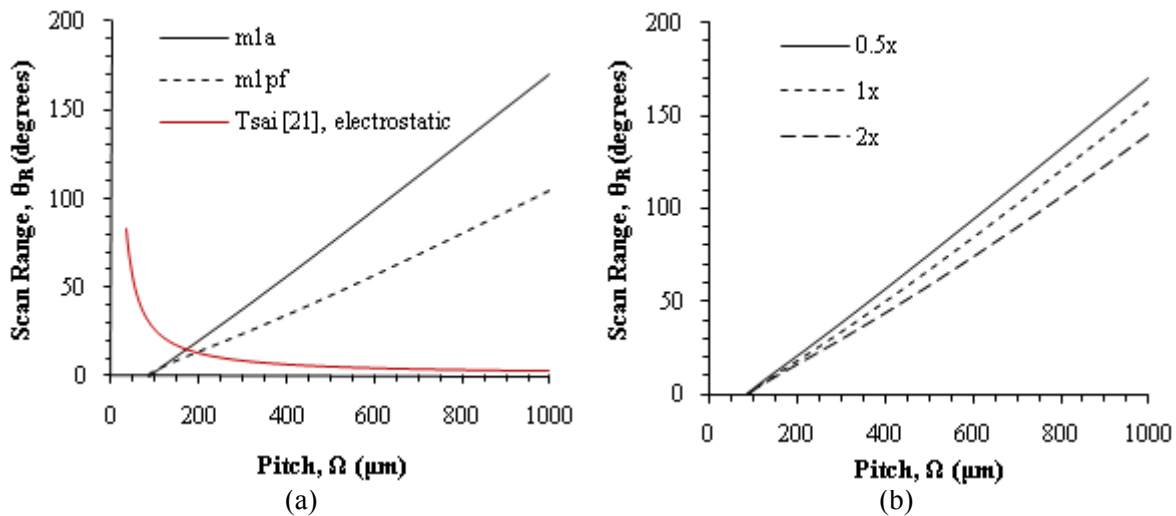
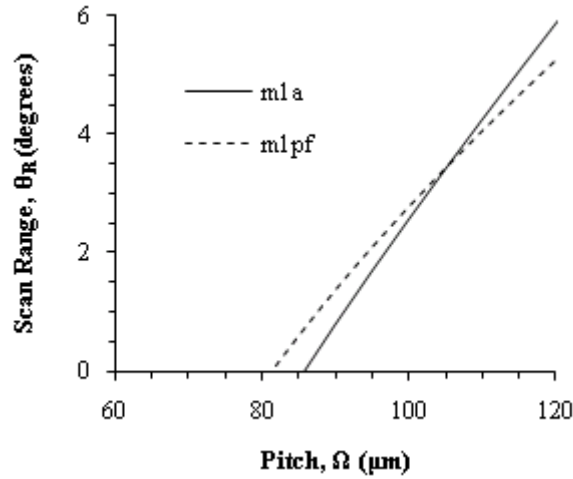


FIGURE 2.26 (a) Scaling of *m1a*- and *m1pf*-based folded electrothermal actuator scan range θ_R at small device pitch Ω showing the point at which the *m1pf*-based actuator has a larger response than the *m1a*-based actuators.



The scaling of θ_R is unfavorable, but for very dense arrays with small pitch a change in actuator type from discrete heater to embedded film heater can improve the situation, as shown in Figure 2.26. However, rotational performance at small pitches falls far below a device like the TI DLP that produces $\theta_R = 20^\circ$. The discrete heater has a finite width w_h which takes up actuator length that could otherwise be used to generate angular or translational displacements. In Figure 2.26, the point at which the *m1pf*-based actuator produces a larger scan range than the *m1a*-based actuator is $\Omega \approx 105 \mu\text{m}$. This cross-over point, like the other aspects of folded electrothermal actuator design is dependent on the thermal resistances of the device and must be evaluated for each new case.

2.4.4 Speed Scaling

The speed of a MEMS device is typically characterized by its time constant, resonant frequency, or -3 dB point. Scanning applications typically require video rate speed, or 30 Hz (0.033 s), so the speed in both the thermal and mechanical domains must exceed this. In the thermal domain the -3 dB point is inappropriate as the processes are purely dissipative, however a thermal cut-off frequency $f_{c,\text{th}}$ can be defined as the frequency at which the device response drops by 3 dB from its DC value. This is measured experimentally but correlates to the thermal time constant,

$$\tau_{\text{th}} = R_{\text{th}} C_{\text{th}} = \frac{1}{2\pi f_{\text{c,th}}}, \quad (2.102)$$

where R_{th} is the total thermal resistance to thermal ground and C_{th} is the total thermal capacitance between the heat source and thermal ground and includes the device and the air around it. The thermal capacitance contribution of the beams is

$$C_{\text{th}} = N_{\text{p,b}} l_{\text{b}} \sum_{\text{members}} \rho_{\text{d},i} C_{\text{p},i} w_i t_i = N_{\text{p,b}} (\rho_{\text{d}} C_{\text{p}})_{\text{eff,b}} l_{\text{b}} w_{\text{b}} t_{\text{b}} \quad (2.103)$$

and the thermal capacitance of the other structural elements are similarly defined while the air under the structure has the simple thermal capacitance expression.

The lumped electrothermal model of a beam is sufficient for determining R_{th} for the discrete resistor heater actuators, but the distributed heating of the m1pf beam requires solution of the 1-D, time-dependent heat equation

$$(\rho_{\text{d}} C_{\text{p}})_{\text{eff,b}} \frac{d\Delta T_{\text{a,e}}}{dt} = \kappa_{\text{eff,b}} \frac{d^2 \Delta T_{\text{a,e}}}{dx^2} + Q_{\text{G}} \quad (2.104)$$

to derive an approximate analytic expression for R_{th} .

For the simple case of a m1pf beam held at the same constant temperature at both ends, (2.104) has the solution

$$\Delta T_{\text{a,e}}(x, \tau) = \frac{Q_{\text{G}} l_{\text{b}}^2}{2\kappa_{\text{eff,b}}} \left[\frac{x}{l_{\text{b}}} \left(1 - \frac{x}{l_{\text{b}}}\right) - \frac{8}{\pi^3} \sum_{m=\text{odd}}^{\infty} \frac{1}{m^3} \exp\left(-\frac{m^2 \pi^2 \kappa_{\text{eff,b}}}{(\rho_{\text{d}} C_{\text{p}})_{\text{eff,b}} l_{\text{b}}^2} \tau\right) \sin\left(m\pi \frac{x}{l_{\text{b}}}\right) \right]. \quad (2.105)$$

The first eigenmode (i.e. for $m = 1$) dominates the transient term in the solution and serves to define the time constant $\tau_{\text{th,a,e}}$ for the m1pf beam as

$$\tau_{\text{th,a,e}} = \frac{(\rho_d C_p)_{\text{eff,b}} l_b^2}{\pi^2 \kappa_{\text{eff,b}}} = R_{\text{th,a,e,trans}} C_{\text{th,a,e,trans}}. \quad (2.106)$$

The heat capacity of the dominant mode is

$$C_{\text{th,a,e,trans}} = \frac{2N_{\text{p,b}}(\rho_d C_p)_{\text{eff,b}} l_b w_b t_b}{\pi} [57]. \quad (2.107)$$

By equating (2.106) and (2.102) and substituting in the expression for C_{th} from (2.107) an approximation of the thermal resistance of the powered m1pf beam from a transient perspective is given as

$$R_{\text{th,a,e,trans}} = \frac{l_b}{2\pi N_{\text{p,b}} k_{\text{eff,b}} w_b t_b}. \quad (2.108)$$

The optimal value of thermal resistance of a m1a-based actuator from a speed perspective is achieved when $\lambda = 0.5$ which leads to

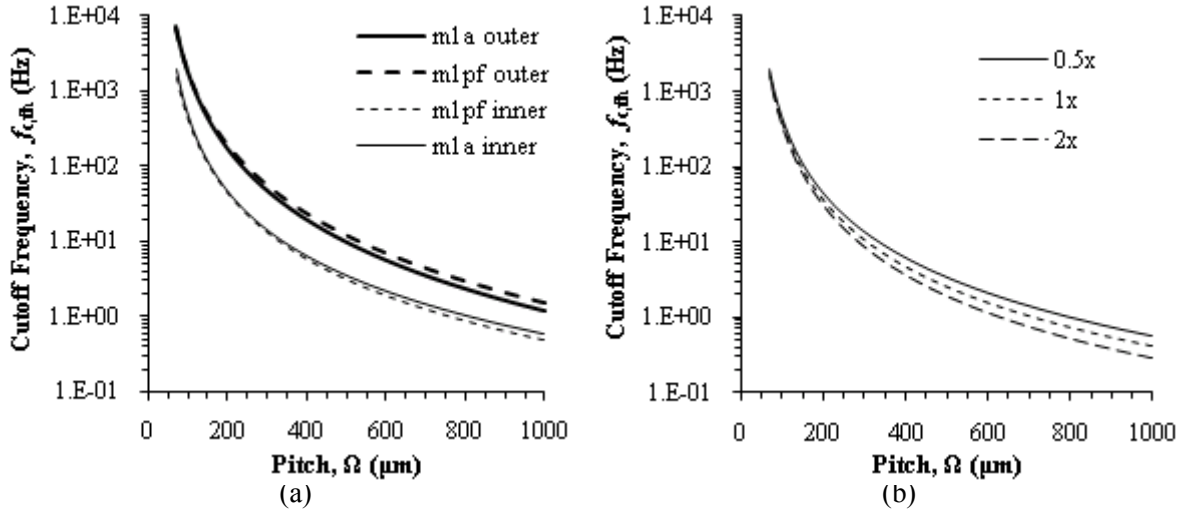
$$R_{\text{th,a,d,trans}} = \frac{l_b}{4N_{\text{p,b}} k_{\text{eff,b}} w_b t_b} = \frac{R_{\text{th,a,d}}}{4}. \quad (2.109)$$

On the basis of this analysis, if all other things were equal, $\tau_{\text{th,a,e}} \approx 0.4\tau_{\text{th,a,d}}$ and the m1pf is inherently faster than the m1a beam by more than a factor of two.

A comparison of the m1a- and m1pf-based topologies from Figure 2.16 is shown in Figure 2.27 using the thermal resistances and geometries from Table 2.5. Optimal resistor positions are used for the m1a-based actuator so the speed scaling analysis is compatible with the power scaling analysis of Section 2.4.5. In the speed analysis, the thermal circuit in Figure 2.17 (a) represents the m1pf-based actuator and the thermal resistance from the thermal transient perspective is split equally between the two halves of the circuit (i.e. the total thermal resistance between the power source and the anchor is $R_{\text{th,anc}} + 2R_{\text{th,a,e,trans}}$). Speed scaling is favorable with decreasing pitch for folded electrothermal actu-

ators. Changing the thermal resistances of the device can be used to impact the device speed as shown in Figure 2.27 (b).

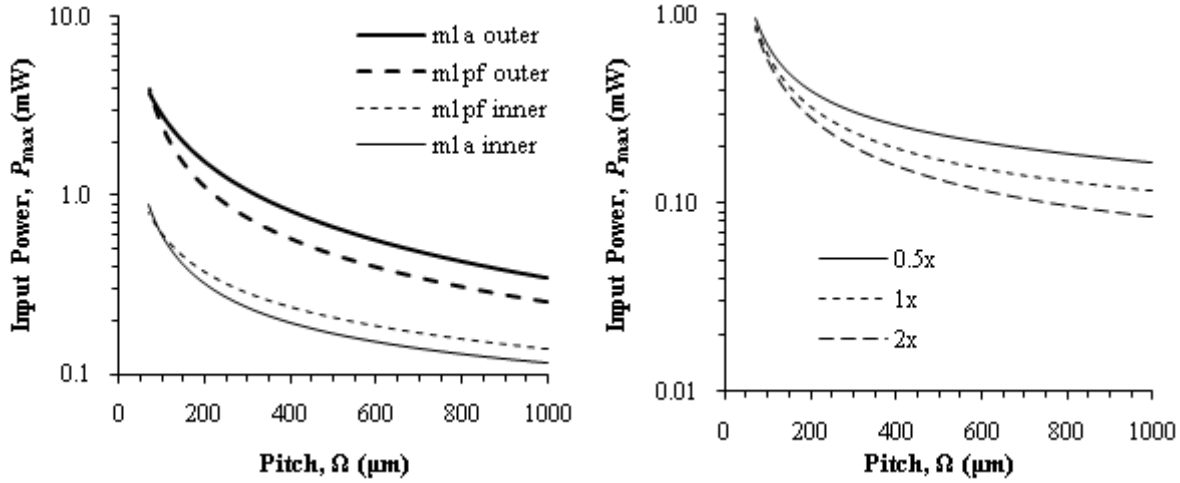
FIGURE 2.27 (a) Scaling of the thermal cutoff frequency $f_{c,th}$ with device pitch Ω for the actuator topologies shown in Figure 2.16. (b) Scaling of thermal cutoff frequency $f_{c,th}$ of the inner leg of the mla-based actuator with device pitch Ω for various multiples of $R_{th,ped}$



2.4.5 Power Scaling

It is proposed that the appropriate measure of the rationale for scaling folded electrothermal actuators to smaller dimensions is the angular displacement per unit power at that value of power that results in the maximum temperature being achieved in the device that can be sustained while ensuring reliable operation. Similarly, if motion in the z -direction is the desired output, the figure of merit would be the z -displacement per unit power. Reliable operation is defined as producing output within specification to a certain tolerance for a specific number of cycles. For CMOS-MEMS electrothermal actuators, the maximum temperature for reliable operation ΔT_{max} has not been fully characterized and this is a critical unknown. However, it has been observed that device failure in the form of diminished response occurs within hours when the device is raised above 200 °C and, in the form of metal delamination, within minutes when the device is raised above 300 °C.

FIGURE 2.28 (a) Scaling of P_{\max} , the power to achieve maximum reliable operating temperature, with device pitch for the inner and outer legs of mla- and mlpf- based actuators. (b) Scaling of P_{\max} for the inner leg of the mla-based actuator with device pitch Ω for various multiples of $R_{\text{th,ded}}$



Similar to the above analyses, the actuator topology is taken from Figure 2.16 and the geometric parameters and thermal isolation values from Table 2.5. For the mla-based actuator, the resistor heater position is the same as Section 2.4.3. The power P_{\max} dissipated to reach ΔT_{\max} and achieve $\theta_{m,\max}$ for the inner and outer legs of a mla- and mlpf-based actuator is shown in Figure 2.28. P_{\max} scales unfavorably with Ω because the actuator beam plays a significant role in its own thermal isolation and as l_a decreases, Fick's law dictates more power is needed to achieve larger temperature gradients.

The unfavorable scaling of folded electrothermal actuators, the angular scaling and the power scaling are demonstrated in the figure of merit and the heat dissipation density,

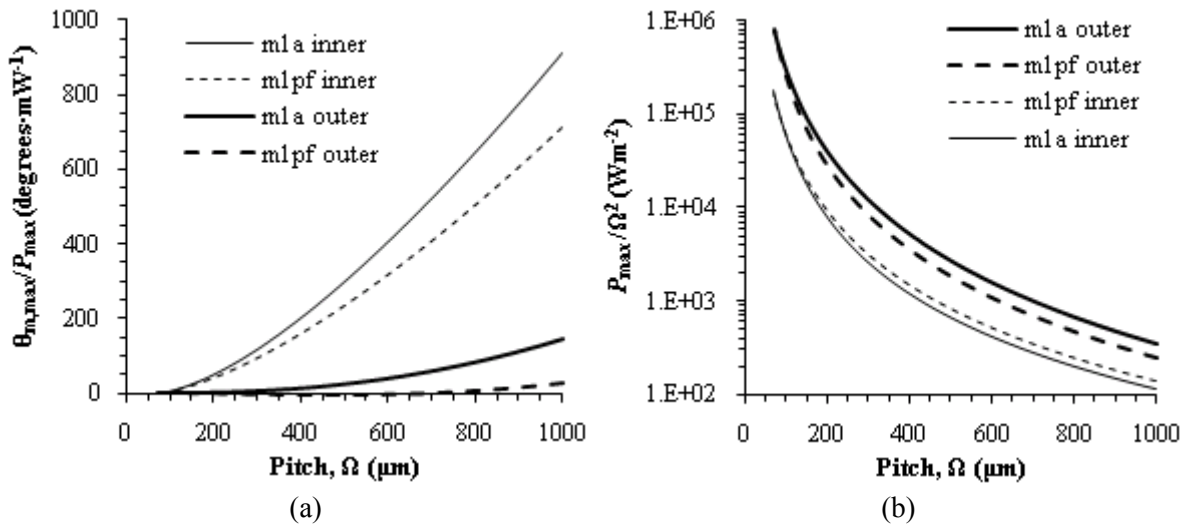
$$FOM = \frac{\theta_{m,\max}}{P_{\max}}, \quad (2.110)$$

$$\tilde{P} = \frac{P_{\max}}{\Omega^2} \quad (2.111)$$

respectively, as shown in Figure 2.29 (a) and (b). The trend in \tilde{P} is particularly problematic because to achieve devices on the micron scale, w_{anc} must decrease along with the quantity of material making up the anchor, which further isolates the device and makes the dissipation of the heat more difficult.

The same sequence of analysis can be done for the various topologies of 1-D folded electrothermal actuators and 3-D electrothermal actuators and leads to the same conclusion, that in a MEMS fabrication technology that provides the designer no control over the layer thicknesses or the device materials, the scaling of the actuator is too unfavorable to allow devices to be designed at the 10's of microns scale. The angular displacement advantage of electrothermal actuators is lost as the device shrinks and the power necessary to reach reasonable angular displacements, and the currents required to generate the power, become prohibitive, especially considering the number of devices in a given area typically increases as the device size decreases (i.e. array dimensions only increase). Additionally, the mechanical anchor's efficacy as a thermal ground is compromised as device density and \tilde{P} increase.

FIGURE 2.29 (a) Scaling of $\theta_{m,max}/P_{max}$ with pitch Ω for the inner and outer legs of m1a- and m1pf- based actuators. (b) Scaling of the heat power dissipation density P_{max}/Ω^2 with Ω



However, a path to practical micron-scale electrothermally actuated mirrors is discernible, but requires: 1. the actuator layer thicknesses are optimized for thermal sensitivity and scaled along with device pitch, 2. the anchors are made of highly thermally conductive materials, 3. the thermal isolation is formed only of thermally insulating materials, 4. electrical connectivity is formed by materials with high electrical conductivity and low thermal conductivity, 5. the devices are latched so no power is dissipated when an angular position is being held, 6. the conduction of heat from the surface of the payload is maximized.

2.5 Actuator Mechanical Design

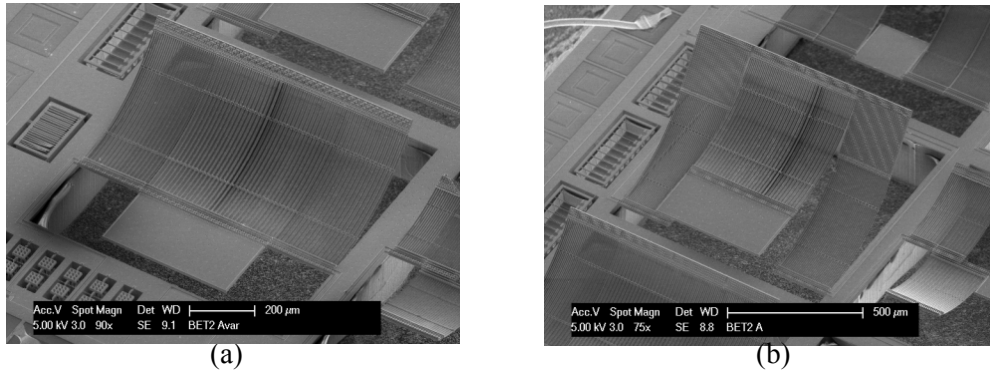
2.5.1 Self-Assembly

The displacements that occur in MEMS devices when they are released are referred to as self-assembly and are caused by residual stress in the films comprising the structures. Vertical residual stress gradients in the actuator beams generate bending moments similar to those generated by mismatched thermal expansion that lead to the shape change described by (2.1) and (2.17). If the residual stress in each member is assumed constant, this effect is described by applying the residual stress in the i^{th} member $\sigma_{i,\text{res}}$ in (2.15) which gives a radius of curvature of

$$\frac{1}{\rho_{c,\text{res}}} = \frac{M_{y,\text{res}}}{(EI)_{\text{eff},y}} = \frac{\sum_{\text{members}} \sigma_{i,\text{res}} \Delta y_i \Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{2} \right)}{\sum_{\text{members}} E_i^* \Delta y_i \Delta z_i \left[\Delta z_i \left(z_{b,i} - z_{na} + \frac{\Delta z_i}{3} \right) + (z_{b,i} - z_{na})^2 \right]}. \quad (2.112)$$

For the bimorph case, a simple expression similar in form to (2.1) is available [30].

FIGURE 2.30 (a) *Folded electrothermal actuator with no z-self-assembly displacement.* (b) *Folded electrothermal actuator with large z-self-assembly displacement.*



Residual stress is an artifact of the processing [57] and is constant over the length scales of a single MEMS device so $\rho_{c,\text{res}}$ is constant. Examples of the impact of residual stress on folded electrothermal actuators are shown in Figure 2.30. The tip angle of an actuator leg, for both types of actuator, resulting from residual stress is

$$\theta_{\text{tip,res}} = \frac{l_b}{\rho_{c,\text{res}}} . \quad (2.113)$$

The z -displacements of the tip for embedded film heater and discrete heater resistor actuator types are

$$z_{\text{tip,e,res}} = \frac{l_b^2}{2\rho_{c,\text{res}}} \quad (2.114)$$

and

$$z_{\text{tip,d,res}} = \frac{l_b^2}{2\rho_{c,\text{res}}} + w_h \sin \frac{\lambda l_b}{\rho_{c,\text{res}}} , \quad (2.115)$$

respectively. The x -displacement for both types of actuator is

$$x_{\text{tip,d,res}} = -l_b \left(1 - \text{sinc} \frac{l_b}{\rho_{c,\text{res}}} \right) . \quad (2.116)$$

In the event of ambient temperature variation, for which the temperature change in the beam is constant, the resultant radius of curvature of the beam is constant and is given by

$$\frac{1}{\rho_c} = \frac{1}{\rho_{c,\text{res}}} + \frac{1}{\rho_{c,\text{amb}}} . \quad (2.117)$$

The tip angle and z - and x -displacements are found by substituting ρ_c into (2.113) to (2.116). The displacements of the pedestal of 1-D folded electrothermal actuators or 3-D electrothermal actuators are found by appropriate combinations of the equations in (2.113) to (2.116) in a manner similar to that shown in Section 2.4.1 and are not reiterated here as their generality is limited. However, this should highlight again the need for an analytic framework for kinematic problems general enough to encompass elements of varying curvature.

It is essential to understand and design for self-assembly as it defines the rest position of the devices. In arrays, it is even more important to ensure self-assembly doesn't result in contact between array members or with other structures. For example, the 1-D actuator topologies shown in Figure 2.31 were analyzed for z - and x -self-assembly assuming $\rho_{c,res} = 550 \mu\text{m}$, $l_b = 480 \mu\text{m}$, $w_{ped} = 200 \mu\text{m}$ and the length of the extender l_e as shown. The self-assembly displacements given in Table 2.6 demonstrate the wide range of translations possible and the need to ensure the topology self-assembly matches the application. The reader should note that in the case of actuator Type B and Type C, the benefit of rejection of common-mode temperature variation is lost and significant x - and z -displacements can occur in the unpowered device.

FIGURE 2.31 Plan-views of actuator topologies analyzed for self-assembly displacement.

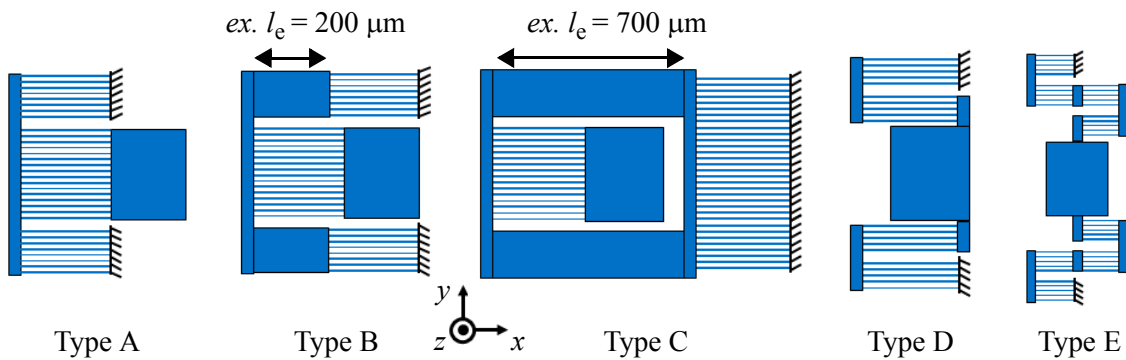


TABLE 2.6 Examples of self-assembly displacements for various topologies of 1-D folded electrothermal actuator.

Actuator Type	x -Self-Assembly (μm)	z -Self-Assembly (μm)
A	0	0
B	-71	153
C	-257	552
D	0	0
E	0	0

The zero x -self-assembly of types A, D and E make them suitable for arrayed scanning applications. During the release etch process, there is variation in the release time amongst array elements and if the x -self-assembly is significant, adjacent array elements can displace to a position that blocks the etch process and exacerbates intra-array variance. It is also possible that physical contact may occur

between adjacent elements. Such adverse effects can be avoided by increasing the gap between adjacent elements, however this may be undesirable for optical applications in which high FF is desired, so unless there is an overwhelming application need for an actuator type with significant self-assembly, the zero self-assembly types should be chosen.

2.5.2 Geometric Constraints

The mirror pitch and the fabrication limitations are the basis for the geometric constraints on the device. The fabrication-based constraints are common to all devices. The pitch-based constraints are dependent on the topology of the device and its number of DOF. As an example, the pitch-based constraints of the 1-D actuator topology from Figure 2.16 (Type D of Figure 2.31) are examined. In the aforementioned scaling arguments the variation in l_a with Ω is implicit but it is assumed that $N_{p,b}$, $l_{s,a}$ and $l_{s,anc}$ and $l_{s,ped}$ are constant as Ω changes. The variation in l_a and other parameters with Ω is made explicit, which has implications for the mechanical modes of the device as discussed in Section 2.5.4.

The maximum actuator length for the Type D topology from Figure 2.16 is

$$l_{a,max} = \Omega - w_{anc} - g_{ped} - g_s - 3l_{iso} - \frac{w_{ped}}{2} - \frac{3w_s}{2}. \quad (2.118)$$

The maximum number of actuator beams in parallel for a single leg of an actuator is

$$N_{p,b} = \frac{\Omega - w_{anc} - 2g_b - w_{ped}}{4(w_b + g_b)}. \quad (2.119)$$

The actuator strut length is

$$l_{s,a} = 2N_{p,b}(w_b + g_b) - g_b. \quad (2.120)$$

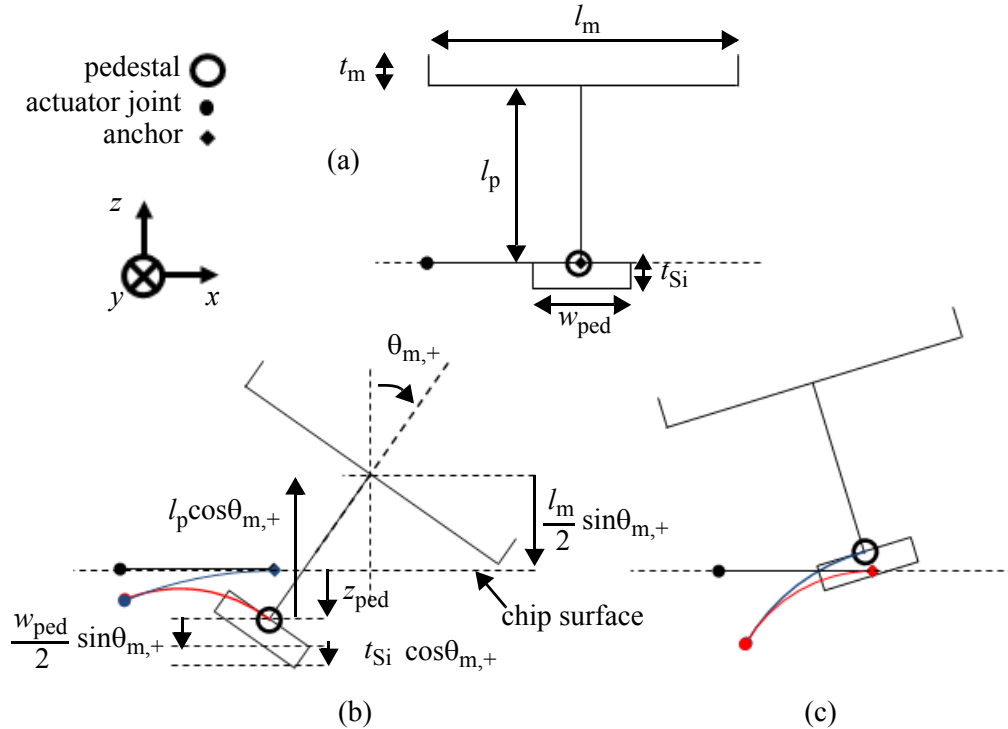
The anchor and pedestal strut lengths are

$$l_{s,anc} = l_{s,ped} = N_{p,b}(w_b + g_b). \quad (2.121)$$

2.5.3 Mirror and Post Dimensional Constraints

The mirror thickness t_m post height l_p and post width w_p are designed to place the plate and post bending modes far beyond the modes of the actuator. Through FEA it is found that mirrors up to 1 mm on a side have a first plate bending mode frequency > 5 kHz down to $t_m = 5 \mu\text{m}$. The posts have their first torsional mode frequency > 2 kHz down to $w_p = 10 \mu\text{m}$ for $l_p = 500 \mu\text{m}$. Additionally, the post is designed to ensure that at the extent of the angular rotation range the edge of the mirror does not contact the chip surface. The z -displacement of the pedestal and the thickness of Si under it leads to a constraint on the angular deflection unless additional clearance beyond the thickness of the substrate is provided.

FIGURE 2.32 Abstracted line drawing of a Type D, 1-D folded electrothermal actuator from Figure 2.16 (a) with mirror and post for analysis of post height l_p constraint based on mirror width l_m and expected rotation angles. (a) At rest. (b) Displacement with inner actuator powered. (c) Displacement with outer actuator powered.



The constraint on the post length $l_{p,min}$ for the actuator shown in Figure 2.16 (a) is demonstrated through Figure 2.32. When the inner leg of the actuator is powered the pedestal rotates in the positive sense and the pedestal moves in the negative z -direction. The edge of the mirror sweeps through an

elliptic arc until it reaches the surface of the chip. If the device is designed for this to be the maximum rotation angle $\theta_{m,+,\max}$ then for a given mirror length, the post must meet the condition

$$l_p > \frac{l_m}{2} \tan \theta_{m,+,\max} - \frac{z_{\text{ped}}}{\cos \theta_{m,+,\max}} . \quad (2.122)$$

If the thickness of the wafer does not meet the condition

$$t_w > \frac{w_{\text{ped}}}{2} \sin \theta_{m,+,\max} + t_{\text{Si}} \cos \theta_{m,+,\max} + z_{\text{ped}} \quad (2.123)$$

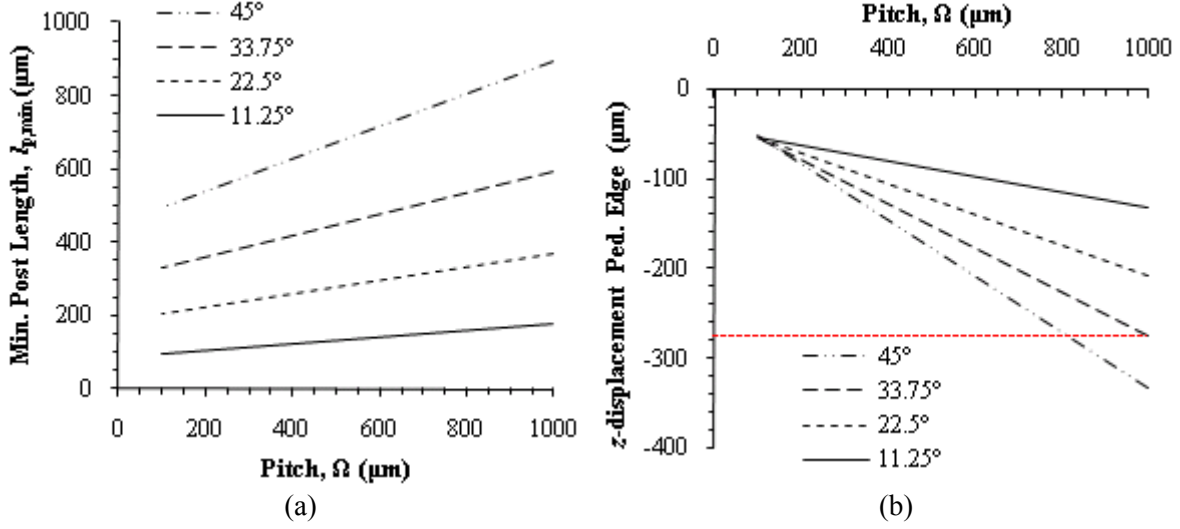
then a carrier chip must be used (see Section 3.3.4) with a pocket depth

$$t_{\text{pocket}} > \frac{w_{\text{ped}}}{2} \sin \theta_{m,+,\max} + t_{\text{Si}} \cos \theta_{m,+,\max} + z_{\text{ped}} - t_w \quad (2.124)$$

in order for angular FSD to be achievable.

For example, in the case of an actuator shown in Figure 2.16 (a), with an angular specification of $\pm 45^\circ$, the tip of the inner actuator must move through an angle greater than 45° to counteract the parasitic rotation of the outer actuator. Both angular displacements contribute to the z -displacement of the edge of the mirror. Figure 2.33 (a) illustrates the variation in the minimum post height $l_{p,\min}$ necessary to ensure the edge of the mirror does not contact the surface of the chip. As $\theta_{m,+,\max}$ decreases, $l_{p,\min}$ decreases. As the pitch Ω decreases, $l_{p,\min}$ decreases; however the reader should note that in this case the temperature changes and the power dissipations necessary to achieve the angles listed in the legend of Figure 2.33 (a) are not considered. Only geometric considerations have been explored in this graph. Similarly, Figure 2.33 (b) shows the variation in z -displacement of the outer edge of the pedestal with pitch Ω and provides a comparison of the z -displacement with the thickness of the JAZZ chip for which $t_w = 275 \mu\text{m}$.

FIGURE 2.33 (a) Variation in mirror post constraint $l_{p,\min}$ with pitch Ω for various angular displacements when the inner actuator is powered for the actuator in Figure 2.16 (a) with geometries given in Table 2.5. (b) Variation in z-displacement of the outer edge of the pedestal with pitch Ω for the same actuator topology and geometry.



The constraints in (2.122) to (2.124) are based on the actuator topology shown in Figure 2.16 (a), so for comparison the analogous constraints for the actuator in Figure 2.30 (a) are illustrated in Figure 2.34 and are given by

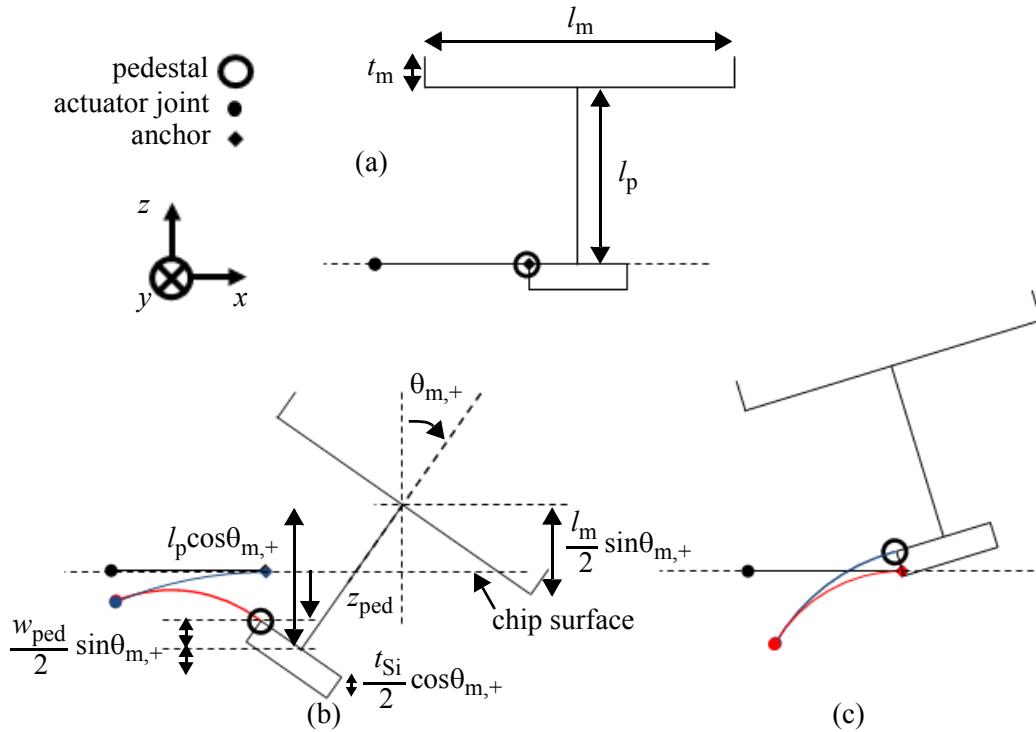
$$l_p > \frac{l_m}{2} \tan \theta_{m,+,\max} + \frac{w_{\text{ped}}}{2} \tan \theta_{m,+,\max} - \frac{z_{\text{ped}}}{\cos \theta_{m,+,\max}}, \quad (2.125)$$

$$t_w > w_{\text{ped}} \sin \theta_{m,+,\max} + t_{Si} \cos \theta_{m,+,\max} - z_{\text{ped}} \quad (2.126)$$

$$\text{and} \quad (2.127)$$

$$t_{\text{pocket}} > w_{\text{ped}} \sin \theta_{m,+,\max} + t_{Si} \cos \theta_{m,+,\max} - z_{\text{ped}} - t_w. \quad (2.128)$$

FIGURE 2.34 Abstracted line drawing of a Type A, 1-D folded electrothermal actuator from Figure 2.30 (a) with mirror and post for analysis of post height l_p constraint based on mirror width l_m and thickness t_m and expected rotation angles. (a) At rest. (b) Displacement with inner actuator powered. (c) Displacement with outer actuator powered.



2.5.4 Mechanical Modes

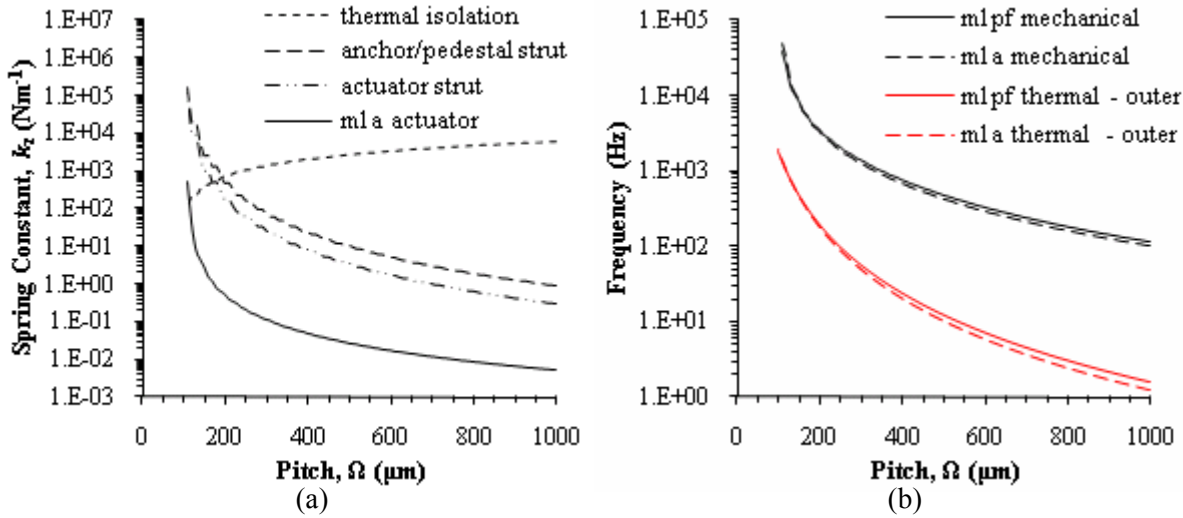
The actuator beams, struts and via isolation units are modeled as lumped elements for the purpose of analysis. The spring constant of an element for bending in the z -direction about the y -axis is

$$k_z = \frac{3(EI)_{\text{eff},y}}{l_b^3}. \quad (2.129)$$

Equation (2.14) or FEA is used to determine the effective flexural rigidity $(EI)_{\text{eff},y}$. Values of $(EI)_{\text{eff},y}$ are listed in Table 2.7 for m1a and m1pf beams and the strut and thermal isolation shown in Figure 2.6 and geometries in Table 2.5. The trends in the spring constants of the elements are shown in Figure 2.35 and demonstrate the actuator beams are the most flexible elements of the structure.

TABLE 2.7 Examples of effective flexural rigidity of 1-DOF actuator elements from Figure 2.16 topology.

Element	$(ED)_{\text{eff},y}$ (Nm ²)
m1a beam	4.6×10^{-14}
m1pf beam	5.7×10^{-14}
thermal isolation unit	5.8×10^{-14}
strut	7.0×10^{-12}

FIGURE 2.35 (a) Spring constant variation with pitch for the elements of a Type D folded electrothermal actuator. (b) Approximation of the first mode frequency variation with pitch for a Type D actuator with l_p scaled to maintain a 45° scan angle when the inner leg of the actuator is powered.

At large pitches, the actuator is the dominant flexible element in determining the mode frequency. It is only when the pitch is small ($< 200 \mu\text{m}$ in the case shown in Figure 2.35) that elements like the thermal isolation begin to play a role in the mode frequency. In any case, the important condition is that the 1st mechanical mode frequency exceeds the thermal cutoff frequency $f_{c,\text{th}}$, which is demonstrated by Figure 2.35 (b) for a Type D actuator with l_p scaled to maintain $\theta_{m,+,\text{max}} = 45^\circ$ when the inner actuator is powered, assuming $t_m = 10 \mu\text{m}$ and $w_p = 20 \mu\text{m}$.

The actuator types in Figure 2.31 have different mode frequencies and shapes. FEA eigenmodes for the various actuators are shown in Figure 2.36. The mode frequencies given in Table 2.8 represent actuators with $l_b = 550 \mu\text{m}$, $t_m = 25 \mu\text{m}$, $w_{\text{ped}} = 200 \mu\text{m}$ and $w_p = 100 \mu\text{m}$ which explains the difference with the mode frequencies shown in Figure 2.35 (b). The reader should note that linearity is

assumed for this analysis and the large FSDs of the mirrors could drive the system into non-linearity and these values would no longer be valid.

FIGURE 2.36 The first three eigenmodes of the various folded electrothermal actuator topologies.

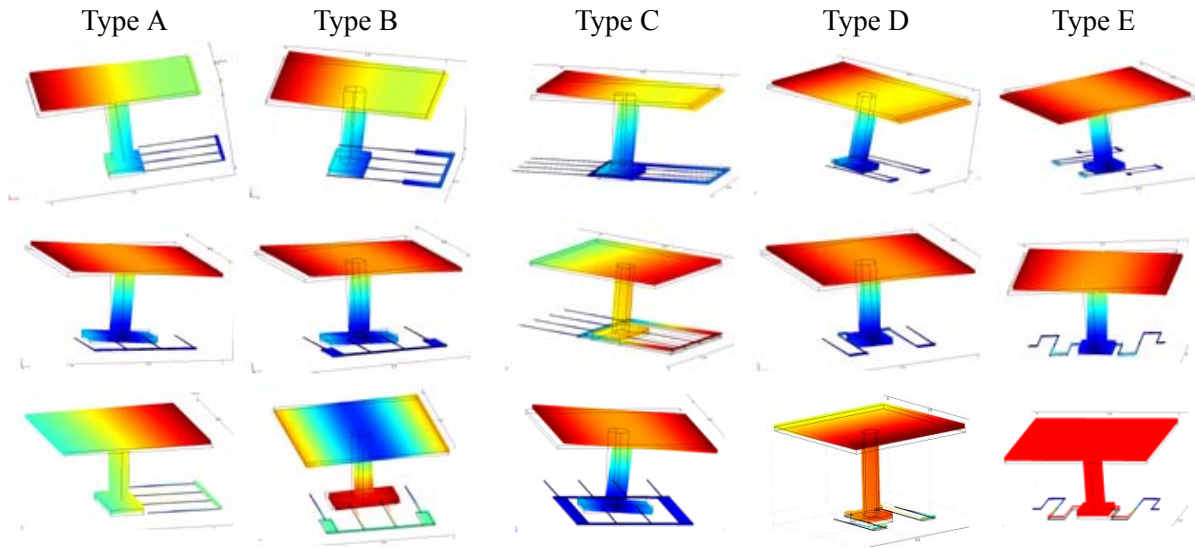


TABLE 2.8 Mode frequencies for folded electrothermal actuator topologies.

Actuator Type	1 st Mode, f_1 (Hz)	2 nd Mode, f_2 (Hz)	3 rd Mode, f_3 (Hz)
A	99	220	542
B	100	224	551
C	134	193	226
D	100	205	3697
E	85	180	280

2.6 Electrothermal Design and Operation Summary

The objective of the chapter is to lay out the factors: material, geometric, physical and fabrication that affect the design and scaling of micromirror arrays with folded electrothermal actuators.

At the root is the structure of the actuator beam and the heater mechanism that dissipates the heat that changes the temperature of the beam and causes motion of the structure. Timoshenko's theory of the bimorph is shown to be insufficient to accurately model the electrothermomechanical behavior of complex CMOS-MEMS beams and it is shown how the application of a systematic multimorph beam

theory can improve the accuracy of analytic predictions. The material dependencies are highlighted through the analysis of the thermal sensitivity γ of several beam cross-sections.

One level up in the design hierarchy is the topological form of the device. 1-D and 3-D actuator topologies are presented, but for brevity only 1-D actuators are fully analyzed for scaling dependencies. However, the analysis is structured so that 3-D actuators of an arbitrary number of legs can be similarly explored. Thermal isolation is shown to be a critical factor in the performance of the device due to its role in isolating the temperature gradients in certain parts of the actuator.

Finally, the mechanical behavior of the device is examined to ensure the modes and mode frequencies are compatible with, and do not limit, the electrothermal response. The issue of self-assembly is discussed along with its potential adverse impact on release etch processing.

Over the range of CMOS-MEMS device pitch from $1 \text{ mm} > \Omega > 50 \text{ }\mu\text{m}$ it is shown that the angular range θ_R decreases and the power dissipation P_{max} needed to achieve the maximum temperature change $\Delta T_{\text{max}} = 180 \text{ }^\circ\text{C}$ in the device increases. This is summarized in the *FOM*, θ_R/P_{max} . The adverse *FOM* scaling law results from the linear dependence of θ_m on l_a and the difficulty in achieving large temperature gradients over decreasing distances with constant material parameters. Expectedly, as power scaling is adverse, speed scaling is advantageous, but this is cold comfort for the most detrimental scaling behavior, that of the heat dissipation density \tilde{P} . Array dimensions typically remain constant or increase as device pitch decreases. This improves resolution and increases the functionality per unit area and hence reduces the overall cost per functional operation. In the case of folded electrothermal actuators \tilde{P} increases by almost four orders of magnitude over the pitch range considered. The conclusion of the analysis is that high density arrays of electrothermal devices with $\Omega < 100 \text{ }\mu\text{m}$ requires custom processing using optimal materials and a latching mechanism at the device level to eliminate power consumption when an angular position is held. However, through comparison of scan range θ_R with electrostatic devices, it is shown that electrothermal devices are desirable when the array pitch Ω scales above approximately $200 \text{ }\mu\text{m}$.

3

SOI-CMOS-MEMS Fabrication

“I never failed once. It just happened to be a 2000-step process.”

- Thomas Edison

SOI-CMOS-MEMS was developed to realize the independent optimization of an electrothermal actuator and a micromirror. The ultimate goal, to produce a micromirror device with a high fill factor and a high scan range, qualities not previously achieved together. In this chapter the fabrication technology is described in detail, highlighting where appropriate the design issues arising from process and materials choices. The chapter is broken into sections devoted to the CMOS-MEMS steps and the SOI process steps prior to bonding. The bonding and release steps are covered in a separate section.

For the purposes of this dissertation a small number of devices was necessary and processing was done at the chip level, but the development of the fabrication technology was done with wafer-level scaling in mind, with the exception of bonding and release.

The complexity of the SOI-CMOS-MEMS technology may appear excessive and the question should arise, “Is this process manufacturable?”. To that, it is stated that the question is not whether it is manufacturable, but rather, “Should it be manufacturable?”. This means that with the right vehicle and the right profit margin, the necessary minds and development partners can be found to make any process manufacturable. Intel’s 90 nm technology gate oxidation process produces a film 1.2 nm thick film across a 300 mm wafer with atomic scale uniformity [58], an astonishing feat and one that would have been considered unmanufacturable 30 years ago when gate oxides were 100 nm thick on 100 mm

wafers. This case in point emphatically demonstrates that when customers want the product, a way is found to meet the demand. To answer the “Should...?” the device must be fabricated and characterized and its inherent strengths and weaknesses identified. This chapter deals with the first part of that story.

The SOI-CMOS-MEMS fabrication process steps in which significant changes of research interest are made to the CMOS and SOI chips and their composite are described in detail in this chapter. The process flow is broken into sections covering the process steps performed on the CMOS chips, SOI wafers and the composite SOI-CMOS-MEMS chips. However, there is a large number of tasks whose successful execution are critical to the finished device’s functionality but are not of research interest, either because they have been well described in the literature (like spin casting of resist and wirebonding), or are too specific to the peculiar characteristics of the particular environment in which the devices were fabricated to be of general interest. To provide a complete picture of the process flow without belaboring such steps, the entire process flow is recorded in Appendix A with additional comments and information to enable the exact reproduction of the SOI-CMOS-MEMS fabrication process. No further reference is made to Appendix A and the reader is encouraged to follow it in parallel with the text to appreciate how these steps fit in the overall flow. Furthermore, specific literature references to generic steps such as cleaning, spin casting, lithography, etc. are not provided, however general processing text such as Madou [59], Wolf and Tauber [60] and Plummer et al. [61] are recommended to readers unfamiliar with standard microsystem fabrication processes. Resist patterns are not shown in process schematics unless they are present on the chips or wafers during intermediate steps that must be illustrated in detail.

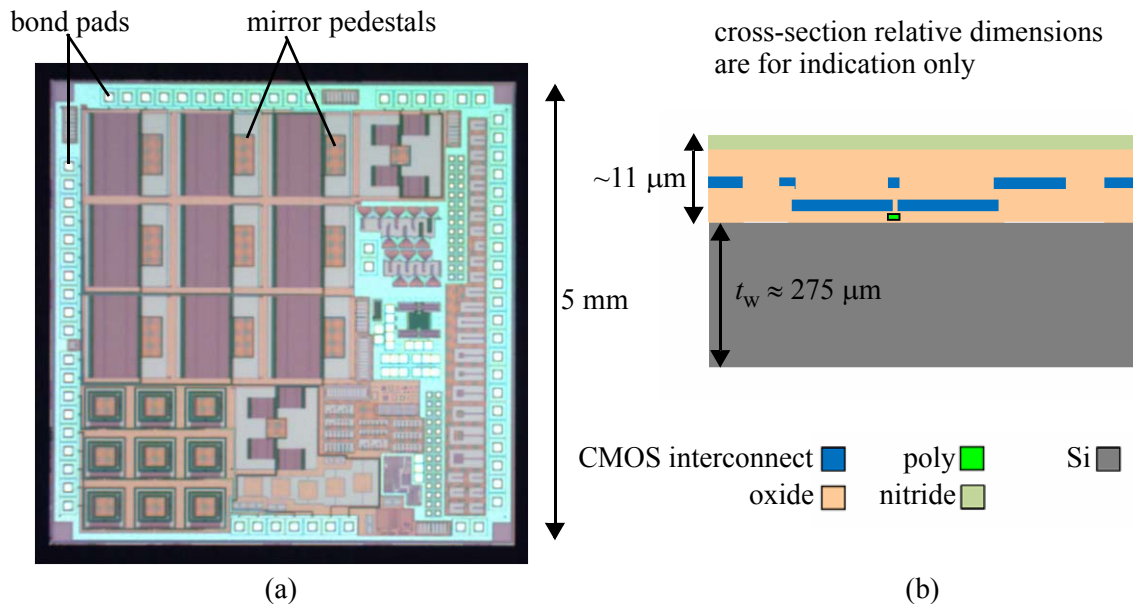
3.1 Post-CMOS Processing

The formation of MEMS devices from CMOS interconnect and dielectric layers was first proposed by Parameswaran et al. in 1989 [41]. The concept was extended by Fedder et al. [62] through the application of dry Si etching. The advantage of CMOS-MEMS lies in the stability of the foundry CMOS

processes used to produce them and the electronic integration it affords. Much work has been done in the intervening period to increase the flexibility of the concept, develop additional processing techniques and demonstrate the capability of CMOS-MEMS in application areas such as magnetic imaging sensors [63], functionalized chemical sensors [49] and scanning micromirrors [43].

Post-CMOS MEMS processing begins after the completion of CMOS fabrication, which is typically performed by a semiconductor foundry such as JAZZ Semiconductor or Taiwan Semiconductor Manufacturing Company, Ltd. (a.k.a. TSMC). At the point that the chips begin post-CMOS processing, the passivation oxide/nitride is intact over most of the chip, with the exception of the bond pads, which have been opened for wirebonding. An image of a CMOS chip as received from JAZZ Semiconductor is shown in Figure 3.1 (a) and a schematic cross-section of a MEMS micromirror is shown in Figure 3.1 (b).

FIGURE 3.1 (a) Top down microscope image of a CMOS chip as received from a semiconductor foundry. (b) Cross-sectional schematic of a MEMS micromirror pedestal and actuator.



3.1.1 Backside Aluminum Deposition and Patterning

Aluminum is sputter deposited on the backside of the CMOS chips (see schematic cross-section in Figure 3.2) to act as an etch mask in the final backside release etch process of the process flow. The

quality of the surface finish of the Al is not important but the film must be free of pinholes and must not delaminate during the intervening processes or the backside Si would be attacked during the final release etch, which would weaken the chip structurally. The thickness of the Al layer is 100 nm and is deposited on a Perkin-Elmer 8L using the conditions given in Appendix C.1. The thickness was determined based on experience and the impact of this value on the final device performance has not been characterized.

FIGURE 3.2 Schematic cross-section of a CMOS chip after backside Al deposition.

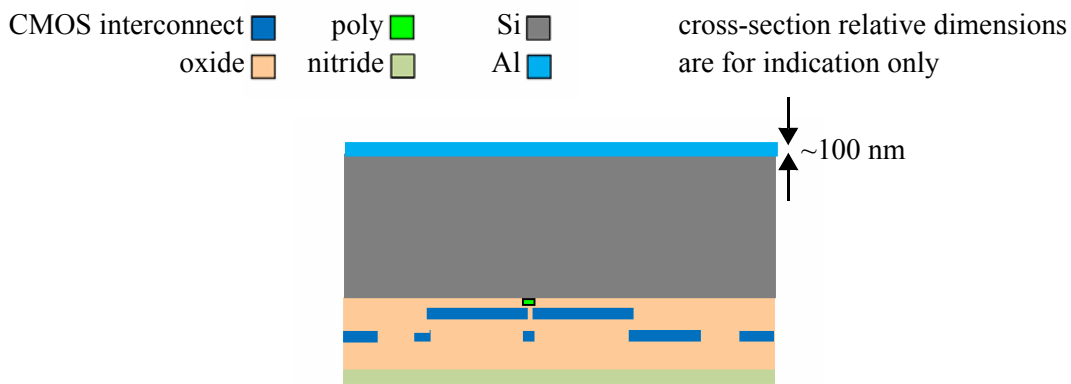
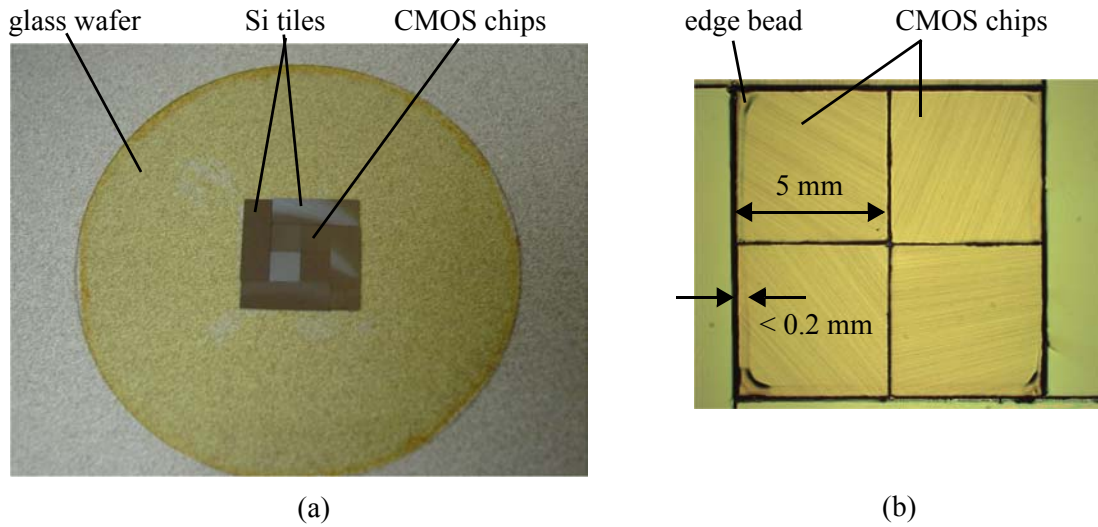


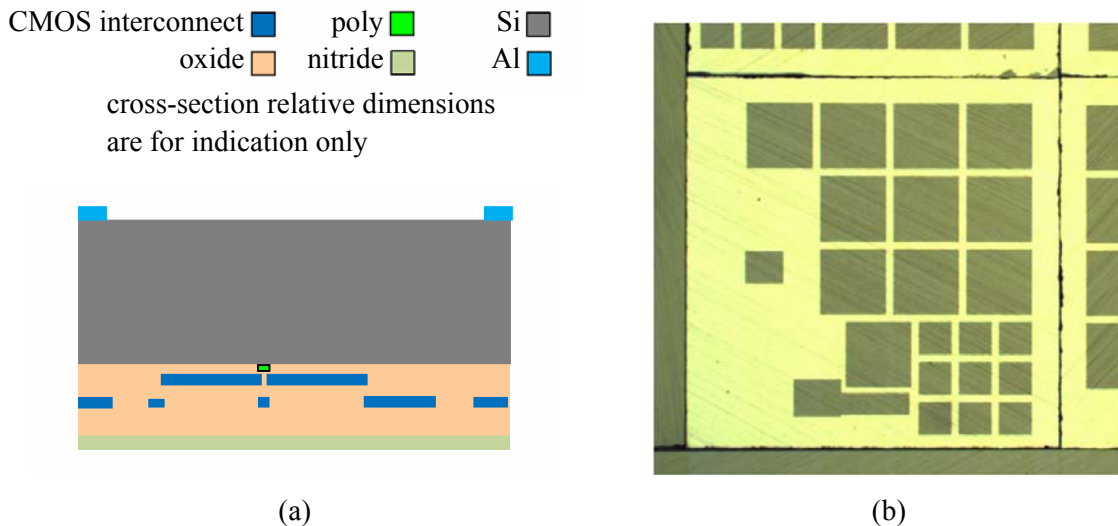
FIGURE 3.3 Photograph of four CMOS chips mounted on a 75 mm diameter glass wafer and surrounded by Si tiles whose function is to move the edge discontinuity away from the CMOS edge and reduce edge bead formation during imaging resist coat. (b) Photograph of the imaging resist after spin coat.



The CMOS are then mounted face down on a 75 mm diameter glass wafer using AZ4210 photoresist. Si tiles of thickness $\pm 5 \mu\text{m}$ of the CMOS chip thickness (i.e. $t_w + \text{CMOS stack thickness}$) are arrayed around the CMOS to reduce edge bead formation during the spinning of AZ4210 imaging resist onto the backside of the CMOS (see Figure 3.3 (b)). Si tile fabrication is described in Appendix B.4. An edge bead still occurs with Si tiles so the chips should be arranged so the backside pattern is located towards the center of the CMOS chips. Without tiling the edge bead can reach the center of the CMOS chips. The width of the backside edge bead on the CMOS limits the minimum distance from the edge of the chip at which MEMS devices can be reliably fabricated when using backside processing, modulated by the depth of focus of the lithography equipment being used. The edge bead is less than 0.2 mm.

The Al is patterned by exposing the photoresist using direct write lithography (DWL), developing it using AZ developer and using it as an etch mask for a wet Al etch (see schematic cross-section in Figure 3.4). Following Al etch, the resist is stripped and the CMOS chips are removed from the glass carrier wafer and cleaned before being remounted on the glass carrier wafer for backside Si etching.

FIGURE 3.4 (a) Cross-sectional schematic after backside Al patterning. (b) Patterned backside Al.



3.1.2 Backside ARDEM Si Processing

Backside Si etching thins the Si under the MEMS structures to enable incorporation of the Si substrate in the final device. In this step, the Si underneath the mirror pedestal and the actuators is etched to different thicknesses using Aspect Ratio Dependent Etch Modulation (ARDEM). The reader is referred to Chapter 4 for a detailed elaboration of this technique, its theoretic foundation and the analytic models that enable its application. It suffices to say here, that with ARDEM, a resist pattern with constant line width and varying space widths, correlated to the features on the frontside of the CMOS chip, is lithographically defined on the backside of the CMOS chip and used as an etch mask for a Bosch-type deep reactive ion etch (DRIE) process [64][65][66] whose etch rate varies locally, dependent on the space width [67][68]. High density regions of the ARDEM pattern with small pitches result in shallower depths than regions of the pattern with lower density and larger pitches.

The thickness of the imaging resist t_{res} depends on the selectivity of the etch process to Si over resist

$$S_{\text{Si-res}} = \frac{ER_{\text{Si}}}{ER_{\text{res}}}. \quad (3.1)$$

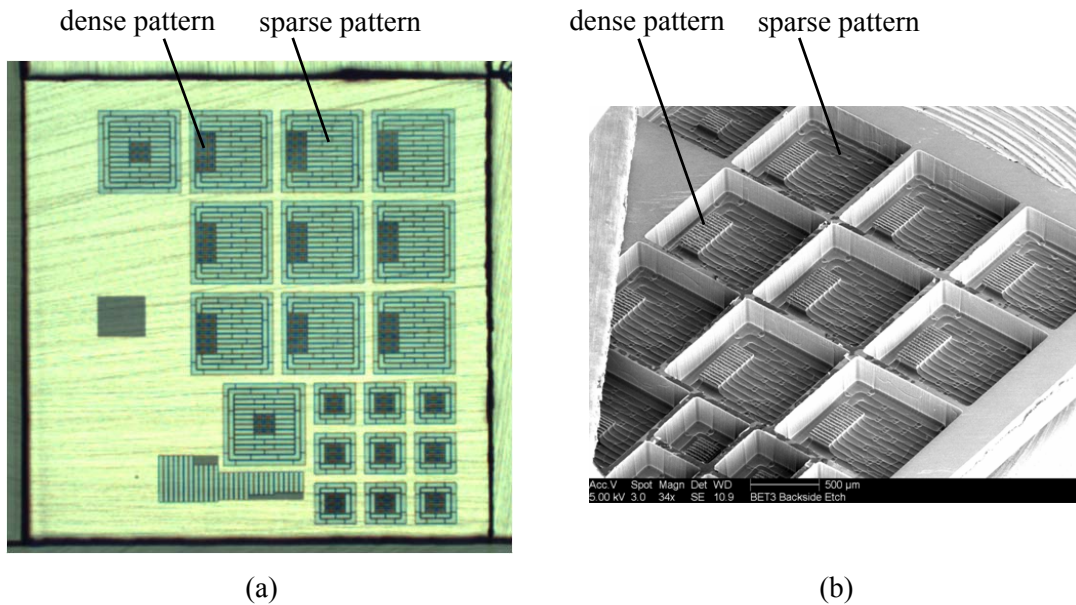
For a target etch depth in the anisotropic step of $D_{\text{Si,aniso}}$, the imaging resist thickness after resist hard-bake must meet the condition that

$$t_{\text{res}} > \frac{D_{\text{Si,aniso}}}{S_{\text{Si-res}}}. \quad (3.2)$$

To accommodate process and cross-chip variations, the thickness should be increased compared to (3.2). The amount depends on the trade-off between imaging resolution, which decreases as t_{res} increases, and the risk of resist breakthrough in the event of the process running at the bounds of the expected levels of variation.

For SOI-CMOS-MEMS mirror arrays on the millimeter scale, the pedestal length, $l_{\text{ped}} \approx 200 \mu\text{m}$ requires that Si is retained under the pedestal to prevent stress-induced bending of the pedestal in the finished device. The Si thickness under the pedestal $t_{\text{ped,Si}}$ is not optimized, but based on the work of Xie [43] $t_{\text{ped,Si}} > 25 \mu\text{m}$ is deemed sufficient to eliminate risk of bending.

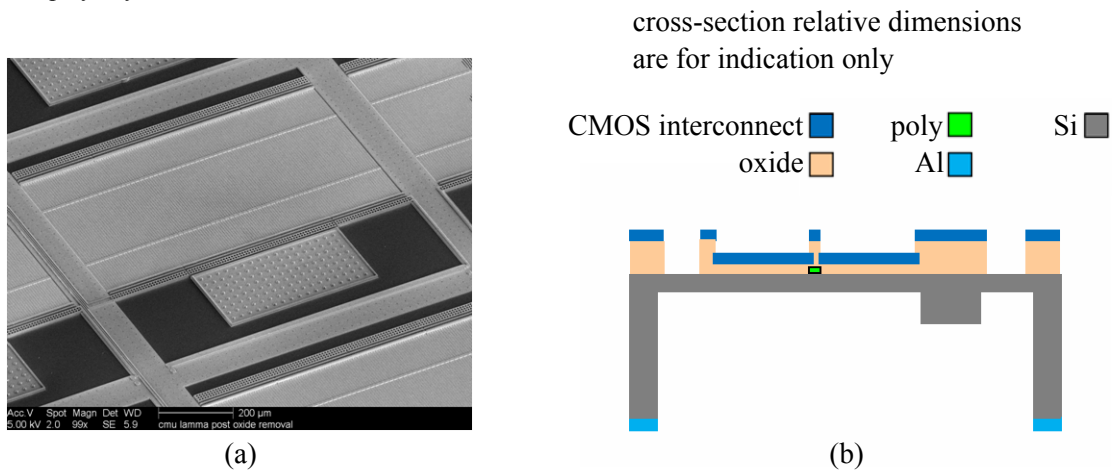
FIGURE 3.5 (a) Top down image of the backside of a CMOS chip after ARDEM resist patterning. (b) SEM image of the CMOS chip after backside Si etch.



DWL is used to expose the ARDEM pattern (see Figure 3.5 (a)) which is developed in AZ developer. In the ARDEM pattern image in Figure 3.5 (a) the dense pattern is an array of squares with a $20 \mu\text{m}$ space and the sparse pattern has a space of $50 \mu\text{m}$ width with a length at least $200 \mu\text{m}$. The 75 mm glass wafer carrying the patterned CMOS chips is mounted on a resist coated 100 mm Si wafer using $150 \text{ }^\circ\text{C}$ Revalpha Nitto Denko heat release tape. The carrier wafer is prepared using the process flow in Appendix B.6. Tapes with lower release temperatures are available and may also be suitable for mounting the glass wafer on a Si carrier but this was not investigated. The most important aspect of the mounting process is a uniform, consistent and constant thermal contact of the glass carrier wafer with the Si carrier wafer throughout the etch process. If the thermal contact is poor initially, or degrades throughout the process, the surface temperature of the CMOS chips increases and $S_{\text{Si-res}}$

shown in Figure 3.7 (a) and a schematic of the CMOS chip is shown in Figure 3.7 (b). The timing of the oxide etch is critical to the stability of the mechanical properties of the final device, increasingly so as higher levels of interconnect are used to define the mechanical structure. This is because the ion bombardment in the process is large enough to mill and chamfer the Al in the interconnect stack after the barrier metals are etched away. For example, with an optimized frontside oxide etch time, the thickness of the Al in the m3 layer is thinned by > 120 nm as shown in Figure 6.2.

FIGURE 3.7 (a) SEM of a MEMS folded actuator after frontside oxide etch. (b) Schematic cross-section of the CMOS chip after frontside oxide etch.



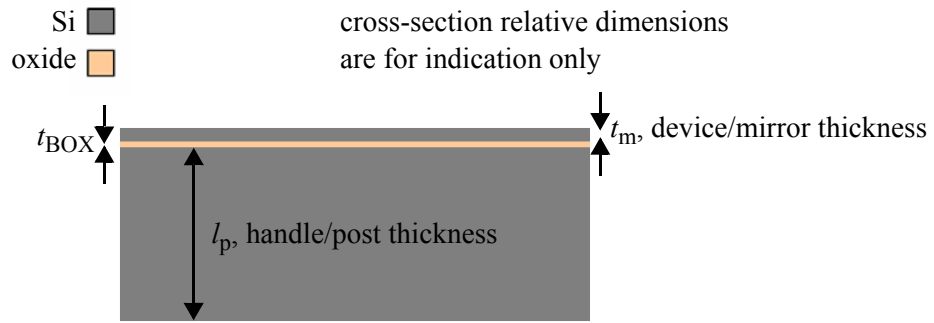
3.2 SOI Processing

Double-sided polished (DSP) SOI wafers (see Figure 3.8) are used to form the mirror and post of SOI-CMOS-MEMS mirrors. The post is formed from the handle layer and the mirror is formed from the device layer. The buried oxide (BOX) serves as an etch stop for the post etch process. As described in Section 2.5.3, the minimum thickness of the handle layer l_p given by (2.122) is defined by the linear dimension of the mirror, its range of motion and the z -displacement of the pedestal. For the mm-scale mirrors used to develop the SOI-CMOS-MEMS process the handle layer is $500 \mu\text{m}$ thick. The thickness of the BOX t_{BOX} depends on the selectivity of the post etch process to Si over oxide

$$S_{\text{Si-BOX}} = \frac{ER_{\text{Si}}}{ER_{\text{BOX}}} \quad (3.3)$$

during the overetch portion of the post etch (i.e. that time between the BOX first being exposed and the Si being completely removed), where ER_{BOX} is the etch rate of the BOX. For the BOX to be a successful etch stop layer it must be thick enough that it is not etched through during the overetch.

FIGURE 3.8 Cross-sectional schematic of a DSP SOI wafer used to fabricate the mirrors and posts of the SOI-CMOS-MEMS mirror arrays.



For a given etch process, if the minimum Si etch rate is $ER_{\text{Si,min}}$ and the maximum Si etch rate is $ER_{\text{Si,max}}$ over the etching area then ER_{Si} can be defined as the median Si etch rate and the Si etch rate range is

$$\Delta ER_{\text{Si}} = ER_{\text{Si,max}} - ER_{\text{Si,min}} \quad (3.4)$$

The condition for a successful BOX etch stop is

$$t_{\text{BOX}} > \frac{l_p}{S_{\text{Si-BOX}}} \cdot \frac{\Delta ER_{\text{Si}}}{ER_{\text{Si}}} \left(1 - \frac{1}{4} \left(\frac{\Delta ER_{\text{Si}}}{ER_{\text{Si}}} \right)^2 \right)^{-1}, \quad (3.5)$$

which for most well-engineered etch processes is sufficiently approximated as

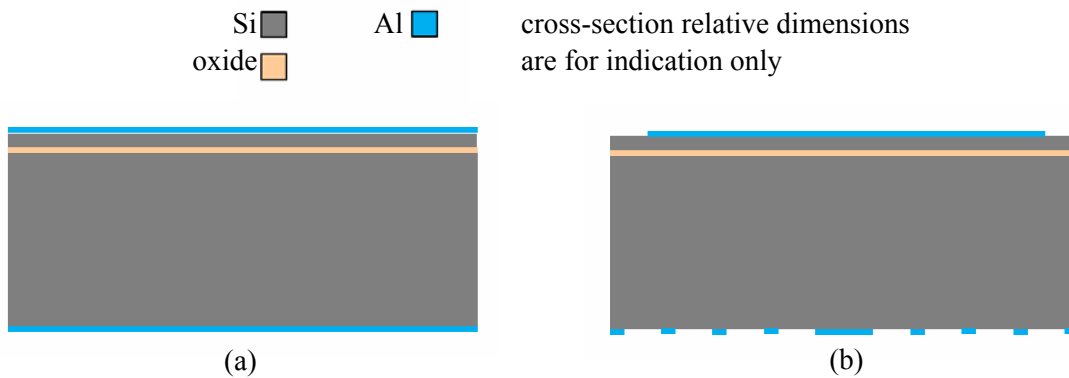
$$t_{\text{BOX}} > \frac{l_p}{S_{\text{Si-BOX}}} \cdot \frac{\Delta ER_{\text{Si}}}{ER_{\text{Si}}} \quad (3.6)$$

For the post etch process used in this research $t_{\text{BOX}} = 1 \mu\text{m}$. The minimum thickness of the device layer is determined by the mechanical modes of the mirror in comparison to the expected operating conditions of the device, the ability of the device layer to survive the fabrication process, the impact of reflective coating stress on mirror curvature and it is constrained on the upper end by the desired FF . For $FF = 95\%$ and mm-scale mirrors, $t_m = 25 \mu\text{m}$.

3.2.1 Mirror and Post Patterning

Al is used to form the mirror surface and the base of the post. The Al is sputter deposited on both sides of the wafer (see Figure 3.9 (a)) with a Perkin-Elmer 8L using the process conditions given in Appendix C.1. The Al is 100 nm thick on both sides. This thickness of Al film does not have holes that could lead to undesirable Si etching at other stages of the process. The impact of Al thickness and stress on the curvature of the mirrors has not been characterized and is an area that should be investigated further. The surface finish of the mirror is critical to its reflectance and hence substrate cleaning and inspection must be done with care prior to Al deposition.

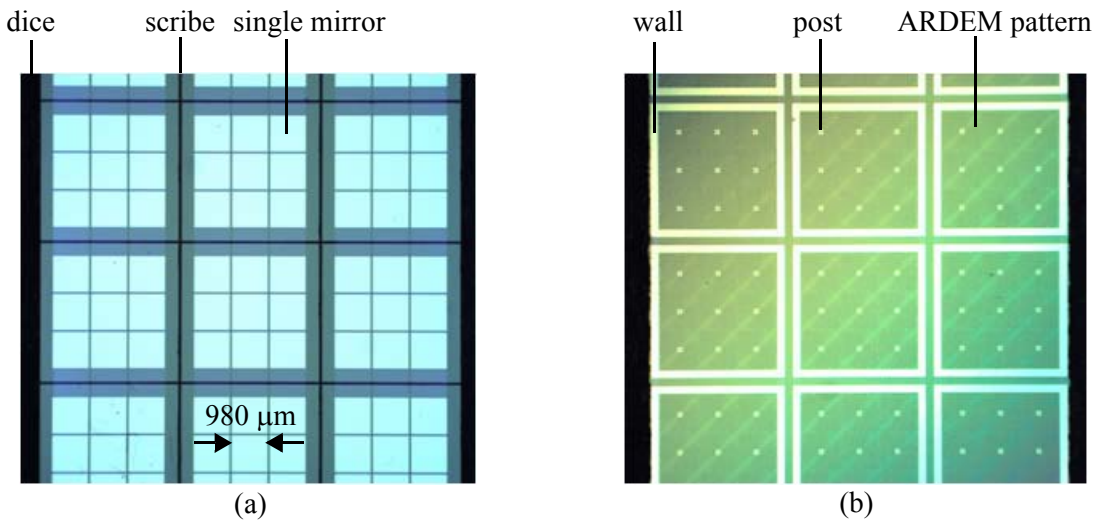
FIGURE 3.9 (a) Cross-sectional schematic of the SOI wafer after Al deposition. (b) Cross-sectional schematic of the SOI wafer after mirror and post patterning.



Following Al deposition, the mirror and post patterns are formed on the device and handle sides of the SOI wafer, respectively through contact lithography and wet Al etch (see Figure 3.9 (b)). The two sides are patterned separately. The side not being patterned is coated with a protective layer of resist to prevent scratching of the Al surfaces. After the second wet Al etch, the wafer is scribed on the mirror

side to a depth of $t_m + 5 \mu\text{m}$ to define individual mirror die and then blocks of mirror die are diced from the wafer (the block size has tended to be driven by handling concerns i.e. large enough to handle easily, but small enough to prevent breakage - 10 to 20 mm on a side has proved manageable) (see Figure 3.10). The scribe must be deep enough to penetrate below the BOX on the device side so the mirror die are singulated during the post Si etch.

FIGURE 3.10 Plan view photographs of (a) the scribed mirror/device side of the SOI wafer and (b) the post/handle side of the SOI wafer for an array of mm-scale mirrors.



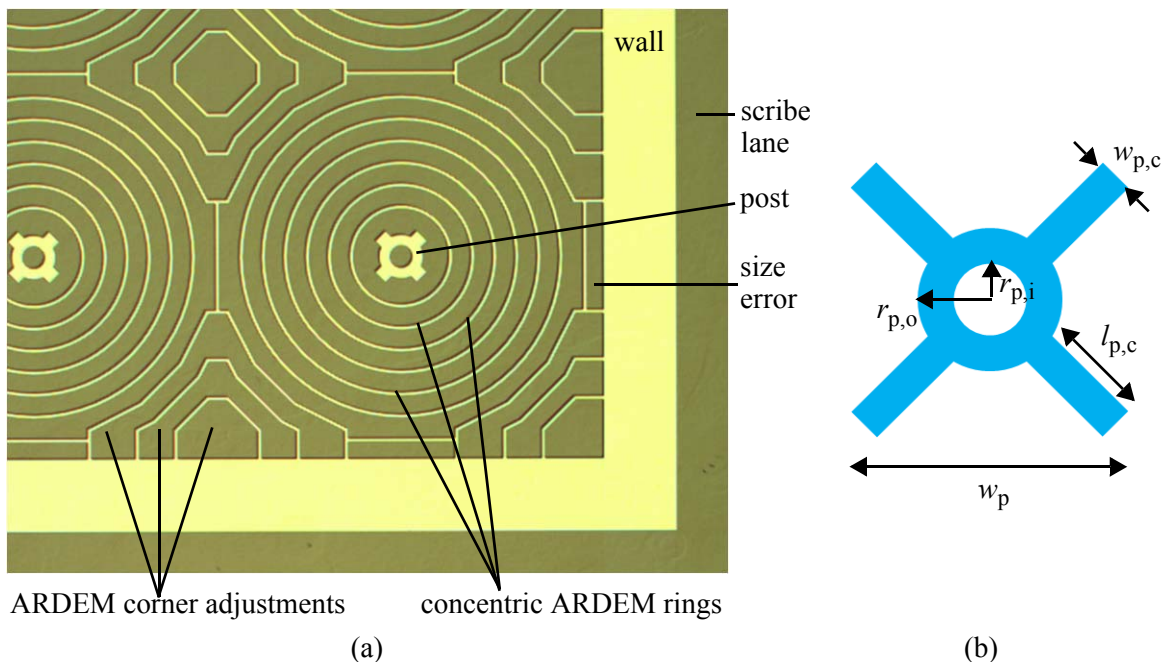
The ARDEM concept is used for the post etch so the pattern is more complex than simply small Al islands in a large field. ARDEM in the context of the post etch is used primarily to improve etch rate uniformity so that thinner BOX layers can be used and the models of Chapter 4 are relevant in this respect, however ARDE also modulates lateral etching, bowing and notching. These ARDE effects have not been fully characterized in terms of mask geometry and feature depths and the critical AR ranges are derived empirically. Post etch ARDEM is illustrated and described in greater detail in the following section.

3.2.2 Post Profile Control by ARDEM

ARDE has been shown to impact other characteristics of the etch process as well as etch rate. Control of notching [69][70] and trenching [63] have been demonstrated using sacrificial patterns that

locally vary the AR of an etching structure and this property is used in post etching. The post ARDEM pattern consists of concentric rings (see Figure 3.11 (a)) with equal characteristic dimensions d (see Section 4.3.5) encircling the posts to improve etch uniformity. When the concentric circles begin to merge the radial symmetry breaks down and more complex patterns are needed to fill the space. Based on observation of etch rate dependence on shape, acute angles are avoided. The limits of pattern dependence of ARDE has not been thoroughly explored and could be a useful research area if the prohibition on acute angles proves too limiting. The irregular ARDEM features are designed to maintain the characteristic dimension of the rest of the pattern and to maintain symmetry when replicated in a regular array. The automatic generation of features of equal characteristic dimension to fill an arbitrary space is a problem that has not been explored, but if ARDEM were to be used extensively for irregular layouts such an investigation would be invaluable.

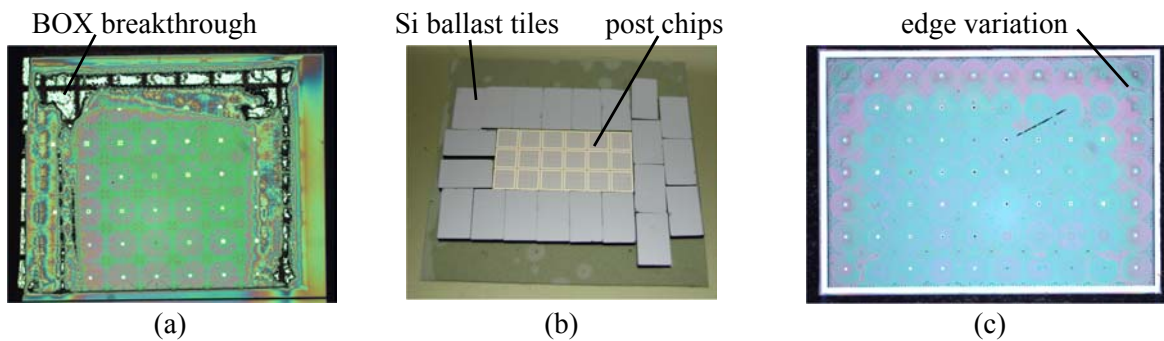
FIGURE 3.11 (a) Photograph of the detail of the ARDEM and post pattern on the SOI wafer for a mm-scale mirror. (b) Schematic layout of a post.



Preliminary post etch tests were done using different ARs around the posts to identify process trends. The inner ring around the post typically defines d for the rest of the chip but for these tests a single set of outer rings was used for all posts and only the geometry of the post and the radius of the

innermost ring was adjusted to vary the AR seen by the post. The 2-D post layout comprises two structures: a ring and a cross as shown in Figure 3.11 (b). The ring post reduces post mass compared to a solid post, while the cross structure enhances mechanical stiffness faster than it adds mass for the same effective width w_p . The post geometry is characterized by the inner and outer radii of the ring $r_{p,i}$ and $r_{p,o}$, respectively and the width $w_{p,c}$ and length $l_{p,c}$ of the arms of the cross.

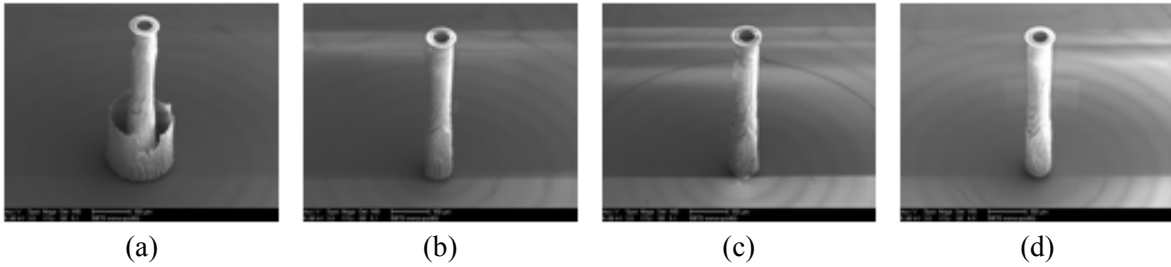
FIGURE 3.12 (a) A post chip with BOX breakthrough. (b) Si tiles arrayed around post chips to act as ballast. (c) A post chip etched using Si ballast tiles has no oxide breakthrough, although edge etch rate variation is clearly visible.



500 μm handle thickness SOI wafers were used for the tests. The post chips were mounted on a resist coated 100 mm diameter Si carrier wafer using 150 $^{\circ}\text{C}$ Revalpha Nitto Denko heat release tape. The carrier wafer preparation is critical because it must withstand ~ 7 hrs of etching and is done using the process flow in Appendix B.7. The Si was etched on a STS-ASE chamber using the process conditions given in Appendix C.2. Due to ARDP which leads to an increase in lateral etching of the structures as the depth increases, the passivation cycle time is increased and the etch cycle time is decreased as the depth of the etch increases. Without passivation ramping, no posts survived the etch process. Similar to backside ARDEM, the anisotropic process is followed by a polymer removal and a short isotropic etch. It was found that an extreme variation in etch rate, likely due to microloading variation, occurred at the edge of the etching post chips that resulted in BOX breakthrough as shown in Figure 3.12 (a). By arraying 1 mm thick tiles of Si around the etching chips, as shown in Figure 3.12 (b), to act as ballast for the reactive F in the plasma, BOX breakthrough is prevented (see Figure 3.12 (c)). Fabrication of Si etch ballast tiles is described in Appendix B.5.

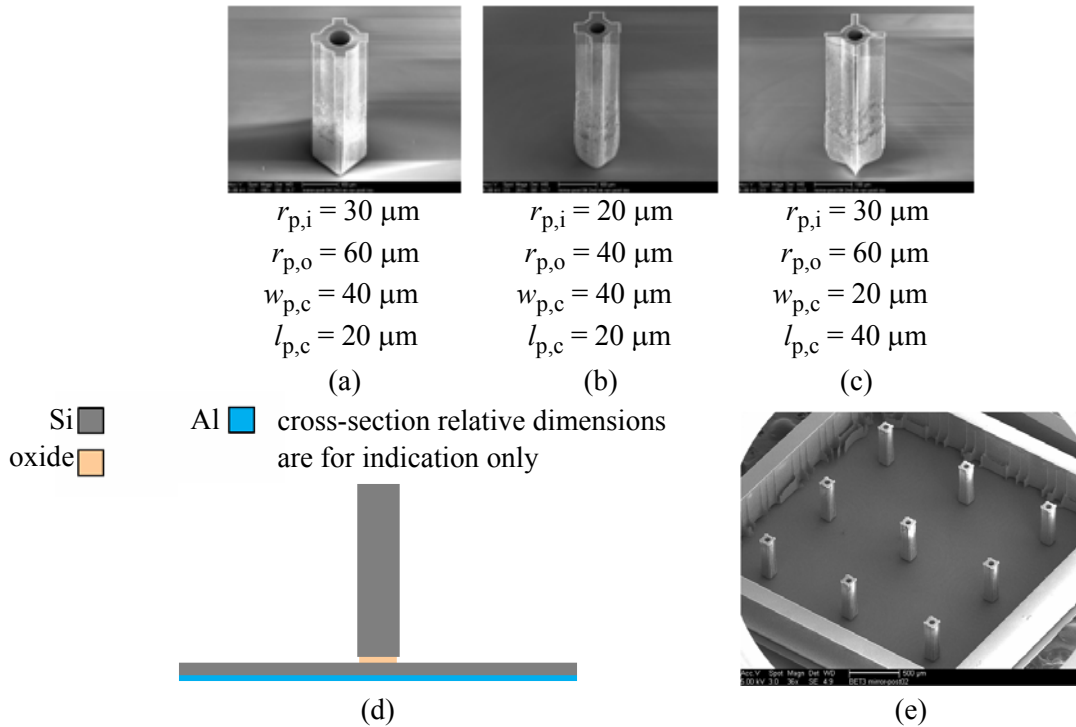
The first test was run with a constant radius of $130\ \mu\text{m}$ for the innermost ring but varying post width and shape. Based on the results of this test, a second test was done in which a smaller range of post widths and varying innermost ring radius was used. The full results of the two tests are shown in Appendix E, but a sample of etched post images are shown in Figure 3.13 that demonstrate the important trends. As AR increases the tapering of the sidewalls at large etch depths increases resulting in a wider base of the ARDEM pattern that takes longer to remove in the isotropic process. As AR decreases, the notching and sidewall attack increases to the point that the entire post is etched away (nb. the post for $AR = 6.3$ did not survive). It appears there is a small process window between being unable to remove the ARDEM pattern and maintaining intact posts.

FIGURE 3.13 SEM images of etched posts with $r_{p,i} = 20\ \mu\text{m}$ and $r_{p,o} = 40\ \mu\text{m}$ showing the variation in post profile for different AR: (a) 13, (b) 10, (c) 8.3, (d) 7.1.



Based on the preliminary tests, the mm-scale mirrors are fabricated with three types of post with a cross shape as shown in Figure 3.14 (a) to (c). The post chips are etched as described above for the preliminary tests. Following post etch, the chips are cleaned in an O_2 plasma to remove all etch polymers and the BOX is removed in buffered hydrofluoric acid (BHF). The completed mirror chip is shown schematically in Figure 3.14 (d) and in a SEM image in Figure 3.14 (e).

FIGURE 3.14 (a) to (c) SEM images of the post types selected for mm-scale mirror fabrication. (d) Schematic cross-section of a post after etch. (e) Type (a) post chip after etch and buried oxide removal.



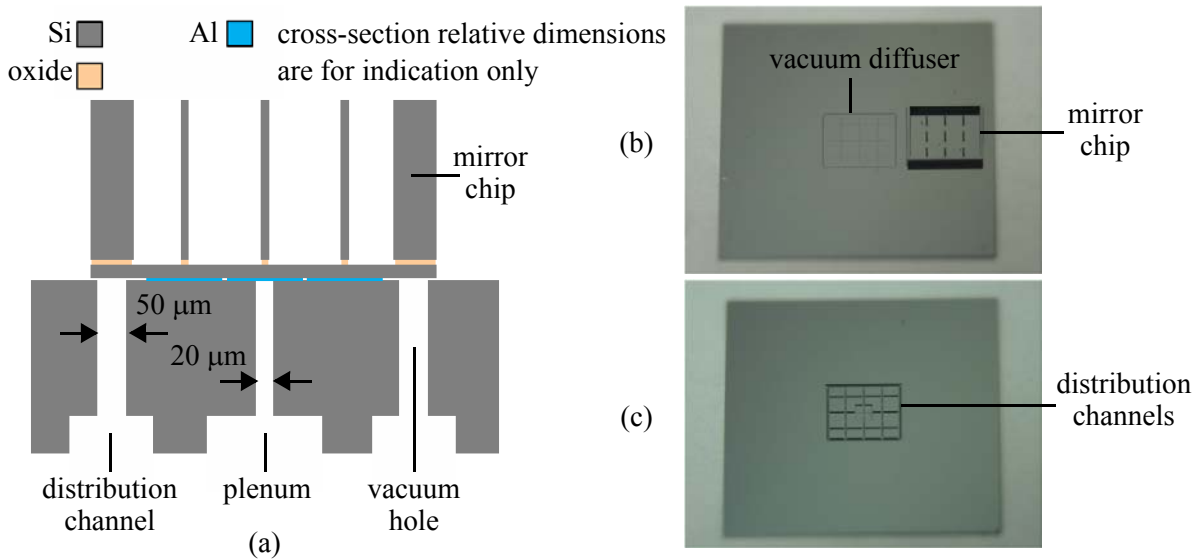
3.3 SOI-CMOS-MEMS Processing

This section describes the process steps in which the CMOS-MEMS die and the SOI mirror die are bonded together and etched to release all the mechanical structures. During this part of the processing a catastrophic electrical failure was discovered in which the TiW barrier metals and W vias are etched away. This effect has its origin in the heating of the structures during the release etch processes. The investigation of this phenomena is described in detail in Chapter 5. The released structures reach very high temperatures (as high as 350 °C) which dramatically changes the selectivity of the process to TiW barrier metal and W vias, leading to their attack. The release processes described in this section reflect the learning gained from the investigation of etch heating, but otherwise the phenomenon is not discussed further until Chapter 5.

3.3.1 Flip-Chip Bonding

A Laurier M9-A device bonder is used to bond the CMOS-MEMS and the SOI mirror chips. The adhesive is a two-part epoxy system called EPO-TEK 377 [71]. This epoxy was chosen for its operating temperature of 200 °C, its 98% solid content indicating very little solvent to evaporate and contaminate the bonder, its low shrinkage (2%), which minimizes stress during curing, its very low viscosity (< 300 cPs), which makes it easy to dispense and its 24 hour pot life, which allows it to be mixed and used over a days work in the lab. The curing time for the epoxy is 1 hr at 150 °C but the supplier indicated that the curing time for a two part epoxy is also dependent on the volume, so for the sub-nL quantities being used the cure time on the bonder was increased to 60 min at 160 °C followed by an overnight cure at 150 °C. This process is sufficient to bond mm-scale mirrors however optimization of the curing schedule has not been investigated.

FIGURE 3.15 (a) Cross-sectional schematic of a vacuum diffuser plate. (b) Vacuum diffuser plate, frontside with mirror chip. (c) Vacuum diffuser plate, backside.

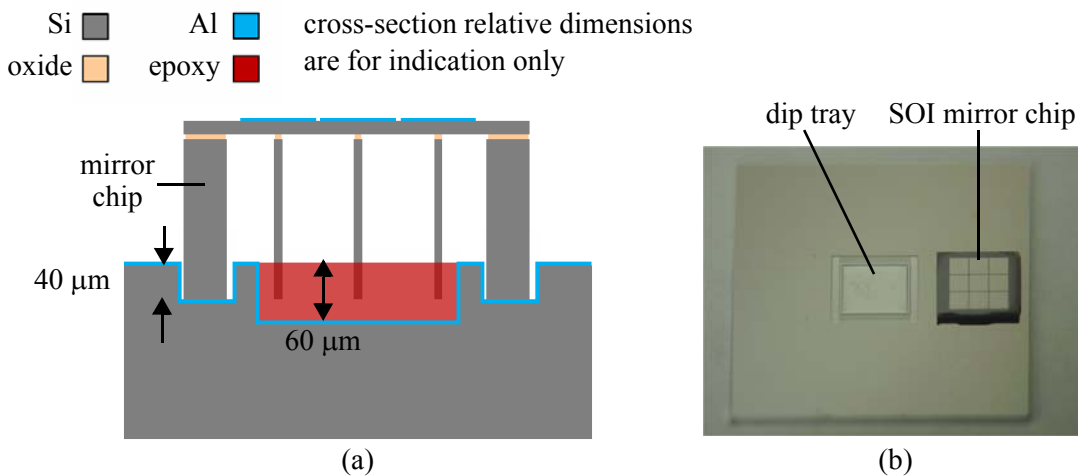


The bonder has lower and upper chucks and each half of the bonded chip is held on the chucks by vacuum during the bonding process. Because flatness and coplanarity of the two pieces is critical to bonding success flexing of either chip must be avoided. Custom vacuum diffuser plates were fabricated that hold down the chips only on their rigid surface or provide a symmetric stress pattern that

prevents flexing at the bond sites. The diffusers are fabricated from 100 mm diameter, 220 μm thick DSP Si wafers with double sided lithography and etching. The detailed diffuser process flow is given in Appendix B.2. A cross-sectional schematic of a vacuum diffuser plate is shown in Figure 3.15 (a) and photographs of the front and back of a diffuser are shown in Figure 3.15 (b) and (c).

The epoxy is prepared according to Appendix B.3 and dispensed to a dip tray using a 1 mL syringe with a 26 gauge needle. The dip tray is formed from a 100 mm diameter, 500 μm thick Si wafer using the flow given in Appendix B.1 and is shown in schematic and photograph in Figure 3.16. The surface of the dip tray is coated with Al to facilitate wetting of the dip tray by the epoxy. For other adhesive materials different wetting enhancing coatings may be needed.

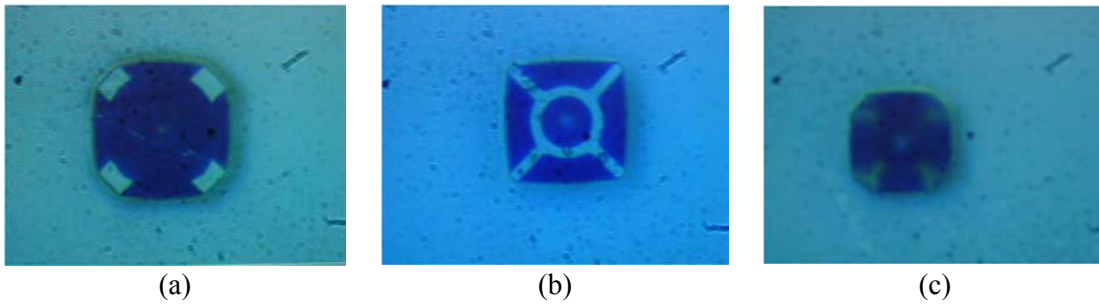
FIGURE 3.16 (a) Cross-sectional schematic of epoxy dip tray and mirror chip for mm-scale mirrors. (b) Photograph of a dip tray with post chip.



Due to limitations in device bonder vacuum control, the posts are dipped into the epoxy under manual control. For mm-scale mirrors, the wall of the mirror chip is removed at the end of the process and is not dipped into the epoxy. The base of the wall is the only surface that makes mechanical contact with the dip tray and hence the dipping force is concentrated on it. Manual control of the z -motion of the bonder lower chuck is used to bring the dip tray up to the mirror chip until a contact force is observed (~ 100 g). The dipping force is increased slowly up to 500 g and held for 10 s. This time is arbitrary but proved to be successful so no further investigation was done. After dipping, the lower

chuck is returned to its home position while the dipped mirror chip remains on the upper chuck. Photographs of the camera image of the posts with epoxy on them are shown in Figure 3.17. The cross-arms of the post appear to be a significant factor in the amount of epoxy picked up by the post.

FIGURE 3.17 Photographs of posts from Figure 3.14 after epoxy dipping, in the same order as shown in Figure 3.14. Magnification is constant.



The dip tray is removed from the lower chuck and replaced with the CMOS diffuser plate and a CMOS-MEMS chip (see Figure 3.18). The SOI mirror chip and the CMOS-MEMS chip are aligned and co-planarity of the two chips is achieved using the pitch and roll adjustment capability of the device bonder. The CMOS-MEMS chip on the lower chuck is moved up to contact the SOI mirror chip with a contact force of 200 g. The temperature of the upper and lower chucks is raised to 160 °C and held for 1 hr. The vacuum is released on the SOI mirror chip and the lower chuck is homed. The now-bonded SOI-CMOS-MEMS chip shown in Figure 3.19 is placed in a 150 °C oven for 12 hrs (i.e. overnight) for the epoxy to finish curing.

FIGURE 3.18 (a) Photograph of CMOS-MEMS chip and diffuser plate. (b) Photograph of the mixed camera image of the dipped SOI post overlaid with the CMOS-MEMS mirror pedestal.

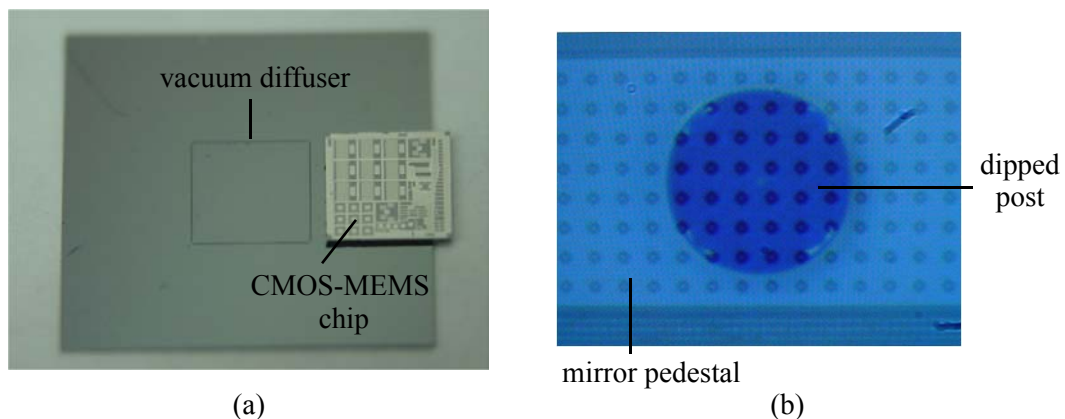
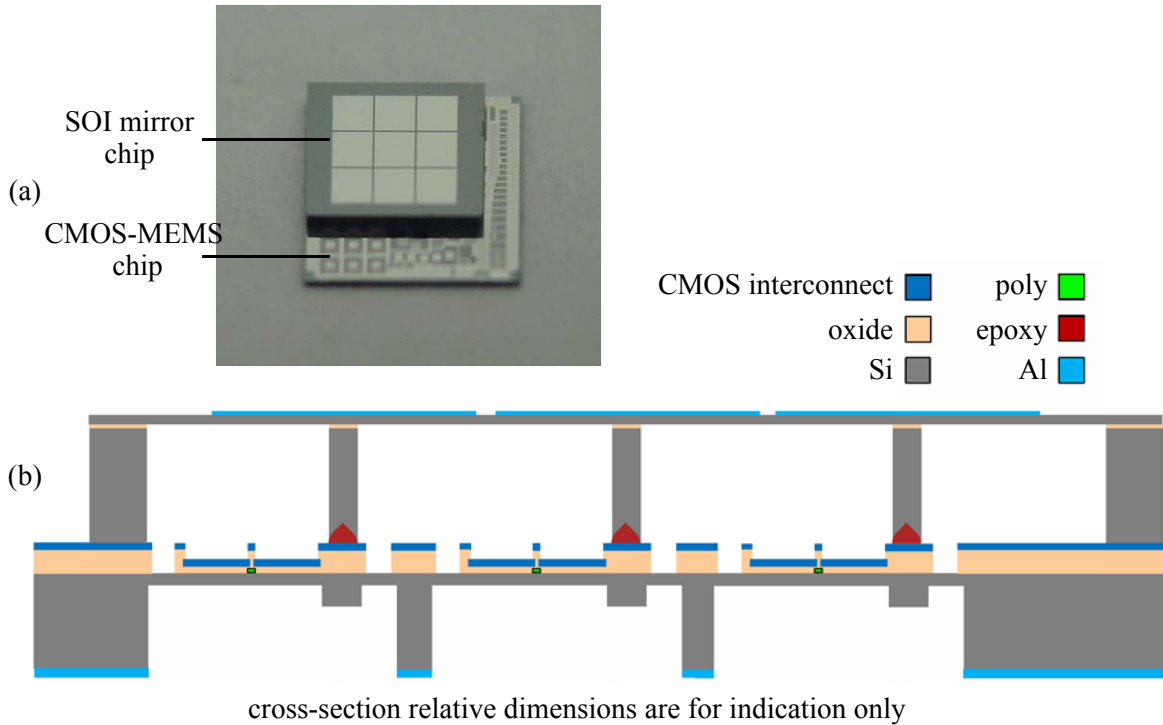


FIGURE 3.19 (a) Photograph of a bonded and cured SOI-CMOS-MEMS chip. (b) Cross-sectional schematic of the bonded SOI-CMOS-MEMS chip.



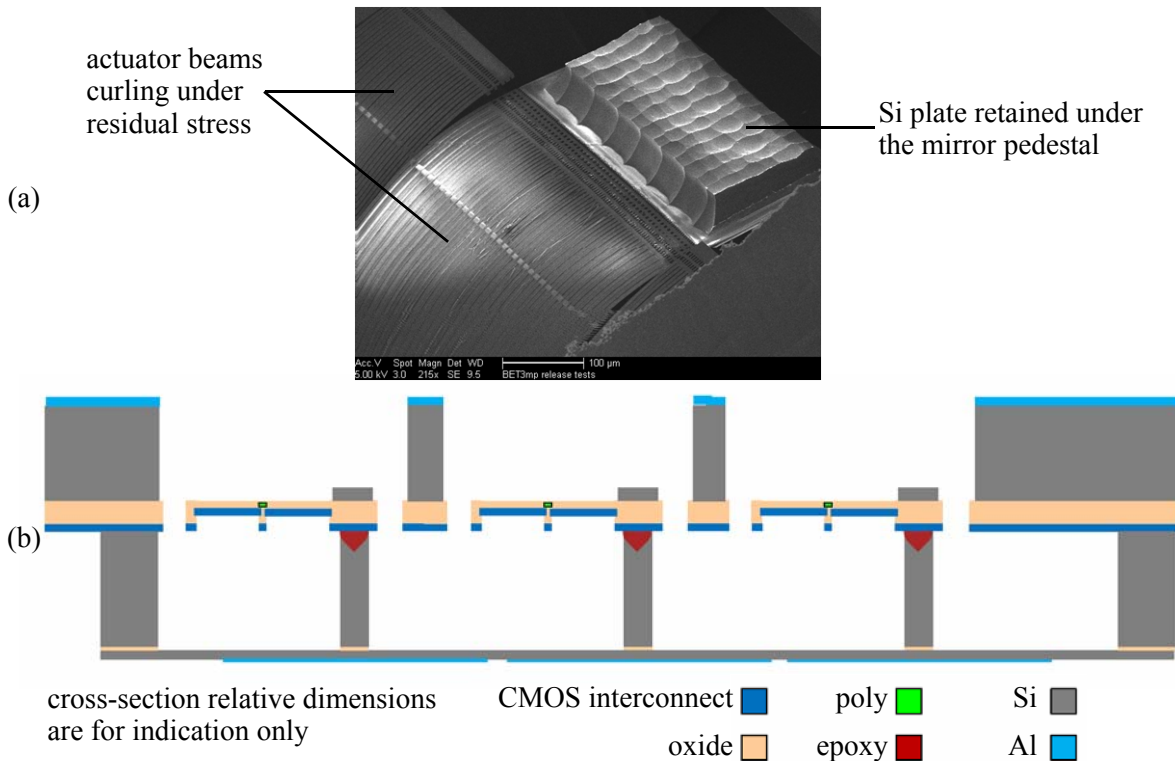
3.3.2 Backside CMOS-MEMS Release

The SOI-CMOS-MEMS mirror array is released in two stages. First, the continuous Si plate on the underside of the CMOS is removed and then the mirrors are released. The separate backside and frontside plasma release etch process is an innovation of this research. The SOI-CMOS-MEMS chip is mounted mirror side down on a blank Si wafer using 120 °C Revalpa Nitto Denko heat release tape. Again, good thermal contact is essential or loss of Si anisotropy will occur and selectivity to barrier metals and W vias will decrease leading to electrical open circuits. 120 °C heat release tape is used because of the three options available from the CMU Nanofabrication facility (90 °C, 120 °C, 150 °C) it has the lowest residual adhesiveness after heat release. A blank Si wafer is used as a carrier to act as ballast for the F neutrals in the plasma which reduces the Si etch rate and further protects the chip from etch heating effects. As a final precaution, the etch process given in Appendix C.2 is modified by

reducing the platen power in the anisotropic etch step from 12 W to 6 W which reduces ion bombardment and the etch heating caused by it.

The endpoint of the backside release etch process is done manually and the total time is dependent on the thickness of the Si plate defined by the backside ARDEM process described in Section 3.1.2. Over etch should be minimized to protect the poly heaters and to reduce the impact of etch heating induced barrier metal attack. The CMOS-MEMS actuators are fully released in this step and curl under the action of residual stress in the CMOS stack (see Figure 3.20 (a)). A cross-sectional schematic of the SOI-CMOS-MEMS chip at this stage is shown in Figure 3.20 (b). This curling and the barrier metal attack that accelerates after the actuator is released are thought to be the main causes of coplanarity excursions of mirrors in the array observed after mirror release etch shown in Section 3.3.3.

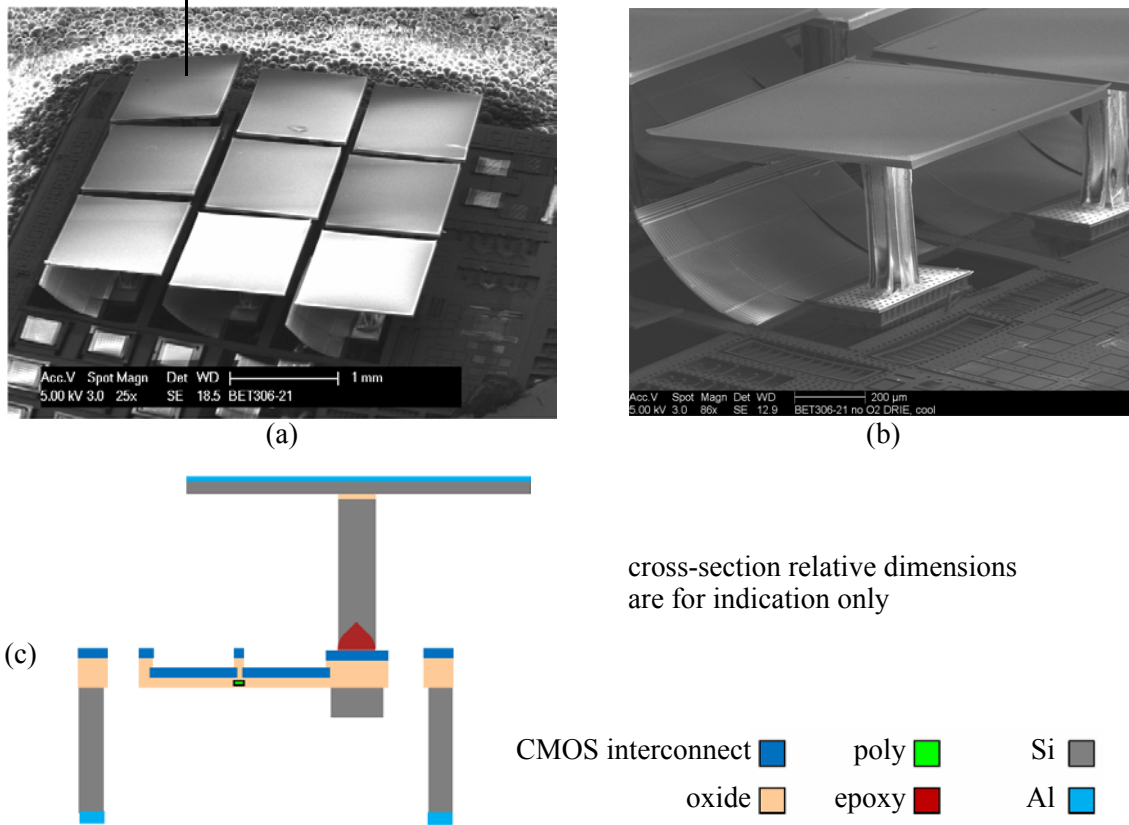
FIGURE 3.20 SEM of the backside of CMOS-MEMS actuator after backside release etch. (b) Cross-sectional schematic of the SOI-CMOS-MEMS chip after backside CMOS-MEMS release etch.



3.3.3 Frontside Mirror Release

Following the backside CMOS-MEMS release etch the SOI-CMOS-MEMS chip is demounted from its carrier and remounted on the same Si carrier wafer using heat release tape so the mirror side is exposed to the plasma. The chip is etched using the process in Appendix C.2 to a depth of $\sim 20\ \mu\text{m}$, at which point, the platen power is reduced to 6 W and the process sequence is changed so that after every 2 passivation/etch cycles the plasma is shut off and the chamber is pumped out. In this way, anisotropy of the Si etch is maintained and the attack of barrier metals and W vias is reduced enough that the electrical functionality of the chip is preserved.

FIGURE 3.21 (a) SEM of a released SOI-CMOS-MEMS mm-scale mirror array. (b) Close-up SEM of a single SOI-CMOS-MEMS mirror. (c) Schematic cross-section of a SOI-CMOS-MEMS mirror after release etch. significant planarity excursion



An image of a released SOI-CMOS-MEMS chip is shown in Figure 3.21 (a), a close-up of a single mirror is shown in Figure 3.21 (b) and a cross-sectional schematic is shown in Figure 3.21 (c). The issue of loss of coplanarity among array elements is visible in Figure 3.21 (a) where the upper-left ele-

ment of the array has a significant difference in rest angle from the rest of the members of the array. The cause of this is thought to be barrier metal attack in the actuator beams caused by etch heating. The actuator beams are multimorphs of oxide, Al and TiW for the JAZZ Semiconductor technology. Equation (2.112) states that the curvature of a multimorph is inversely proportional to its flexural rigidity $(EI)_{\text{eff},y}$. As the barrier metals are etched away in the release etch $(EI)_{\text{eff},y}$ decreases but the main sources of the residual stress difference, oxide and Al, remain constant, so the curvature increases. The etch heating power is input to the structure where Si is etching at the pedestal and mirror and where ion bombardment is greatest at the mirror surface. The temperature gradient from the power source to the thermal ground leads to the inner actuator being hotter than the outer actuator. The barrier metals of the inner actuator are etched more rapidly as it is hotter so its curvature increases faster than the outer actuator, breaking the symmetry of the folded structure and inducing a mirror rest angle.

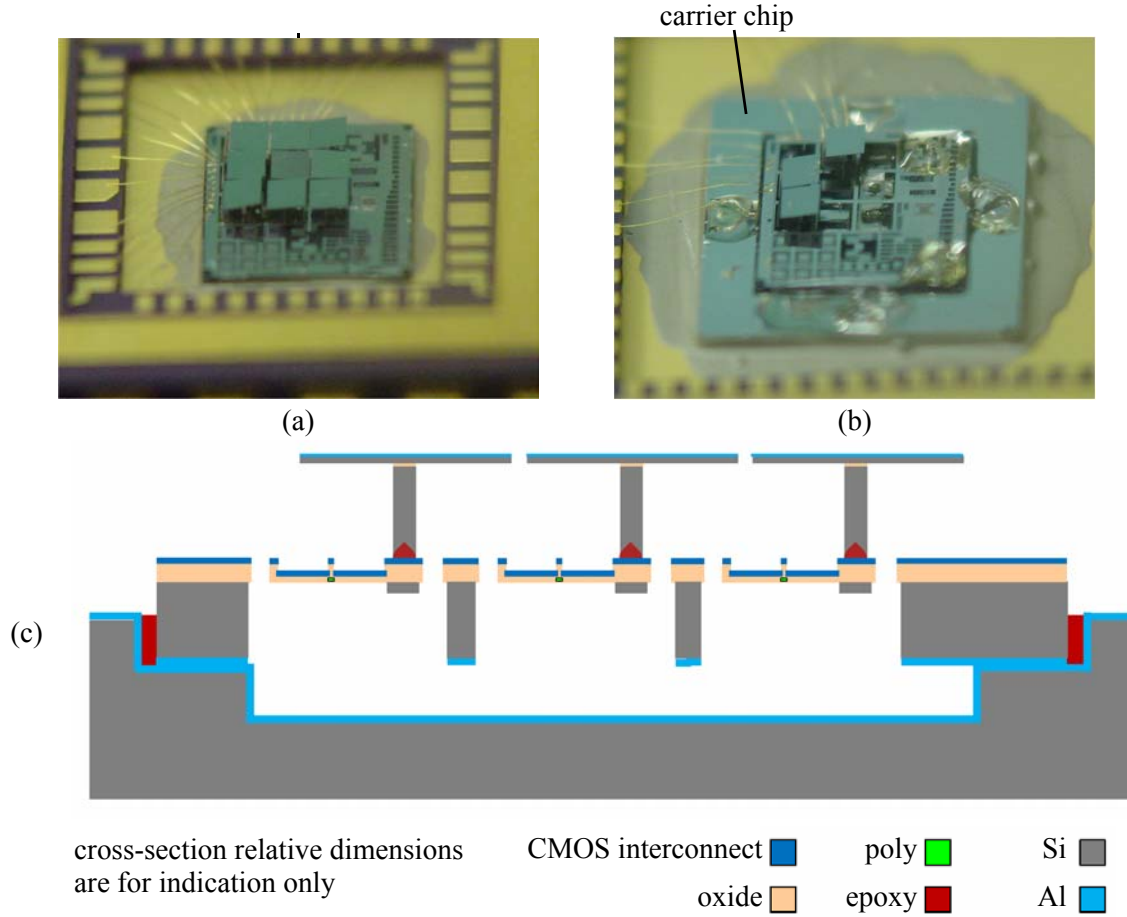
The image of a single mirror in Figure 3.21 (b) illustrates an important point for post geometry design and bonding performance. The image of the post tips with epoxy on them in Figure 3.17 show a large quantity of epoxy is picked up during dipping and the quantity depends on the length of the cross arms $l_{p,c}$. Figure 3.21 (b) shows the epoxy is not only collected at the tip but is also wicked up the side-wall of the post to a height of $\sim 100 \mu\text{m}$ and some of the polymer wicks back down onto the pedestal during bonding. The process of polymer collection and delivery to the pedestal is important to the strength and quality of the bond. The control of polymer wicking and delivery using post geometry has not been characterized but it could prove to be a beneficial avenue of research for optimizing device robustness.

3.3.4 Device Packaging

SOI-CMOS-MEMS chips can be mounted directly on a dual inline package (DIP) (ex. Figure 3.22 (a)) using an adhesive such as Ag paste, provided the range of motion in the z -direction does not exceed the chip thickness t_w as described in Section 2.5.3. If the condition in Section 2.123 is

not met a carrier chip can be used as shown in Figure 3.22 (b) and (c). The carrier chip has a recessed pocket that allows the mirror pedestals a greater range of z -motion than the thickness of the chip alone. The fabrication, design and use of the carrier chip is described in detail in [72].

FIGURE 3.22 (a) Photograph of a SOI-CMOS-MEMS chip mounted directly in a DIP. (b) SOI-CMOS-MEMS chip bonded into a carrier chip that is mounted directly in a DIP. (c) Cross-sectional schematic of an SOI-CMOS-MEMS chip in a carrier chip.

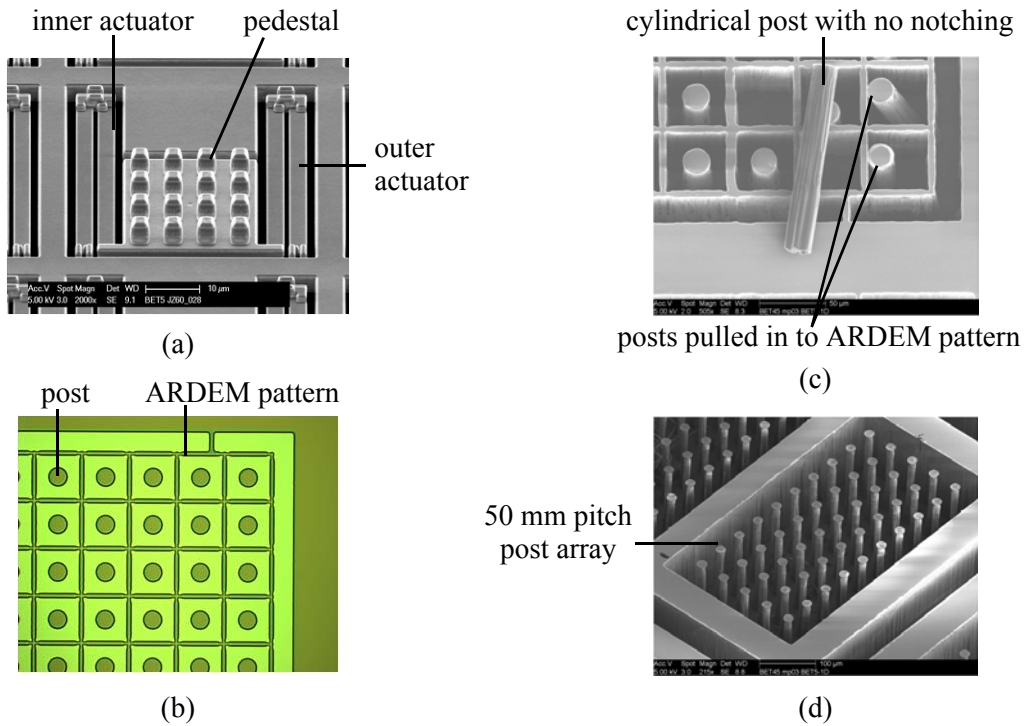


3.4 Fabrication Technology Scaling

A goal of the research documented in this dissertation was to develop a scalable fabrication platform that could be used to produce micromirror arrays at a range of scales to span the application space from large scanning mirrors to SLMs. Actuators for mirror arrays on pitches of 500 μm , 100 μm and 50 μm were designed and fabricated through the foundry CMOS process. Mirror/post chips, dip trays

and diffuser plates were designed and put through the fabrication sequences detailed in this chapter. The posts on the 50 μm pitch mirror/post chips do not survive post etch. The posts on the 100 μm pitch mirror/post chips do not survive BHF oxide removal. The mirrors on the 500 μm pitch devices do not survive flip-chip bonding. This sub-section describes and discusses the cause of the scaling failures and offers suggestions for future process development to overcome these issues. The SOI wafer used for the process scaling research has a 150 μm handle layer, a 0.5 μm BOX and a 5 μm device layer. Due to the CD bias of the post patterning process the width of the ARDEM line is 5 μm .

FIGURE 3.23 (a) SEM image of a 50 μm pitch mirror actuator with a $w_{\text{ped}} = 20 \mu\text{m}$. (b) Photograph of ARDEM pattern for the post of the 50 μm pitch mirror. (c) SEM image of posts broken during etch by an electrostatic pull-in failure mode. (d) 50 μm post array processed by varying etch:passivation ratio throughout the etch process.



3.4.1 50 μm Pitch Post Etch Fabrication

The actuator of the 50 μm pitch mirror is shown in Figure 3.23 (a). The mirror pedestal of this design is 24 μm wide and $w_p = 15 \mu\text{m}$ to fit the post and epoxy on the pedestal. The post ARDEM pattern is shown in Figure 3.23 (b). The post is sized at 20 μm to account for the lateral shrinkage that

occurs during the isotropic part of the post etch process. The observed failure mode is breakage of the posts at the interface with the SOI. The failure occurs before the ARDEM pattern is removed.

The etch process was stopped at various points close to the endpoint of the anisotropic step when the Si breaks through to the BOX. The occurrence of broken posts began only after breakthrough and increases during the overetch. Broken posts come in two flavors: distributed on top of the ARDEM pattern, or stuck to the ARDEM pattern inside their respective holes as shown in Figure 3.23 (c). Those that lie on top of the ARDEM pattern are almost perfect cylinders indicating notching is not the mechanism by which the posts are detaching from the substrate. The most likely explanation is that when the Si breaks through the posts become electrically isolated and charge to a different potential than the ARDEM pattern. When the potential difference reaches a critical point, based on the width of the post and the strength of the Si, the post breaks free of the substrate and pulls in to the ARDEM pattern. Complex dynamics and random processes likely cause some of the posts to lift out of the holes where they pull in to the ARDEM pattern. The post yield at the end of the standard process is <5%.

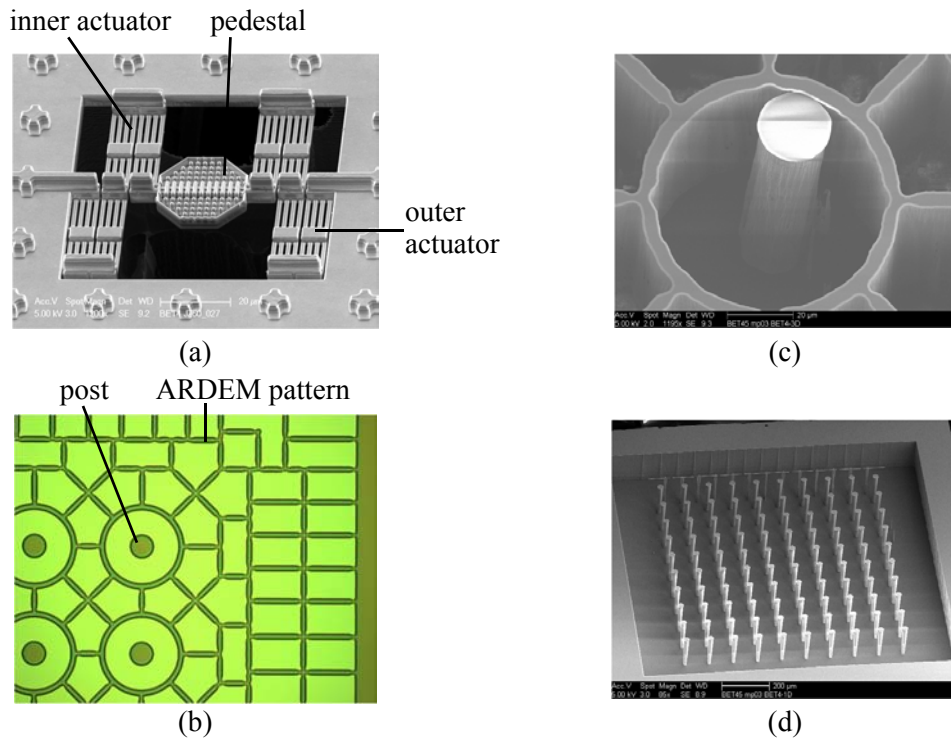
To test the theory that the broken posts are caused by the presence of the ARDEM pattern at the moment the Si breaks through, a modified process concept was applied in which the etch:passivation ratio in the anisotropic step is varied to laterally erode the ARDEM pattern as the etch proceeds vertically. This concept works as shown in Figure 3.23 (d) but the process window is very small and the chip yield for a single etch run is ~20%. The observed failure mode is notching related erosion of the post at the interface with the BOX leading to pillar collapse.

3.4.2 100 μm Pitch Post Etch Fabrication

A type E, 1-D actuator with a 100 μm pitch design is shown in Figure 3.24 (a). The ARDEM pattern in Figure 3.24 (b) is more complicated than the 50 μm design. The pedestal is 25 μm wide and the post is 20 μm wide. The posts of the 100 μm mirror pitch designs fail in the same way as the posts of the 50 μm designs using the standard process (see Figure 3.24 (b)). Changing the etch:passivation ratio

throughout the process led to a higher post yield (see Figure 3.24 (c)) and the process window appears to be larger than at smaller pitches. It is speculated that feature size pushes the lateral ARDE and ARDP phenomena into a wider region of the process space between lateral etching and the ion deflection that leads to notching. The tendency toward notching is observed near the interface of the post Si and the BOX. Detailed experimental investigation of lateral ARDE, ARDP and the coupling with notching is needed to properly design ARDEM features using a two level structure (i.e. post or BOX).

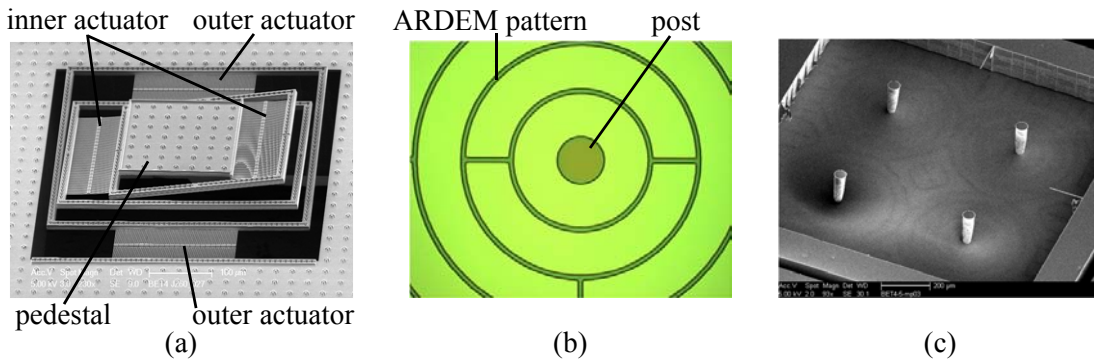
FIGURE 3.24 (a) SEM image of a 100 μm pitch 1-D mirror actuator with a 35 μm wide pedestal. (b) Photograph of the ARDEM pattern for the post of the 100 μm pitch mirror. (c) SEM image of a post broken off during etch due to an electrostatic pull-in failure mode. (d) SEM image of a post array after etch with a variable etch:passivation ratio.



3.4.3 500 μm Pitch Post Etch Fabrication

Figure 3.25 (a) shows a type E, 3-D actuator for 500 μm pitch devices. The pedestal is 175 μm wide and the posts are designed to be 45 μm wide after etch. The ARDEM pattern is a set of concentric rings (see Figure 3.25 (b)) similar to the ARDEM pattern for the mm-scale mirrors shown in Figure 3.11. The standard etch process is used to etch the posts shown in Figure 3.25 (b).

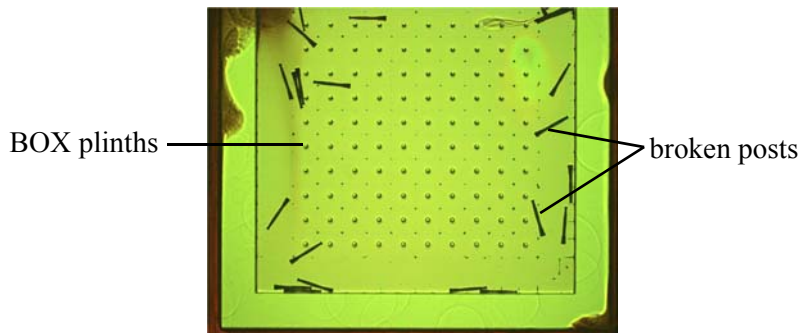
FIGURE 3.25 (a) SEM image of a 500 μm pitch 3-D mirror actuator with a 175 μm wide pedestal. (b) Photograph of the ARDEM pattern around the post. (c) SEM image of a post array after etch.



3.4.4 BHF BOX Removal

The posts of the 50 μm and 100 μm pitch devices do not survive BHF etch (see Figure 3.26). It appears the separation of the posts coupled with the size of the posts' contact with the BOX makes them too weak to withstand the surface tension forces generated by the BHF and the rinsing process. The 500 μm pitch devices do survive the process.

FIGURE 3.26 Photograph of posts broken during BHF BOX removal.

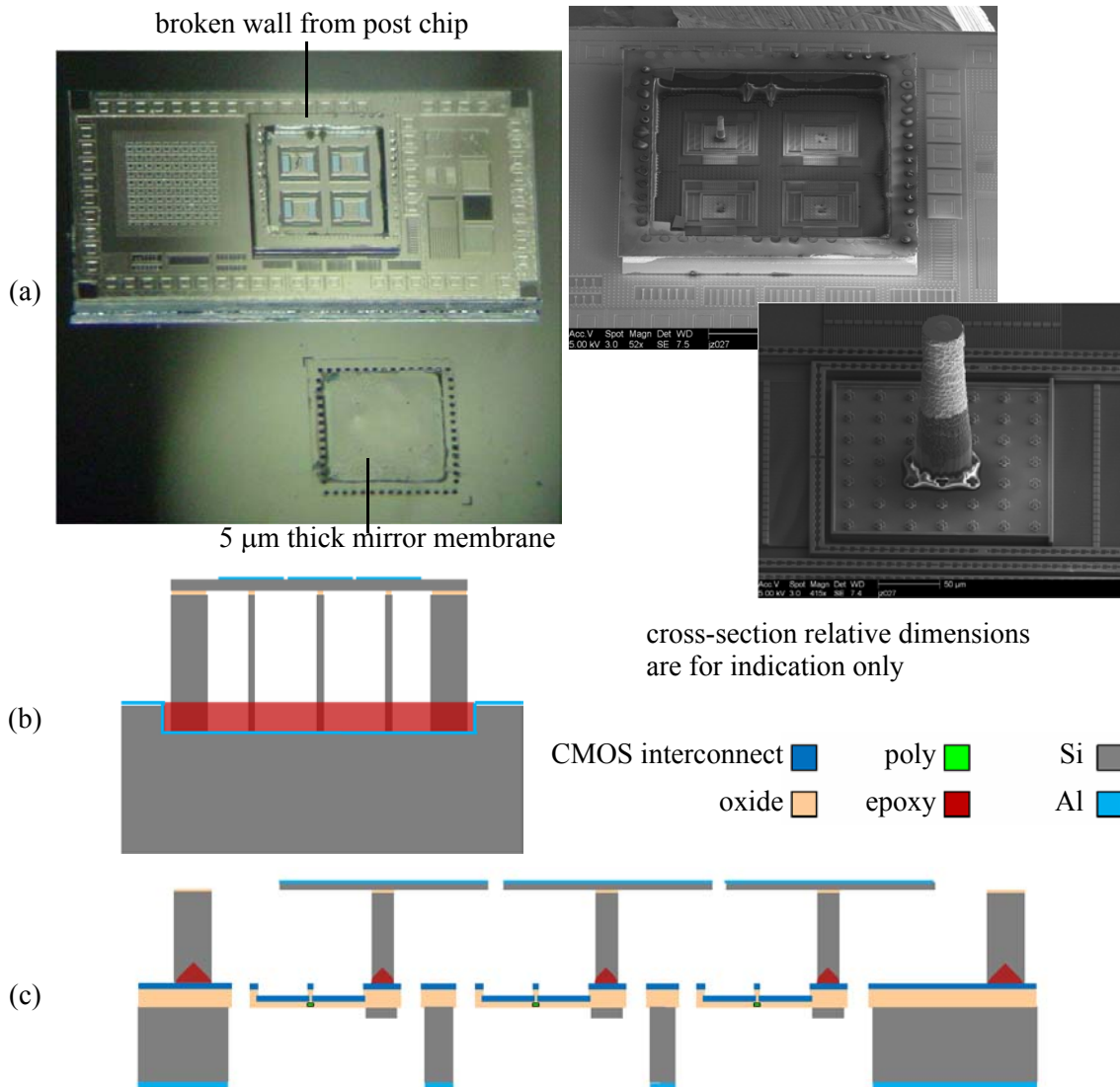


3.4.5 Device Bonding

The 500 μm pitch devices do not survive the SOI-CMOS-MEMS bonding process (see Figure 3.27 (a)). After the preliminary cure of the bonding process the 5 mm thick Si membrane on which the mirrors are formed is bonded to the vacuum diffuser plate and separates from the mirror chip during removal of the SOI-CMOS-MEMS from the device bonder. The reason for this is a change in the SOI-CMOS-MEMS chip concept to include integrated encapsulation of the actuators and mirrors

to prevent fouling. The device concept is shown in cross-sectional schematic in Figure 3.27 (b). The major difference compared to the SOI-CMOS-MEMS bonding concept in Section 3.3.1 is that the wall of the mirror chip is dipped into the epoxy so it is also bonded to the CMOS chip. The effect causing the failure is the wicking of epoxy up the side of the wall and capillary action which pulls the epoxy into the gap between the mirror and the vacuum diffuser plate. This problem can be fixed by returning to a non-integrated wall concept; however, this is a project for a future researcher.

FIGURE 3.27 (a) Photograph of broken SOI mirror membrane and SOI wall adhered to CMOS chip. (b) Modification of the epoxy dip tray to dip both the posts and the wall of the SOI mirror/post chip. (c) Integrated wall device concept to enable actuator and mirror encapsulation.

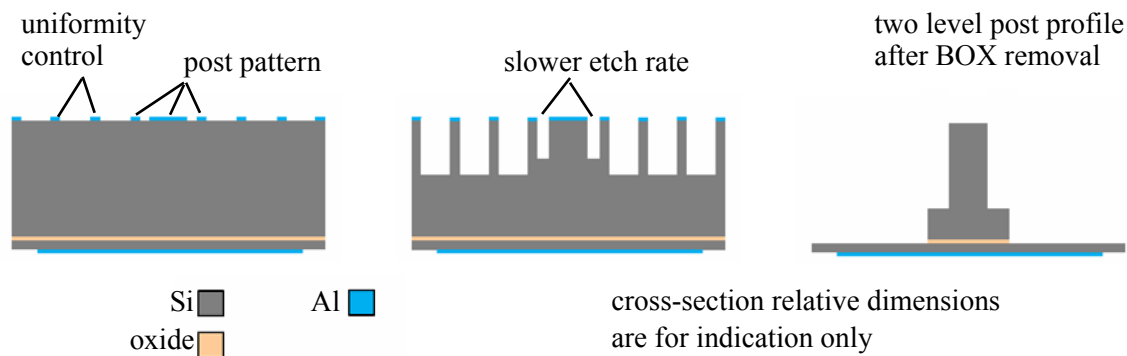


3.4.6 Addressing Post Scaling Issues

The post concept for mm-scale mirrors is that the post will have a uniform transverse cross-section along its length. This concept does not scale as described above for two reasons: 1. as the post density increases the process window between electrostatic pull-in at Si breakthrough and notching decreases to the point that the post yield becomes zero, 2. the surface tension effects during wet BOX removal break the posts off their BOX plinths.

The issue of the post process window can be addressed by using ARDEM to create a two level post as shown schematically in Figure 3.28. The idea is that the transverse cross-section of the post at the interface between the Si and the BOX would be much wider than the free end of the post that bonds to the mirror. The minimum dimension of the pedestal would not be adversely impacted, but the post would be more robust to the notching effect. The surface tension issue destroying the posts can be addressed by moving from a wet process to a vapor phase HF etch. This would provide the additional advantage of eliminating the necessity to protect the Al surface of the mirrors during BOX removal.

FIGURE 3.28 Schematic cross-section of a single mirror with a two level post design and etch concept.



3.5 Fabrication Summary

The SOI-CMOS-MEMS fabrication technology described in this chapter has sufficient process window for producing mm-scale mirror arrays and provides compatibility with a chip mounting process that extends the range of motion of the mirrors. The process window of the post etch decreases as

the scale of the mirror decreases and surface tension issues manifest as the mirror pitch decreases. A post design solution has been suggested to widen the process window of the post etch, but it is necessary to move to a vapor phase BOX removal to eliminate surface tension driven post breakage. The epoxy dipping bonding process has proved to be incompatible with an integrated mirror encapsulation concept and to explore this possibility further requires a new adhesive delivery method or a new bonding approach.

4

Aspect Ratio Dependent Etch Modulation

“It is by going into the abyss that we recover the treasures of life.”

- Joseph Campbell

Aspect ratio dependent etching (ARDE) is an unavoidable fact of life for those applying plasma etch in a fabrication technology. It was first noted by Chin et al. [67] in the etching of submicron Si trenches but has also been observed in the etching of other materials, such as oxide [73] and is typically considered an undesirable effect. It encompasses the decrease in vertical etch rate with increasing aspect ratio (AR) as well as lateral etching and profile effects such as sidewall bowing [67].

It took MEMS researchers to appreciate the benefits the phenomena could bring to a fabricator's tool kit. Kiihamaki et al. [74] demonstrated how ARDE could be used to control depth uniformity and profile across large areas by sub-dividing it into smaller areas that etched at similar rates. Chou and Najafi [75] fabricated curved electrodes by tailoring the mask opening to accentuate ARDE. Both process concepts are exploited in the fabrication of SOI-CMOS-MEMS micromirror arrays. The use of ARDE to control sidewall profiles has also been demonstrated in the literature [69] and is applied here.

Previously, investigators such as Kiihamaki et al. [74] and Chou and Najafi [75] reported their results phenomenologically without detailing the theoretical models by which they generated the masks that were used to exploit ARDE, while researchers, such as Hill et al. [76] modeled microloading and spatial variation in etch rate without including ARDE. This work contributes a detailed exploration of the physical processes driving ARDE phenomena and includes the effect in a model of etch

depth variation across a wafer. In this regard, it advances the application of ARDE in the production of process outcomes that were hitherto impractical to achieve by other means. By accepting the inevitability of the many sources of etch rate variation, its application has become integral to the success of SOI-CMOS-MEMS and its image as an enabling characteristic in MEMS fabrication is reinforced.

This chapter explores the physical mechanism of ARDE for vertical etch rate variation and its inclusion in a framework for a unified model of etch depth variation that comprises spatial variation and pattern-based effects. Lateral ARDE and other effects like bowing and notching have not been modeled, but some preliminary data on their AR dependence are presented. The validity of the theory of ARDE presented in the literature is first established and the theory is then expanded to provide analytic expressions for etch depth given a designed feature width. The name coined for the process control techniques based on the etch depth model is Aspect Ratio Dependent Etch Modulation (ARDEM).

4.1 The Coburn-Winters Model of ARDE

Coburn and Winters [68] postulated a model for ARDE (henceforth, CW model) based on vacuum conductance considerations that related the ratio of the etch rate at the bottom of a structure of depth D and characteristic etch depth d , $ER_{Si}(AR = D/d)$, and the etch rate at the top of the structure $ER_{Si}(0)$ to the ratio of the respective etchant fluxes at these surfaces, $\Gamma(D/d)$ and $\Gamma(0)$. Coburn and Winters surmised that these fluxes would depend on the probability K that a particle passing through the orifice of a structure will reach the bottom of the structure and the probability S that the particle would react with the exposed Si when it reaches the bottom of the structure. They expressed this mathematically as

$$\frac{ER_{Si}(AR = D/d)}{ER_{Si}(0)} = \frac{\Gamma(AR = D/d)}{\Gamma(0)} = \left[1 + S \left(\frac{1}{K} - 1 \right) \right]^{-1}, \quad (4.1)$$

which allows $ER_{Si}(AR = D/d)$ to be expressed as

$$ER_{Si}(AR = D/d) = ER_{Si}(0) \left[1 + S \left(\frac{1}{K} - 1 \right) \right]^{-1}. \quad (4.2)$$

Several investigators have explored independently the effects of pattern shape [77][78], density [79] and AR [73][80] on feature etch rate, but the CW model shows these effects must be combined to form a complete etch model. In the following sections, the validity of this model is considered for the Bosch-type process [64] given in Appendix C.2, expressions for $ER_{Si}(0)$ and K are developed and a value for S is determined experimentally.

4.1.1 Rangelow's Criteria for the Validity of Coburn-Winters Model

Rangelow [81] identified several conditions for the validity of the CW model: 1. The etch rate as a function of aspect ratio $ER_{Si}(AR)$ must depend on surface reaction of neutrals, 2. $ER_{Si}(AR)$ must not depend on ion flux, 3. sidewall etching is negligible and 4. neutral reflection from sidewalls is diffuse. To determine if these conditions are met for the process described here, the etching kinetics, molecular transport mechanism and the relation between the passivation step and the final etch depth must be quantified. This sub-section analyzes these issues and assesses whether Rangelow's criteria are met.

The nature of the process under consideration must be appreciated to assess whether it meets Rangelow's criteria. The time-multiplexed, Bosch-type anisotropic etch process cycle in Appendix C.2 is illustrated in Figure 4.1 and consists of a passivation step of duration τ_p and an etch step of duration τ_e . During the passivation step, a carbon-based inhibitor film is deposited conformally on the surface of the wafer (Figure 4.1 (a)). Before Si begins etching in the etch step, the inhibitor film is removed from horizontal surfaces [82] in time τ_{ep} (Figure 4.1 (b)). The duration of Si etching τ_{eSi} (Figure 4.1 (c)) is the etch step time τ_e minus the time required to remove the inhibitor τ_{ep} (i.e. $\tau_e = \tau_{ep} + \tau_{eSi}$). The depth of Si etched in time τ_{eSi} is D_s . So, there are three possible contributors to an observed change in the rate of hole depth increase: aspect ratio dependent passivation (ARDP), aspect ratio dependent passivation etch and aspect ratio dependent Si etch.

The total Si etch time $\tau = \sum_N \tau_{eSi}$, where N is the total number of cycles. The total etch depth $D = \sum D_s$. The summations are done from the second cycle in the process because the first cycle does not etch Si. This is most likely due to etching of the native oxide and a lower DC bias in the first cycle (see Figure 4.2). The reader should note that the total Si etch time is not the same as the total process time, which is $N(\tau_p + \tau_e)$.

FIGURE 4.1 Conceptual schematic cross-sections of a circular hole of diameter d in a time-multiplexed Bosch-type etch process. (a) Conformal inhibitor polymer coating following passivation cycle of duration τ_p . (b) Inhibitor polymer removed from all horizontal surfaces after time τ_{ep} of etch cycle. (c) Isotropic Si etch for time τ_{eSi} resulting in a depth step $D_s(\tau_{eSi})$.

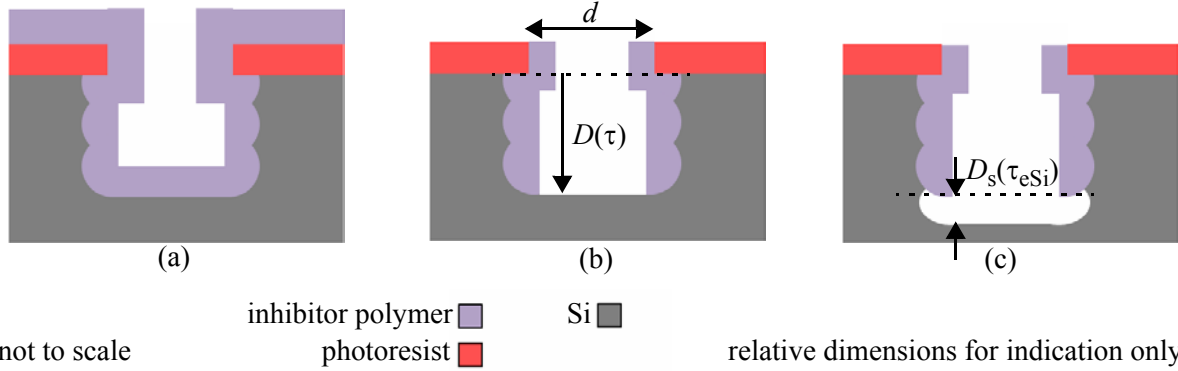
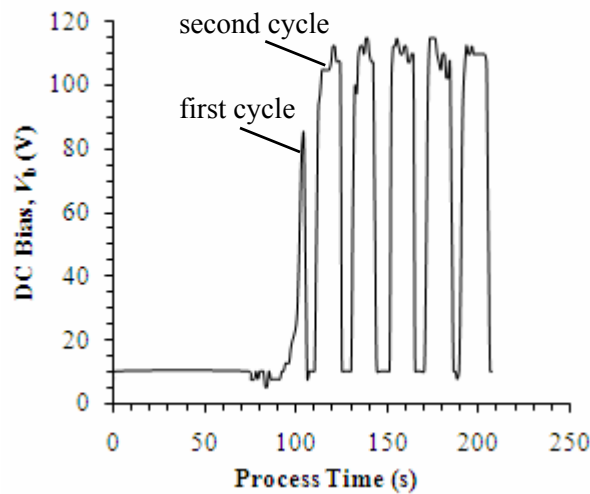


FIGURE 4.2 Graph of DC bias V_b measured on an STS-ASE ICP for the first six cycles of an anisotropic etch process illustrating the distinct difference in V_b for the first cycle of the process.



Adherence to Rangelow's 1st and 2nd criteria can be established using Langmuir kinetics to describe the process, which is an established theory for etch processes [97]. Given only F neutral adsorption, thermal product desorption and ion induced product desorption, the Si etch rate is

$$ER_{\text{Si}} = \frac{c'_{\text{Si}}}{c_{\text{Si}}} \cdot \frac{1}{\frac{1}{K'_d + Y_i K''_i c_{\text{F}^+}} + \frac{4}{K''_a c_{\text{F}}}}, \quad (4.3)$$

where c_{Si} and c'_{Si} are the atomic Si volume and area densities, respectively, in $\text{mol}\cdot\text{m}^{-3}$ and $\text{mol}\cdot\text{m}^{-2}$, c_{F^+} is the F ion density at the sheath edge in $\text{mol}\cdot\text{m}^{-3}$, c_{F} is the neutral F density at the etching surface in $\text{mol}\cdot\text{m}^{-3}$, K'_d is the first-order desorption rate constant in s^{-1} , K''_i is the second order ion-induced desorption rate constant in $\text{m}^3\text{mol}^{-1}\text{s}^{-1}$, K''_a is the second order adsorption rate constant in $\text{m}^3\text{mol}^{-1}\text{s}^{-1}$ and Y_i is the product species yield per incident F^+ . The factor of 4 in the adsorption term in (4.3) reflects the assumption that SiF_4 is the only product species in the reaction. For the purposes of this analysis, this is an acceptable simplification given the accepted range of 70% to 95% of SiF_4 in the product flux [83].

The ionic-desorption limiting case of (4.3) is

$$ER_{\text{Si}}(Y_i K''_i c_{\text{F}^+} \gg K'_d) \approx ER_{\text{Si},\infty} = \frac{c'_{\text{Si}}}{c_{\text{Si}}} \cdot \frac{K''_a c_{\text{F}}}{4}. \quad (4.4)$$

The neutral-flux limiting case of (4.3) is

$$ER_{\text{Si}}(Y_i K''_i c_{\text{F}^+} \ll K'_d) \approx ER_{\text{Si},0} = \frac{c'_{\text{Si}}}{c_{\text{Si}}} \cdot \frac{K'_d K''_a c_{\text{F}}}{K''_a c_{\text{F}} + 4K'_d}. \quad (4.5)$$

The ratio of (4.4) and (4.5) is

$$\chi = \frac{E_{\text{Si},\infty}}{E_{\text{Si},0}} = 1 + \frac{K''_a c_{\text{F}}}{4K'_d}. \quad (4.6)$$

The experimental determination of χ is described in Section 4.4.3 and is used to determine whether the reaction is limited by product desorption or F adsorption through the relation

$$K'_d = \frac{1}{4(\chi - 1)} K''_a c_{\text{F}}. \quad (4.7)$$

Adherence to the 3rd and 4th criteria is assessed by reviewing the cross-sectional profiles of holes etched in Si. If sidewall etching is significant the sidewalls would not be vertical as lateral etching would occur at a finite rate compared to vertical etching. By a similar argument, if neutral reflection is not diffuse, neutrals would be reflected in preferential directions and higher etch rates would be observed in these directions, if the process is neutral-flux limited. Cross-sections of etched holes are presented in Section 4.4 for the assessment of these criteria.

4.1.2 Molecular Flow Regime of the Etch Process

The molecular transport regime for the etch process depends on the Knudsen number K_n (mean free path λ / characteristic dimension d) for the participating molecular species. Assuming the plasma in the etching feature is predominantly a mixture of neutral F and SF₆ [84], the mean free path of F is

$$\lambda_F = \frac{k_B T}{\pi p} \left[\sqrt{2} x_F \delta_F^2 + x_{SF_6} \frac{(\delta_F + \delta_{SF_6})^2}{4} \left(1 + \frac{m_{SF_6}}{m_F} \right)^{0.5} \right]^{-1} \quad (4.8)$$

where T is the plasma temperature in K, p is the pressure in Pa, x_F and x_{SF_6} are the F and SF₆ mole fractions, respectively, δ_F and δ_{SF_6} are the molecular diameters of F and SF₆ in m, respectively, m_F and m_{SF_6} are the molecular masses of F and SF₆ in kg, respectively and k_B is Boltzmann's constant [85]. An analogous expression exists for the mean free path of SF₆.

Typical values of $x_F = 0.05$ have been reported for inductively coupled SF₆ plasmas under these conditions [84]. The plasma temperature is estimated to be $T = 350$ K based on analyses from Piejak et al [86]. From the literature $\delta_F = 0.10$ nm [87] and $\delta_{SF_6} = 0.55$ nm [88], so (4.8) evaluates to 1.6 mm for F for the anisotropic process given in Appendix C.2. The analogous expression for SF₆ yields a mean free path of 1.5 mm. Etched MEMS features and most of the structures in this study have characteristic lengths under these values and are in the free molecular flow regime (i.e. $K_n > 1$). In this regime, expressions for K have been provided by Dushman [85] and Clausing [89] and are

detailed in Section 4.1.3 and Section 4.1.4, respectively. Larger openings are in the transition region (i.e. $0.01 < K_n < 1$) so an error is expected when using Dushman's or Clausing's expression for K .

4.1.3 Dushman's Vacuum Conductance Factor

Dushman [85] derived an approximation K_D to the correction factor for the vacuum conductance of a tube (see Figure 4.4) from the ratio of the conductance of an orifice of area A_o and perimeter H_o to the conductance of a tube aligned along the z -axis with transverse cross-sectional area $A(z)$ and perimeter $H(z)$, such that for structures with depth D ,

$$\frac{1}{K_D} - 1 = \frac{3}{16} A_o \int_0^D \frac{H(z)}{A(z)^2} dz. \quad (4.9)$$

For a regular cylinder of diameter d_o (4.9) evaluates to

$$\frac{1}{K_D} - 1 = \frac{3}{4} \cdot \frac{D}{d_o}. \quad (4.10)$$

Equation (4.10) is used to define $d = d_o$ as the characteristic dimension, such that for any structure

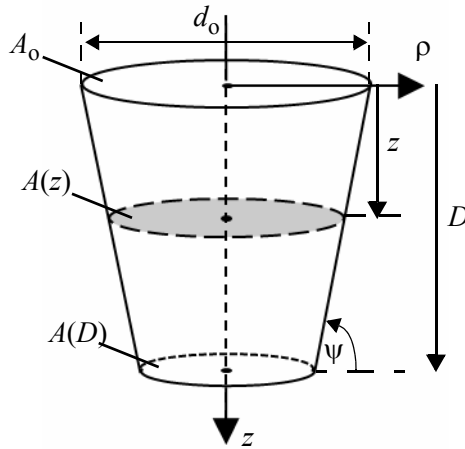
$$d = \frac{4D}{A_o} \left(\int_0^D \frac{H(z)}{A(z)^2} dz \right)^{-1}. \quad (4.11)$$

For structures with constant perimeter and cross-sectional area along their depth (4.11) is simply

$$d = \frac{4A_o}{H_o}. \quad (4.12)$$

The utility of (4.11) and (4.12) in sizing ARDEM masks is discussed in Section 4.3.5 and the extension of (4.10) to tapered structures is briefly speculated upon in Section 4.3.3.

FIGURE 4.3 Tube with orifice area A_0 and depth D aligned along the z -axis, with a perimeter $H(z)$ and cross-sectional area $A(z)$ that vary with the distance z along the tube axis due to the sidewall taper angle.



Substituting (4.10) into (4.2) leads to the compact relation between the Si etch rate at the bottom of an arbitrarily shaped hole with $AR = D/d$

$$ER_{Si}(AR = D/d) = ER_{Si}(0) \left[1 + \frac{3}{4} S \frac{D}{d} \right]^{-1}. \quad (4.13)$$

4.1.4 Clausing's Vacuum Conductance Factor

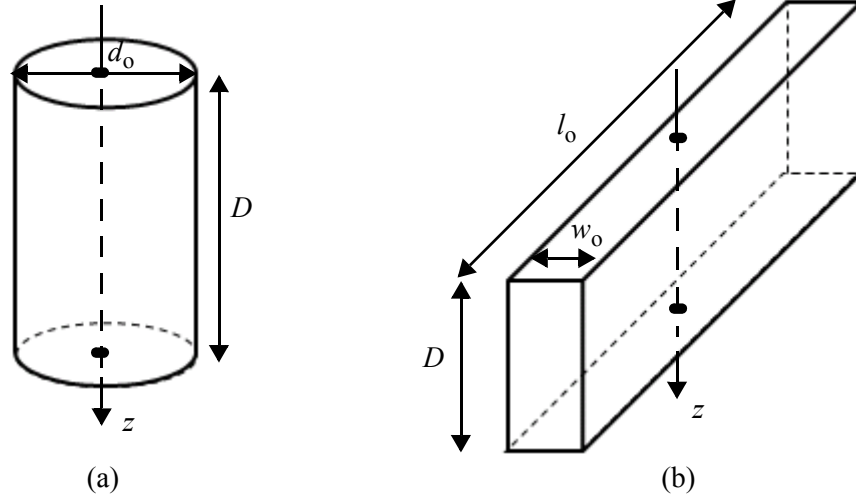
Dushman [85] noted that the expression he derived was only an approximation and that Clausing [89] had performed an analysis that led to a more exact correction factor K_C which is simply applied in (4.2) such that

$$ER_{Si}(AR = D/d) = ER_{Si}(0) \left[1 + S \left(\frac{1}{K_C} - 1 \right) \right]^{-1}. \quad (4.14)$$

However, Clausing's derivation is mathematically complex and limited to two special cases: 1. the regular cylinder (see Figure 4.4 (a)) and 2. the narrow trench (see Figure 4.4 (b)), with the constraints that the slit width $w \ll l$, the slit length and that the depth $D \ll l$. The limitations of Clausing's model cede to Dushman the greater applicability and tractability required by MEMS designers, however in order to determine what is lost in accuracy by Dushman's model, a head-to-head comparison of the

two models is needed. To do this, the calculation of Clausing's factor is reiterated to facilitate its appreciation, as the original is in German, and the depth prediction compared to experimental data is presented for both K_C and K_D .

FIGURE 4.4 The two vacuum conductance correction factor cases considered by Clausing: (a) a regular cylinder and (b) a rectangular slit. In each case, the structure has a constant cross-sectional area, a depth D and is aligned along the z -axis.



Clausing derived his correction factor from detailed considerations of the geometric trajectory of a particle through a structure in the free molecular flow regime given a randomized and hence uniform angular distribution. For the regular cylinder,

$$K_C = \frac{4(1-2\xi)}{3d_0^2D} \left[\frac{d_0^3}{2} + \left(D^2 - \frac{d_0^2}{2} \right) \sqrt{D^2 + d_0^2} - D^3 \right] + \xi + \frac{2(1-\xi)}{d_0^2} \left[D^2 - D \sqrt{D^2 + d_0^2} + \frac{d_0^2}{2} \right], \quad (4.15)$$

where ξ is a constant factor given by

$$\xi = \frac{\left[(D-\tilde{z}) \sqrt{(D-\tilde{z})^2 + d_0^2} - (D-\tilde{z})^2 \right] - \left[\tilde{z} \sqrt{\tilde{z}^2 + d_0^2} - \tilde{z}^2 \right]}{D\tilde{z}^2 - (2\tilde{z}-D)(\tilde{z}^2 + d_0^2) - \frac{D(D-\tilde{z})^2 - (2(D-\tilde{z})-D)((D-\tilde{z})^2 + d_0^2)}{\sqrt{\tilde{z}^2 + d_0^2}} - \frac{D(D-\tilde{z})^2 - (2(D-\tilde{z})-D)((D-\tilde{z})^2 + d_0^2)}{\sqrt{(D-\tilde{z})^2 + d_0^2}}} \quad (4.16)$$

which is evaluated at

$$\tilde{z} = \frac{D}{1 + \frac{3D}{d_o\sqrt{7}}}. \quad (4.17)$$

For the rectangular trench with $w \ll l$ and $D \ll l$,

$$K_C = \xi \left[1 - \frac{w_o}{D} \ln \left(\frac{D + \sqrt{D^2 + w_o^2}}{w_o} \right) \right] + \frac{1}{2w_o} (\sqrt{D^2 + w_o^2} - D) + \frac{w_o}{2D} \ln \left(\frac{D + \sqrt{D^2 + w_o^2}}{w_o} \right), \quad (4.18)$$

where

$$\xi = \frac{\left[(D - \tilde{z}) - \sqrt{(D - \tilde{z})^2 + w_o^2} \right] - \left[\tilde{z} - \sqrt{\tilde{z}^2 + w_o^2} \right]}{\left[2(D - \tilde{z}) - 2\sqrt{(D - \tilde{z})^2 + w_o^2} + \frac{D(D - \tilde{z})}{\sqrt{(D - \tilde{z})^2 + w_o^2}} \right] - \left[2\tilde{z} - 2\sqrt{\tilde{z}^2 + w_o^2} + \frac{D\tilde{z}}{\sqrt{\tilde{z}^2 + w_o^2}} \right]}, \quad (4.19)$$

which, for $w \leq D$, is evaluated at

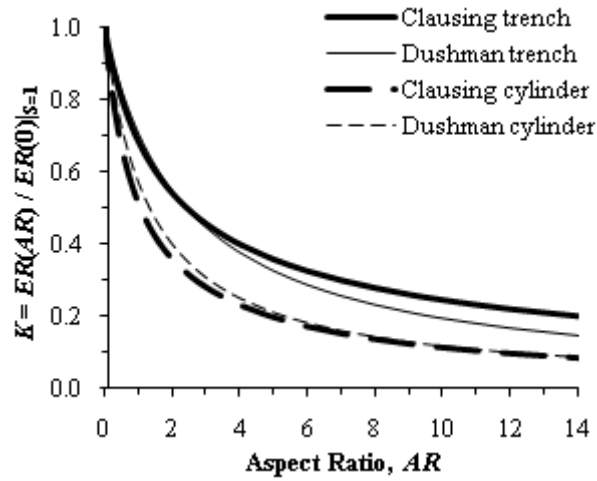
$$\tilde{z} = \frac{w_o D \ln \left(\frac{D}{w_o} \right)}{2D + w_o \ln \left(\frac{D}{w_o} \right)} \quad (4.20)$$

and for $w > D$ is evaluated at $\tilde{z} = 0$.

4.1.5 Comparison of Dushman and Clausing Correction Factors

Figure 4.5 shows a graph comparing the Dushman and Clausing vacuum conductance correction factors for a cylinder and a rectangular trench with constant cross-section. The trench length $l:w$ width ratio is 10:1 for the demonstration. The graph indicates that rectangular trenches have a higher etch rate than cylinders over all AR .

FIGURE 4.5 Comparison of the Dushman and Clausing vacuum conductance correction factors for regular and tapered cylinders and trenches as a function of AR . The comparison is made using the etch rate $ER(AR)$ normalized to the surface etch rate $ER(0)$ with a reaction probability of $S = 0.25$.



4.2 Modeling Surface Etch Rate

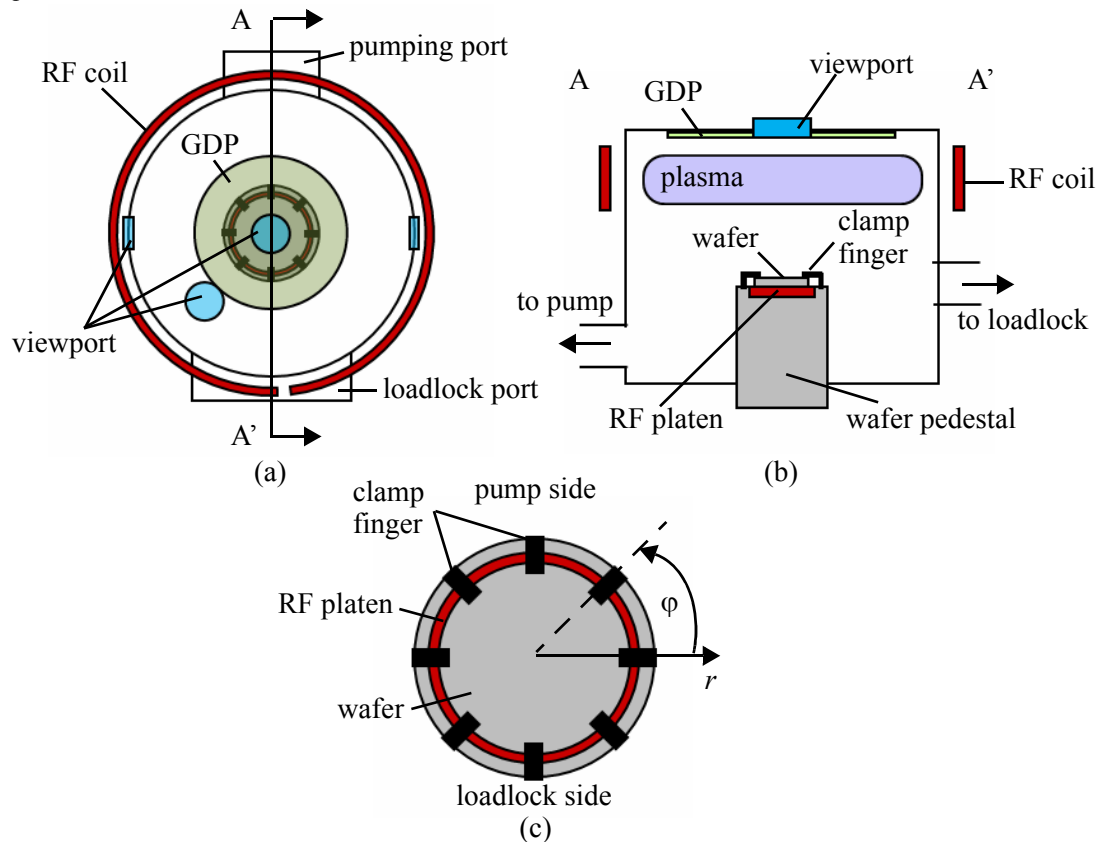
The other element of (4.2) needed to form a model for the etch rate of a feature is $ER_{Si}(0)$, the etch rate at the surface of the feature. The etch rate at any position in a single wafer, plasma etch chamber is subject to several sources of variation such as the shape of the plasma, the non-uniform distributions of etchants, products, ions and neutrals in the chamber and the transport of these species to and from the etching surface. These distributions are overlaid on a wafer map comprising areas of etchable material of varying pattern density and feature size. In this section, these factors of etch rate variation are defined and developed.

4.2.1 Spatial Variation

The CMU STS-ASE plasma chamber is shown schematically in Figure 4.6. Radial and azimuthal variations in an ICP plasma etch chamber are caused by the shape and position of the RF coil, discontinuities that occur at the edge of the wafer pedestal and asymmetry in the shape of the chamber due to the location of load locks, pumping ports, gas distribution plates (GDP) or inlets, clamp fingers (in the case of mechanical clamps) etc.[82][65].

For this work, the radial position r of a feature is defined from the geometric center of the RF platen (see Figure 4.6 (c)) to the geometric center of the feature. It is assumed that the geometric center of the platen coincides with the geometric center of the wafer. In practice this is not the case because there is always some misalignment in the wafer placement, so this assumption introduces a small error. The azimuthal position ϕ is defined in the counterclockwise direction from the reference line between the geometric center of the RF platen and the 3 o'clock position, with respect to the pumping port at the 12 o'clock position (see Figure 4.6 (c)).

FIGURE 4.6 (a) Cross-sectional and (b) plan view schematics of a STS-ASE chamber illustrating sources of spatial non-uniformity. (c) Close-up plan view of the wafer on the platen showing the definition of radial and azimuthal positions.



Spatial variation in etch rate is characterized experimentally because of its sensitivity to chamber type, chamber hardware and process conditions. The nature of the problem defies a general analytic description so in Section 4.4.4 spatial variation models are fitted to empirical data. In contrast to prior

work that used test structures on a square grid [90], spatial variation is explored with radially symmetric distributions of test structures in this work.

4.2.2 Pattern-based Variation

There are two types of pattern-based factors that are considered in this work: macroload M_p and microload μ_p . They relate to phenomena that arise due to the pattern-driven variations in etchant concentration, the quantity of etching material consuming the etchant, the spatially non-uniform consumption of etchant species and the limitations imposed by the finite transport properties of species in the plasma. Mogab [91] identified the loading effect as the impact of the overall quantity of etching material exposed to the plasma in a batch reactor on the etch rate of those materials. Mogab's effect has since been called macroloading as it refers to a global reduction in etch rate and to contrast it with microloading, which refers to variations in etch rate caused by local pattern density variation whose range is on the order of microns to millimeters [92]. Microloading is strong enough that it has been applied to perform structure formation [93] in a manner similar to the way ARDE is used in this work.

Macroloading and microloading have been shown, in the steady state, to follow the diffusion equation [94] and thus depend on the shape of the plasma, the geometric relation between the RF coil and wafer, the mutual diffusivity of the species in the plasma and the transport regime in which it operates, among other factors. In the single wafer STS-ASE, M_p is the proportion of the Si wafer surface area that is exposed to the plasma. While the impact of macroloading can be calculated on a global level [91] its analytic expression for specific features on a wafer is not known to the author. For this reason, macroloading is characterized empirically in this work by fitting a function to the experimental data.

Microloading, on the other hand, was shown by Hill et al. [76] to be analytically tractable when treated as a spatial filtering problem. Hill et al.'s approach, which is applied in this work, is to use the diffusion equation to determine an impulse response function $W(r, \varphi)$ for the decrease in etchant con-

centration $\Delta c_F = c_{Fb} - c_F$ due to exposed etching material, where c_{Fb} is the F concentration in the bulk plasma. Hill et al. perform a convolution of the impulse response with a pattern function $L(r, \varphi)$ representing the physical layout of the features on the wafer ($L = 0$ for photoresist and $L = 1$ for exposed Si) such that

$$\mu_p(r, \varphi) = W(r, \varphi) \otimes L(r, \varphi). \quad (4.21)$$

Alternatively, these functions can be expressed equivalently in Cartesian coordinates as

$$\mu_p(x, y) = W(x, y) \otimes L(x, y). \quad (4.22)$$

In this form, μ_p is computed efficiently using Fourier transforms. μ_p is interpreted as the reduction in the etch rate at (r, φ) due to the consumption of F by the surrounding exposed Si.

4.2.3 Microloading Weighting Function

Hill et al. [76] proposed a weighting function of the form

$$W = \frac{a}{\rho}, \quad (4.23)$$

based on the impulse response of the diffusion equation assuming a point sink of etchant species in a hemispheric region, where ρ is the radial distance from the point under consideration and a is a scaling parameter incorporating the reaction rate of F with Si and the diffusion constant for F in the plasma. Hill's weighting function is not wholly compatible with the F concentration reduction Δc_F at a point on the surface of an etching wafer due to other exposed Si regions because it contains the physical paradox of an infinite concentration gradient at the point and the contribution of a load of infinite weight from the point itself. So, (4.23) poses the problem of how to treat the area around a point in a discretized numeric computation of μ_p for realistic $L(r, \varphi)$.

For an axially symmetric diffusion problem, the gradient of W with respect to ρ must be zero at the point under consideration and W must be bounded. Jensen et al. [94] derived an approximate analytic

solution c_F of this diffusion problem that exhibited these properties; however, Jensen's solution does not provide a tractable analytic form, which is part of the goal of this work. To determine the validity of Hill's function it is compared with a normalized FEA solution for Δc_F along the surface of a wafer due to a central area of exposed etching Si of radius r_{\min} . The FEA was performed using Comsol Multiphysics[®] (3.5a with Matlab[®]). The script for the simulation is given in Appendix D.1. The parameter r_{\min} represents the minimum lithography feature size for a given technology. The wafer surface is modeled as one boundary of an axially symmetric region (see Figure 4.7) with dimensionless coordinates $\zeta = z/r_{\min}$ and $\eta = \rho/r_{\min}$. The extent of the region is determined by the thickness of the stagnation region above the wafer t_{stag} and the wafer pedestal radius R_p . The constant c_F boundary condition at $\eta = R_p/r_{\min}$ is based on the work of Kiehlbauch et al. [95] and Economou et al. [96] who showed through simulation that neutral transport to and from the wafer is primarily axial in a high gas flow system with a showerhead-type GDP, like the STS-ASE. The effect of etching is incorporated in the simulation by a temperature dependent Si-F etch transport parameter $h' = r_{\min}h$ that is derived in Section 5.8.5. Detailed analysis of the plasma conditions is done in Section 5.2 to determine the diffusivity value D_{F-SF_6} and bulk F concentration c_{Fb} for the simulation. In this simulation, $D_{F-SF_6} = 0.5 \text{ m}^2\text{s}^{-1}$, $c_{Fb} = 55 \times 10^{-6} \text{ mol}\cdot\text{m}^{-3}$, the etching temperature is equal to the platen temperature given in Appendix C.2, $h = 710 \text{ m}^{-1}$ and $r_{\min} = 1 \text{ }\mu\text{m}$.

The value of t_{stag} is not known directly for the STS-ASE chamber. However, an inference was made based on the observations that $c_F(0,0)$ is strongly dependent on t_{stag} and bottoms out above a certain exposed Si area and that ER_{Si} is linearly dependent on c_F . The concentration observations are demonstrated by raw $c_F(\rho,0)$ solutions shown for a range of central exposed Si areas of radius r in Figure 4.8 (a) and (b) for $t_{\text{stag}} = 1 \text{ mm}$ and 50 mm , respectively. In the experimental data, which is presented in Section 4.4 the variation in etch rate with M_p drops by a factor of 2 from $M_p \sim 0\%$ load to $M_p \sim 100\%$ load, suggesting c_F also dropped by a similar factor. For that to occur, given the FEA results, $t_{\text{stag}} \approx 1.5 \text{ mm}$.

FIGURE 4.7 Axially symmetric region for FEA simulation of the impulse response of F reduction Δc_F at the surface of a wafer due to a central area of exposed Si of radius r .

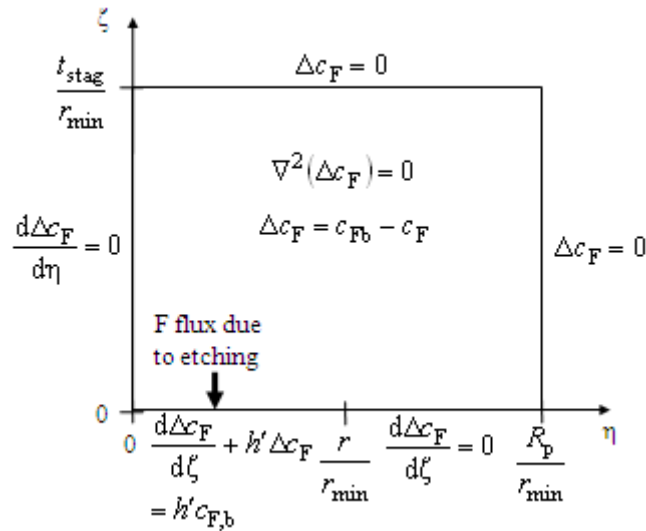
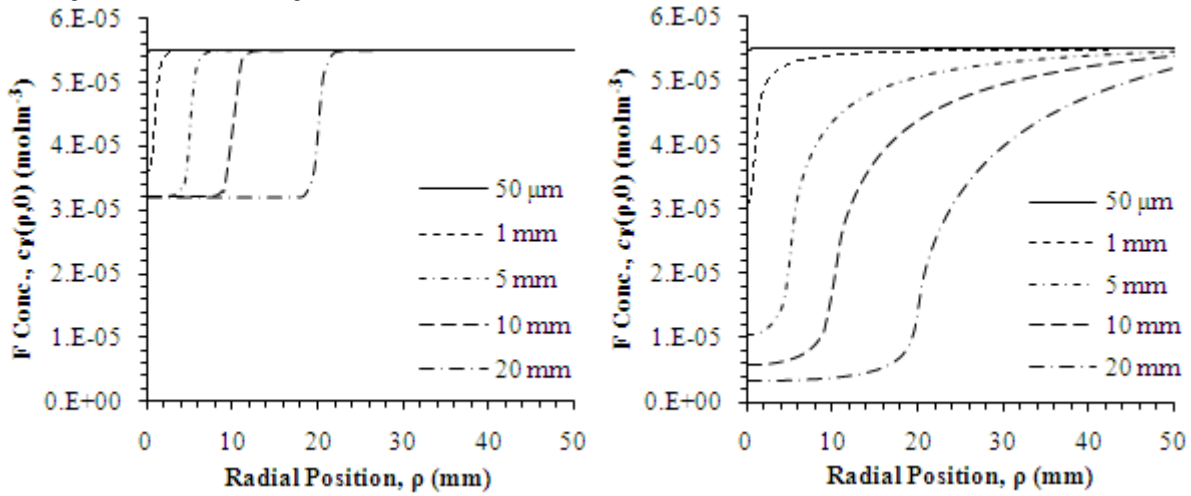
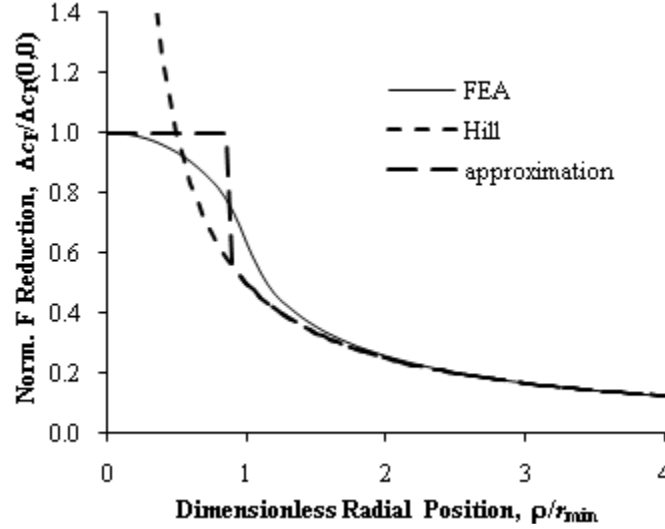


FIGURE 4.8 Raw $c_F(\rho,0)$ solutions for the region and boundary conditions shown in Figure 4.7 for (a) $t_{stag} = 1$ mm and (b) $t_{stag} = 50$ mm and various sizes of central exposed Si area.



The normalized FEA solution, a scaled version of Hill's function and an approximate solution for use in numeric computations are shown in Figure 4.9. For $\rho > 3r_{min}$, Hill's function matches the FEA solution to 1% or better. The error in Hill's function rapidly increases below $3r_{min}$, but is reduced in the approximate weighting function by equating it to a constant value. The value is selected based on that value of ρ for which the numeric integration of the error between the FEA solution and Hill's function is a minimum. This condition occurs at $\rho = 0.85r_{min}$.

FIGURE 4.9 Graph of Δc_F normalized to the F reduction at the center of the region $\Delta c_F(0,0)$ as a function of dimensionless distance from the center of the area of exposed etching Si . The FEA solution is compared to Hill's function [76] and an approximate solution used for numerically computing microloading.



4.3 Unified Etch Depth Model

ARDE, spatial variation, macroloading and microloading contribute to the variation in ER_{Si} . In this section these factors are combined in a unified etch model to predict etch depth at a given etch time for features of arbitrary geometry. The etch rate at a point (r, φ) or (x,y) is given by

$$ER_{Si}(r, \varphi) = f(L, r, \varphi, M_p, \mu_p, AR) \quad (4.24)$$

or

$$ER_{Si}(x, y) = f(L, x, y, M_p, \mu_p, AR), \quad (4.25)$$

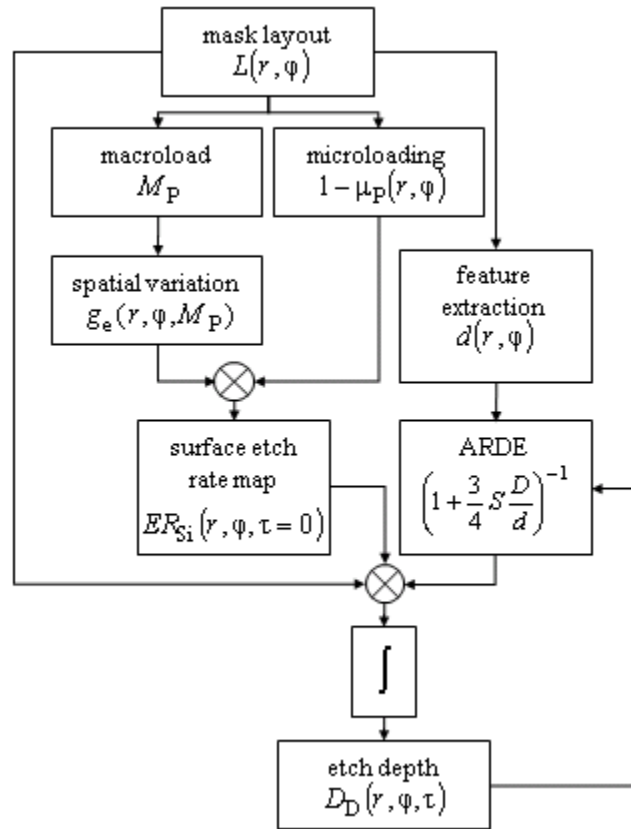
depending on which coordinate system is most convenient. In most cases, this is the Cartesian system because layouts are encoded in this form.

4.3.1 Etch Depth Model Structure

The depth model has the structure shown in Figure 4.10 and is implemented practically according to the flow chart. A given layout pattern $L(r, \varphi)$ is analyzed to obtain M_p, μ_p and the characteristic

dimensions d for the exposed Si features. The characteristic dimension is used to determine the ARDE effect on each feature. This part of the model is initialized with a depth $D = t_{\text{mask}}$, the mask thickness. M_P is applied in the fitted function for spatial and macroload variation and multiplied with the microloading map $\mu_P(r, \varphi)$ to produce the surface etch rate map $ER_{\text{Si}}(r, \varphi, \tau = 0)$ which is multiplied with the ARDE map and $L(r, \varphi)$ and integrated to output the depth D as a function of etch time. The depth map is fed back to the ARDE block for the next iteration of the model.

FIGURE 4.10 Practical implementation of the etch depth model structure comprising spatial and pattern-based sources of etch rate variation assuming constant cross-section with time.



4.3.2 Etch Depth Model

The various components of (4.24) are separated as independent functions to re-express (4.24) as

$$ER_{\text{Si}}(r, \theta\varphi) = L(r, \varphi) \cdot g_e(r, \theta, M_P) \cdot (1 - \mu_P) \left[1 + S \left(\frac{1}{K} - 1 \right) \right]^{-1} \quad (4.26)$$

where $g_e(r, \theta, M_p)$ is a fitted function combining all spatial and macroloading effects and K is either Dushman's (K_D) or Clausing's (K_C) vacuum conductance correction factor. Applying K_D in (4.26) gives

$$ER_{Si,D}(r, \varphi) = L(r, \varphi) \cdot g_e(r, \varphi, M_p) \cdot (1 - \mu_p) \left[1 + \frac{3}{4} S \frac{D}{d} \right]^{-1}. \quad (4.27)$$

When compared to (4.14), (4.26) implies that the surface etch rate is

$$ER_{Si}(r, \varphi, \tau = 0) = L(r, \varphi) g_e(r, \theta, M_p) (1 - \mu_p). \quad (4.28)$$

Equation (4.27) is integrated with respect to time

$$D_D(r, \varphi, \tau) = \int ER_{Si,D}(r, \varphi) d\tau = \int L g_e (1 - \mu_p) \left[1 + \frac{3}{4} S \frac{D}{d} \right]^{-1} d\tau \quad (4.29)$$

with the condition that in practical situations a feature in an etch process is formed by a mask of finite t_{mask} , which is the initial depth of the structure. With the initial condition, (4.29) becomes

$$D_D(r, \varphi, \tau) = \left[\frac{8d}{3S} g_e (1 - \mu_p) \tau + \left(\frac{4d}{3S} + t_{\text{mask}} \right)^2 \right]^{0.5} - \left(\frac{4d}{3S} + t_{\text{mask}} \right). \quad (4.30)$$

The depth model using Dushman's conductance correction factor predicts that larger features will suffer less ARDE but this is offset by greater microloading. The value of d at which the maximum depth occurs depends on the shape of the feature. This is addressed in greater detail in Section 4.4 when microdonut, circular hole and trench test structures are analyzed and compared.

4.3.3 Model Extension to Tapered Profiles

An advantage of the use of Dushman's parameter over Clausing's factor is that ARDE of tapered structures, as observed by Yeom et al. [80], can be determined by evaluating the integral in (4.11) and substituting the result into (4.27). For the simple case of the tapered cylinder shown in Figure 4.3 with orifice diameter d_o and sidewall angle ψ , the etch rate at depth z is

$$ER_{Si,D} = Lg_e(1 - \mu_p) \left[1 + \frac{3}{4} S \frac{z}{d_o} \frac{\left(1 - \frac{z}{d_o \tan \psi}\right)}{\left(1 - \frac{2z}{d_o \tan \psi}\right)^2} \right]^{-1}. \quad (4.31)$$

Similarly, for a tapered rectangular trench with orifice dimensions w_o and l_o and sidewall angle ψ the etch rate at depth z is

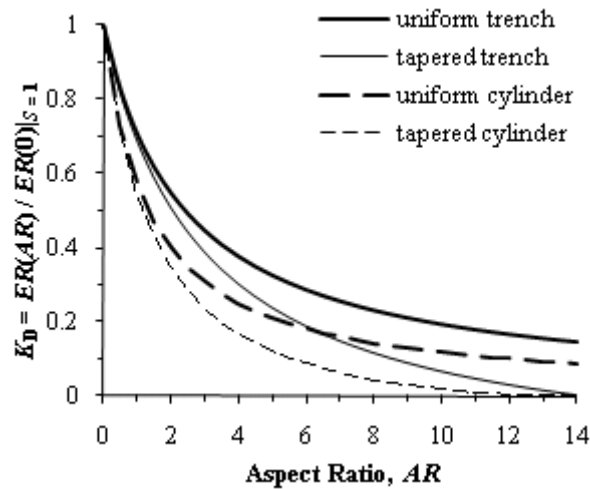
$$ER_{Si,D} = Lg_e(1 - \mu_p) \left[1 + \frac{3}{8} S \frac{z(w_o + l_o)}{w_o l_o} \frac{\left(1 - \frac{2z}{(w_o + l_o) \tan \psi}\right)}{\left(1 - \frac{2z}{w_o \tan \psi}\right) \left(1 - \frac{2z}{l_o \tan \psi}\right)} \right]^{-1}. \quad (4.32)$$

These expressions are amenable to numerical integration to determine the depth $D(\tau)$.

4.3.4 Comparison of Model with Dushman and Clausing Factors

A comparison of the conductance correction factors of regular and tapered cylinders and rectangular trenches is shown in Figure 4.11. A cut-off in etch rate is predicted at different AR for trenches and cylinders.

FIGURE 4.11 Comparison of the Dushman vacuum conductance correction factors for regular and tapered cylinders and trenches. The comparison is made using the etch rate $ER(AR)$ normalized to the surface etch rate $ER(0)$ with a reaction probability of $S = 1$.



4.3.5 Practical Considerations for ARDEM Mask-making

The ultimate goal in modeling etch rate and particularly ARDE is to apply it in the formation of structures, especially CMOS backside structures, and to better control uniformity over large open areas of Si of irregular shape. Kiihamäki et al. [74] demonstrated how uniformity could be improved by subdividing large areas into rectangular sections of equal characteristic dimension and Chou et al. [75] demonstrated curved surface electrodes etched with a single mask made of features of different widths. The most elegant way to achieve this is to invert the problem and compute a mask pattern, subject to suitable constraints, that leads to a desired 3-D structure shape in Si. Unfortunately, such a development must wait for a future student. The necessary definition of the structure shape in 3-D, the parsing of that definition into a form to which the constraints could be applied, the definition of the constraints, the appropriate form of the model to facilitate inversion and the framework for these operations has yet to be created. However, it is still possible to perform these operations for a narrow set of constraints and simple 3-D structures with vertical sidewalls.

The first necessary constraint is the maximum feature width. This will typically be determined by the shape of the final 3-D structure, or by the existing device features, like the frontside structures in the case of CMOS-MEMS. As large a width as possible leads to higher etch rates and larger final height differences. However, several adverse structure effects, like retrograde profiles and trenching have been observed for large feature sizes [63] and this may set a natural upper limit on the feature size but is still to be determined. The width of the walls separating adjacent rectangular areas should be made as narrow as possible and is an additional factor in determining maximum feature width.

In the example shown in Figure 4.12, a mesa of Si is to be formed under the pedestal of a CMOS-MEMS electrothermal actuator. The smallest gap between the frontside CMOS-MEMS pedestal and the anchor defines the maximum feature width. Rectangular sections are used. There is no constraint on shape in principle, however, shapes with acute inner angles experience larger ARDE based on

observation, but have not been characterized and so have been avoided. Large areas are divided into rectangular sections with a $l_o:w_o$ ratio $b = 10$ because at this value of b , the characteristic dimension,

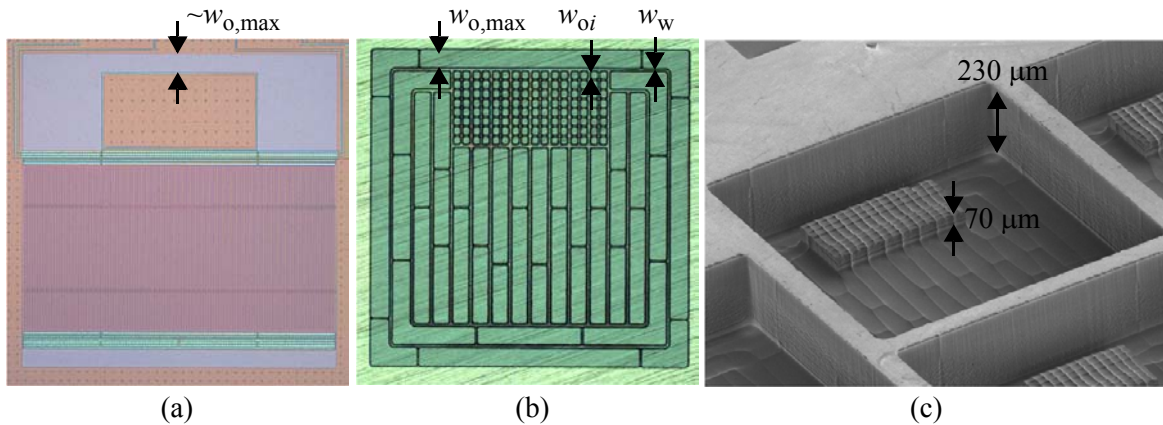
$$d = \frac{4A_o}{H_o} = \frac{2b}{1+b}w_o \quad (4.33)$$

reaches $\sim 92\%$ of its maximum value of $d = 2w$. Effectively, further increases in l , and therefore b , do not lead to a significant etch rate increase. The entire area to be etched to the deepest level is now covered in rectangles. An integer multiple of features must fit in the area to be covered and it may be necessary to trim the width to make them fit. If the width must be trimmed on some rectangles and not others, the length can be adjusted to compensate using the relation

$$l_{oj} = w_{oj} \left(\frac{l_{oi}w_{omax}}{l_{oi} + w_{omax}} \right) \left(w_{oj} - \frac{l_{oi}w_{omax}}{l_{oi} + w_{omax}} \right)^{-1} \quad (4.34)$$

A final consideration on the sizing is the need for the sacrificial mask to remain suspended when it is undercut. If it falls onto the Si in the etching area it will cause defects. The need to stabilize the structure requires adjustment of the wall positions at the ends of the rectangular sections. The positioning for stability has not been characterized and requires further work to determine the optimal condition.

FIGURE 4.12 A simple example of ARDE photomask generation for the two level structure of a mesa in an etch pit. (a) Optical microscope image of CMOS as received from the foundry. (b) Optical microscope image of the ARDEM pattern formed on the backside of the CMOS. (c) Mesa structure in etch pit after backside DRIE.



Once the deepest level structures have been sized, the time τ to reach the desired maximum depth D_{\max} is calculated. At this point the other levels are sized to achieve the required step heights. The maximum step is limited to the time dependent ARDEM range R_D

$$R_D = D_{\max} - \left[\frac{8w_{o,\min}}{3S} g_e (1 - \mu_P) \tau + \left(\frac{4w_{o,\min}}{3S} + t_{\text{mask}} \right)^2 \right]^{0.5} - \left(\frac{4w_{o,\min}}{3S} + t_{\text{mask}} \right), \quad (4.35)$$

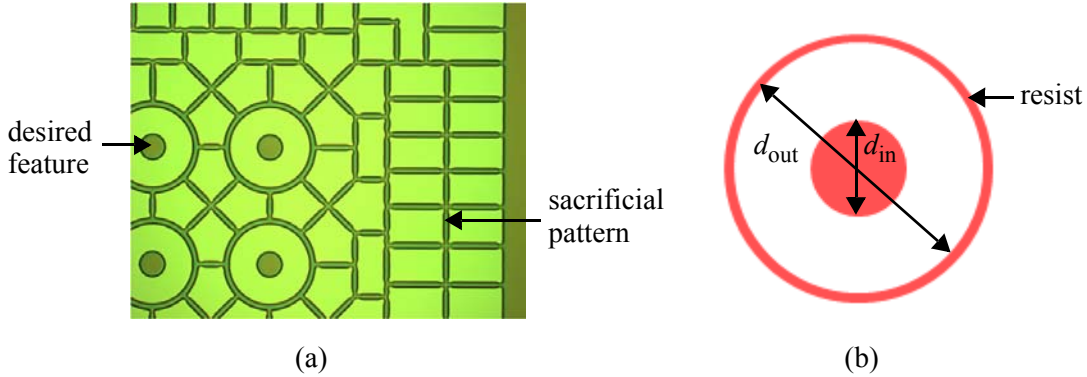
which is constrained by the minimum photolithography dimension $w_{o,\min}$ for a square hole. If the desired step height is less than R_D then it is achievable using ARDEM processing. The correct sizing of the i^{th} depth level is w_{oi} . It has been determined graphically and through the use of the FindRoot function in Mathematica^{®6}. If the desired step height is greater than R_D then $w_{o,\max}$ must be increased, or another method must be found.

The concept of characteristic dimension has also been useful in the enhancement of depth uniformity for irregular features. The optical microscope image in Figure 4.13 shows the ARDEM pattern on the handle side of a SOI wafer. The desired feature is a post that is formed by etching all the Si of the handle layer of thickness t_p with the buried oxide (BOX) layer of thickness t_{BOX} as an etch stop. Although the ARDEM features cannot be rectangular due to the shape of the post, (4.12) can be used to size the irregular features to have equivalent characteristic dimensions. Again, this would benefit from automation, but for a small number of shapes is still amenable to hand calculation. Difficulty arises with shapes such as the annulus, for which a perimeter is not well defined. This type of shape has been treated as though the perimeter was the sum of the circumference of the inner and out edges, as shown in Figure 4.13 (b), such that,

$$d = \frac{4A_o}{H_o} = d_{\text{out}} - d_{\text{in}}. \quad (4.36)$$

This approximation is currently necessary and works sufficiently in practice, but a future researcher may do well to develop the theory to cover such types of shape.

FIGURE 4.13 (a) Example of an irregularly shaped area with ARDEM pattern generated by sizing the features so they have equivalent characteristic dimensions. (b) Schematic of an annulus extracted as a detail from the ARDEM pattern shown in (a).



The tightness of the equivalence on characteristic dimensions d_i is, to first order, dependent on the uniformity requirement. For example, to prevent breakthrough of the BOX it is necessary to have the normalized depth range, or uniformity U of the etch process meet the constraint

$$U < \left(\frac{t_{wh}}{t_{BOX} S_{Si-BOX}} - 0.5 \right)^{-1}, \quad (4.37)$$

where S_{Si-BOX} is the selectivity of Si over BOX given by

$$S_{Si-BOX} = \frac{ER_{Si}}{ER_{box}}. \quad (4.38)$$

For $l_p = 500 \mu\text{m}$, $t_{BOX} = 0.5 \mu\text{m}$ and $S_{Si-BOX} = 180$, $U < 20\%$ (lower U indicates a more uniform process, i.e. lower range). However, in practice, issues such as ion focussing, BOX uniformity and BOX integrity (i.e. pinholes, density variation etc.) reduce the constraint on U , requiring a more uniform process and a tighter range of d_i .

4.4 Etch Process Characterization

This section describes the characterization of the etch process. It comprises a detailed description of the test structures used and the analysis of the components of their etch rate variation. The adherence

of the process to Rangelow's criteria from Section 4.1.1 is demonstrated. Experimental data is presented for the test structures and the analytic depth model in (4.30) and a model based on the numeric integration of (4.14) are fit to the data using the reaction probability as the fitting parameter. S_D' is used for the fitted value of S based on Dushman's correction factor to distinguish it from the actual value and similarly, S_C' is the fitted value of S based on Clausing's correction factor.

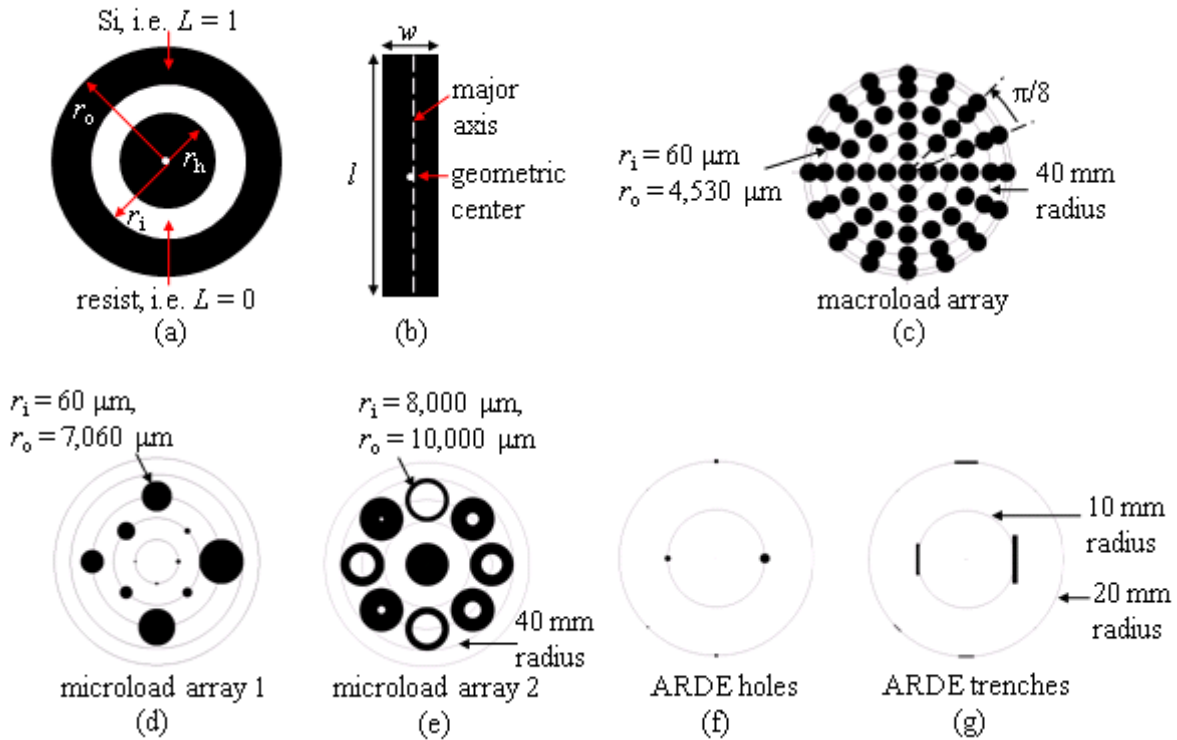
4.4.1 Test Structures for Etch Model Parameter Extraction

Microdonut and trench test structures (Figure 4.14 (a) and (b)) in various patterns (Figure 4.14 (c) to (g)) were used for process regime analyses and characterization. The test patterns are grouped in terms of the process characteristic they are designed to capture: spatial variation, microloading or ARDE. Test features are arrayed on the perimeter of concentric circles with radii of 0 mm, 10 mm, 20 mm, 30 mm, 40 mm and 47.5 mm and separated azimuthally by angular intervals that decrease from $\pi/2$ to a minimum of $\pi/8$ with increasing distance from the wafer center (Figure 4.14 (c)). The use of regularly spaced, identical test features is taken from Taylor et al. [90], however, Taylor's test features were arrayed on a rectangular grid, as opposed to the radially symmetric patterns reported here.

The minimum distance between microdonut centers is 10 mm on spatial and ARDE test patterns. For microloading test patterns, a minimum distance of 20 mm is used in an attempt to avoid loading interactions between adjacent test structures. These distances are based on first order calculations of depletion radius [94], $40 \mu\text{m} < r_d < 15 \text{ mm}$, derived from a calculated sheath thickness of $t_s \sim 2 \text{ mm}$ [65],[97] and a mean free path of neutral F $\lambda_F \sim 1.5 \text{ mm}$. It is shown, for the particular equipment configuration used in this study, that this separation of the microloading test structures is insufficient to prevent perturbation of the etch rate by the adjacent structures.

FIGURE 4.14 (a) Microdonut test structure used for characterization of the CMU, Bosch-type DRIE process. The radius of the central hole $r_h = 50 \mu\text{m}$ for spatial variation and microloading characterization, but varies for ARDE characterization. The inner radius of the annulus is r_i and the outer radius is r_o . (b) ARDE trench test structures of length l and width w with $l = 10w$ in all cases. (c) Wafer-scale macroload array test pattern. $r_h = 50 \mu\text{m}$, $r_i = 60 \mu\text{m}$ and r_o varies to achieve a given macroload. (d) Microload array 1 in which $r_i = 60 \mu\text{m}$ for all microdonuts and r_o varies by site. (e) Microload array 2 in which r_i varies by site and $r_o = 10,000 \mu\text{m}$ for all microdonuts. (f) ARDE test structures with no annulus. r_h varies by site. (g) ARDE trenches with the trench longitudinal axis aligned along the tangent to concentric circles of 10 mm and 20 mm radius.

relative dimensions for indication only



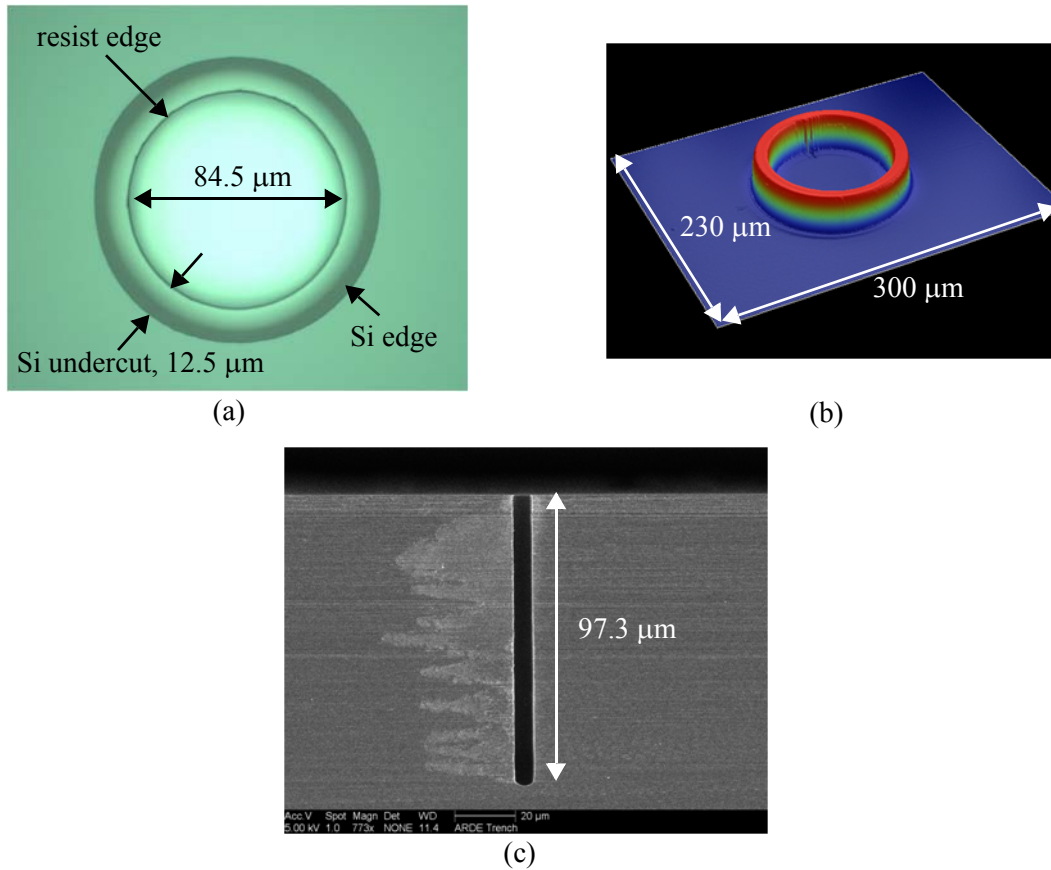
The radius r_h of the central hole in the donut is maintained at $50 \mu\text{m}$ for all tests, except for ARDE test patterns, and was selected as a compromise between minimizing ARDE and microloading and maintaining a constant ARDE impact across all structures. By increasing the difference between the radii of the outer and inner edges of the annulus, r_o and r_i respectively, for all sites on the wafer (see Figure 4.14 (c)), the macroloading is varied such that $0.01 < M_p < 0.9999$. $r_o - r_i$ varies on a site-by-site basis for microload characterization (see Figure 4.14 (d) and (e)). The annulus is not used in ARDE tests, for which the central hole radius r_h varies by site for holes within a 20 mm radius (see Figure 4.14 (f)). Trench test structures are used only for ARDE characterization and each has a $l:w$

ratio of 10. The major axis of each trench structure is aligned along a tangent to the perimeter of the circle on which it is located (see Figure 4.14 (g)). The trench depth is measured at the geometric center of the trench.

100 mm diameter, n-doped, <100> Si wafers were used for the study. Each wafer was coated with hexamethyldisilazane (HMDS) and AZ4210 photoresist (mfg. Clariant) at a spin rate of 4000 rpm for 30 s and softbaked at 90 °C for 30 min. The resist thickness was $2.50 \pm 0.02 \mu\text{m}$ measured using a KLA Tencor P15 profilometer. An AZ4210-coated condition wafer was etched for 10 min using the conditions in Appendix C.2 prior to each test wafer in an attempt to ensure consistent chamber conditions for each test. Three wafers were etched at each test condition to capture run-to-run variation.

Hole diameters and undercuts were measured optically using an Olympus MX80 microscope prior to resist strip (ex. Figure 4.15 (a)). After resist strip, etch depths were measured using a Veeco WYKO NT3300 white-light interferometer (ex. Figure 4.15 (b)). Due to signal loss, structures with $AR > 6$ cannot be measured using interferometry. For donut holes and trenches that could not be measured using interferometry, the trenches were cut with a dicing saw and measured using a scanning electron microscope (SEM) (ex. Figure 4.15 (c)).

FIGURE 4.15 (a) Optical microscope image showing the undercut of the resist mask on a 84.5 μm diameter ARDE test hole. (b) 3-D rendering of a white-light interferometric scan of a 50 μm radius microdonut hole after photoresist strip. (c) Scanning electron microscope image of the cross-section of a 6 μm wide trench.



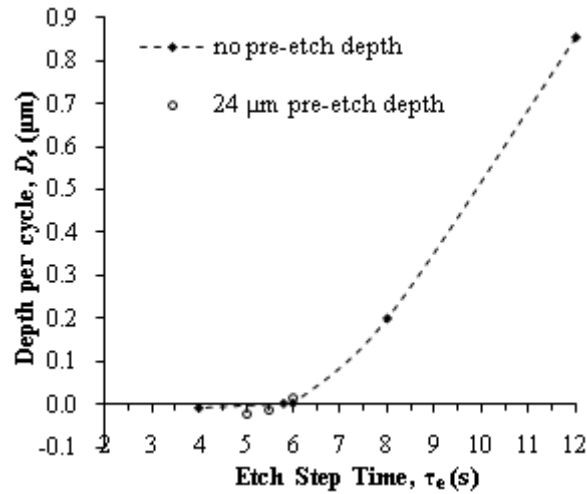
4.4.2 Si Etch Time Stability

The etch depth per cycle D_s is not constant throughout the process due to ARDE, but the contribution of variation in τ_{eSi} to ARDE is unknown. This is important to know, because if τ_{eSi} varies with depth then it must be incorporated into the model and the simple CW model is invalid. The variation in τ_{eSi} is established for circular, resist-masked holes by fixing N and τ_p and reducing τ_e from 12 s, which is the standard etch step time, to the point at which $\tau_e = \tau_{ep}$. At that value of τ_e , Si does not etch and below that value polymer has a net deposition rate on horizontal surfaces. The value of τ_e for which there is no net Si etch or net inhibitor deposition is here called the "cross-over" point between deposition and etching. The test to establish the cross-over point was performed on ARDE wafers. Three wafers each were processed with a constant passivation step time τ_p and number of cycles $N = 30$ but a

range of values of τ_e . The test was done on unetched wafers with a starting depth $D = 0$ to establish the cross-over point. The test was repeated for a small sample of etch:passivation ratios around the previously determined cross-over point on wafers with a pre-etched depth $D \approx 24 \mu\text{m}$. The depths after processing were measured using a combination of profilometry and white light interferometry.

The graph in Figure 4.16 shows the cross-over occurs at ~ 5.5 s of the etch step. Therefore, for the 12 s etch step, the Si etch duration is 6.5 s, which is consistent across all holes. The cross-over point is ~ 5.6 s on the pre-etched wafers. To first order, ARDE is not impacted significantly by aspect ratio dependent passivation (ARDP), so the total Si etch time $\tau = (N-1)\tau_{e\text{Si}}$. This does not mean that ARDP does not exist as this can also be achieved if ARDP is accompanied by a commensurate decrease in the etch rate of the inhibitor on horizontal surfaces, i.e. the inhibitor also suffers from ARDE. The reader should note the etch rate is non-linear during the Si etch portion of the etch step, which is apparent in Figure 4.16, so a constant etch rate over $\tau_{e\text{Si}}$ is an approximation.

FIGURE 4.16 Graph of etch depth per cycle D_s vs. etch step time τ_e for a fixed passivation step time $\tau_p = 8$ s. The negative value at 4 s represents a polymer film that was measured on the silicon surface in the mask openings. The smoothed dashed line is for indication only.



Given $\tau_{e\text{Si}} = 6.5$ s, the average Si etch rate is $130 \text{ nm}\cdot\text{s}^{-1}$ (or $7.9 \mu\text{m}\cdot\text{min}^{-1}$). During the last 1.5 s of the passivation etch interval τ_{ep} , approximately 8 nm of passivation is etched, giving an inhibitor etch

rate on the order of $5 \text{ nm}\cdot\text{s}^{-1}$. At this rate, the total passivation thickness at the start of the etch step is $\sim 30 \text{ nm}$, requiring a passivation deposition rate of $\sim 4 \text{ nm}\cdot\text{s}^{-1}$.

4.4.3 Etch Reaction Kinetics Regime

Rangelow's 1st and 2nd criteria for the validity of the CW model depends on the reaction kinetics of the etching of Si by F. Section 4.1.1 defines a means by which the relative magnitude of the ionic, adsorption and desorption components of the process are determined. The regime of the reaction kinetics was explored using ARDE test wafers that were etched for 5 mins using only the etch step conditions from Appendix C.2 with decreasing values of platen power from 12 W to 0 W to modify the energy of ion bombardment. Prior to photoresist strip, the horizontal Si undercut of the photoresist mask was measured through the mask (see Figure 4.15 (a)) with an accuracy of $\pm 0.25 \mu\text{m}$ using an Olympus MX80 microscope with a 100x objective. Following photoresist strip, the depth was measured using a WYKO NT3300 white light interferometer with an accuracy of $\pm 0.1 \mu\text{m}$.

The etch rate variation with platen power over a range of feature sizes, shown in Figure 4.17, indicates that ion induced desorption becomes negligible at $V_b = 3 \text{ V}$ (0 W platen power), while at $V_b = 150 \text{ V}$ (12 W platen power) the ion induced desorption is saturated. This demonstrates that the process meets Rangelow's 2nd criteria. From (4.3), when the ionic desorption contribution is negligible, the horizontal and vertical etch rates, $ER_{\text{Si,h}}$ and $ER_{\text{Si,v}}$, respectively, should be equal, but significant anisotropy $ER_{\text{Si,h}}/ER_{\text{Si,v}}$ is observed for all hole dimensions over the bias voltage space investigated, as shown in Figure 4.18. The most likely explanation for the observed amount of residual anisotropy at 0 W platen power is neutral shadowing [100]. An investigation of that effect is beyond the scope of this paper but would be useful to understand for better modeling of isotropic Si etch processes and their dependence on feature dimensions.

FIGURE 4.17 Graph of the change in etch depth for holes of varying radius over a range of bias voltages V_b , measured on ARDE wafers etched for 5 min using only the etch step conditions shown in Appendix C.2. The smoothed lines are for indication only.

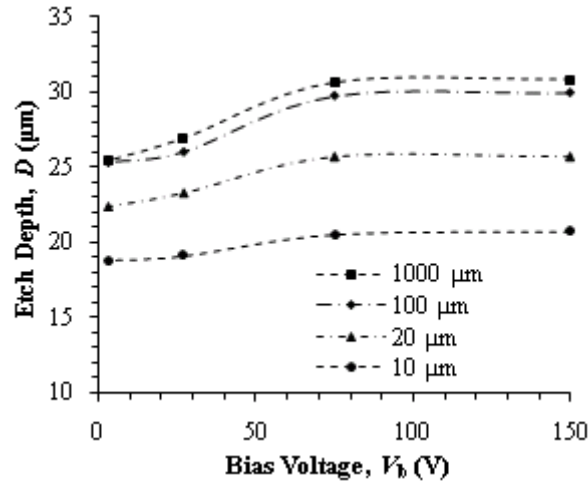
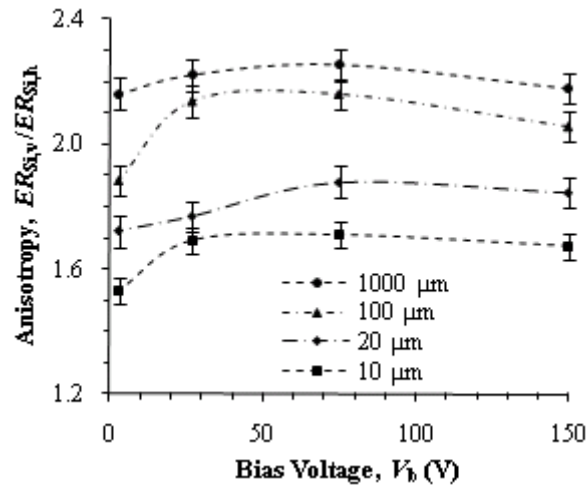


FIGURE 4.18 Graph of the change in the anisotropy (vertical etch rate, $ER_{Si,v}$ / horizontal etch rate, $ER_{Si,h}$) of the etch process for holes of varying radius. The smoothed lines are for indication only. The error in anisotropy of ± 0.05 arises from the low resolution of the microscope used to make the horizontal etch distance measurement.



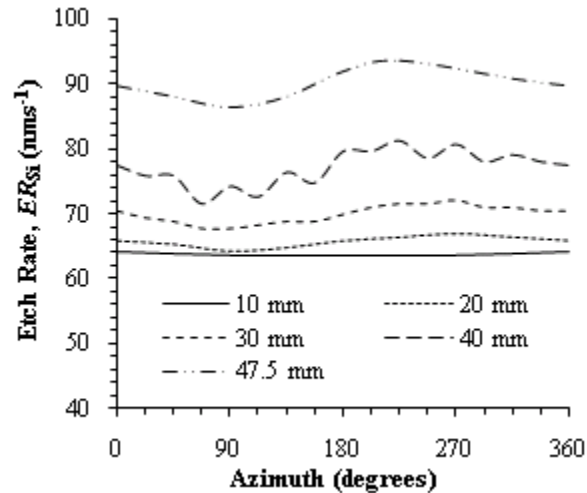
The ratio χ of etch rates at 150 V bias is determined from the experimental data to be ~ 1.2 for holes greater than 1200 μm diameter, for which ARDE effects are small. Entering this value of χ into (4.7) yields $K_d' \approx 1.25K_a''c_F$, which means that etching of Si by F under the process conditions in Appendix C.2 occurs in a neutral-flux-limited regime, thus satisfying Rangelow's 1st criteria. The reader should note that this doesn't imply the time-multiplexed process has the same platen power dependence because the inhibitor removal is likely proceeding in an ion-flux limited regime.

The observed anisotropy of the time-multiplexed process (see Figure 4.15 (c)) and the approximate thickness of the sidewall passivation inhibitor calculated in Section 4.4.2 indicates that the rate of adsorption/reaction of neutral F with the sidewall inhibitor is negligible compared to F neutral adsorption/reaction with Si at the bottom of the hole. The lack of sidewall attack shows that the process satisfies Rangelow's 3rd criteria, while the absence of effects such as trenching and bowing indicate that the 4th criteria is also satisfied.

4.4.4 Macroloads and Spatial Characterization

Azimuthal variation is < 2% within a radius of 30 mm, as shown in Figure 4.19, and is neglected from the model as the test structures lie within this radius. Azimuthal variation outside this distance is driven exclusively by the mechanical clamp fingers and is therefore peculiar to the CMU process kit and can be eliminated by electrostatic clamping. Azimuthal variation can be modeled using a sinusoid in situations where the pattern extends beyond a 20 mm radius.

FIGURE 4.19 Azimuthal Si etch rate variation for test structures on a number of circles concentric with the RF platen in an STS-ASE chamber with mechanical clamp.



The wafer center etch rate variation with M_p for a 50 μm radius hole, is shown in Figure 4.20. Least-squares regression (LSR) is used to fit the 2nd order polynomial $ER_{Si,c} = 37M_p^2 - 112M_p + 140$ (in $\text{nm}\cdot\text{s}^{-1}$) to the observed etch rate variation. The curvature of the etch rate variation with radial position depends on M_p (see Figure 4.21). A 3rd order polynomial was

fitted to the radial etch rate variation, normalized to $ER_{Si,c}$, for each value of M_P , with $R_c^2 > 0.98$, in all cases. The cubic term coefficients are extracted and modeled as a linear function of M_P to obtain $ER_{Si}/ER_{Si,c} = (3400M_P + 1340)r^3 - 60r^2 + r + 1$ (r in m). Together, the macroloading and radial variation gives

$$g_e(r, \theta, M_P) = [37M_P^2 - 112M_P + 140][(3400M_P + 1340)r^3 - 60r^2 + r + 1]. \quad (4.39)$$

FIGURE 4.20 Variation in wafer center etch rate $ER_{Si,c}$ with Si macroload M_P for a central $50 \mu\text{m}$ radius hole. LSR was used to fit the function $ER_{Si,c} = 37M_P^2 - 112M_P + 140$ in $\text{nm}\cdot\text{s}^{-1}$ to the measured data. The solid line represents the fitted function.

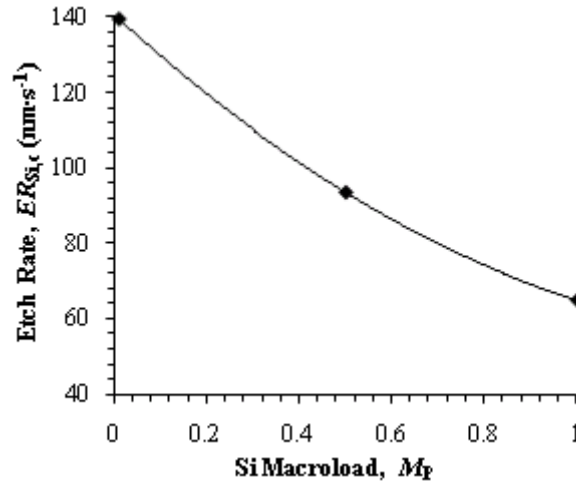
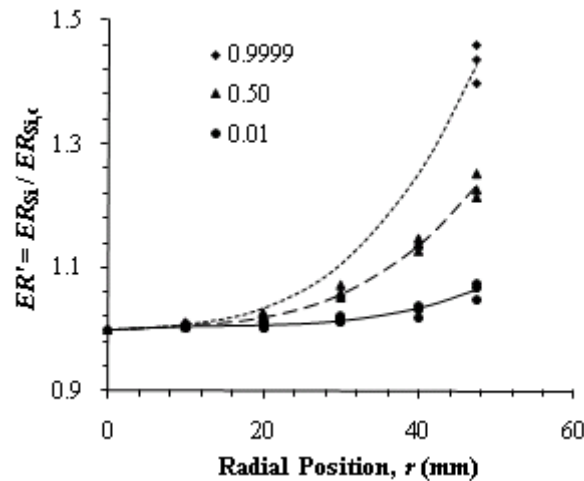


FIGURE 4.21 Radial etch rate variation, normalized to wafer center etch rate, $ER_{Si}/ER_{Si,c}$, for a range of Si macroloads. The solid markers represent the raw data for each microdonut on the perimeter of the circle at a given radius so the spread of points represents azimuthal variation. The lines in the graph represent the LSR fitted function $ER_{Si}/ER_{Si,c} = (3400M_P + 1340)r^3 - 60r^2 + r + 1$ (r in m).



4.4.5 Microloading Characterization

The scaling parameter of the spatial filter must be determined to implement the depth model. By design, the shape of the microdonut leads to a simple form for the microloading μ_P at its center. For a sufficiently isolated single microdonut feature of the kind shown in Figure 4.14, assuming (4.23), the convolution in (4.21) reduces to an integral in the local microdonut coordinates (ρ, ϕ) with a simple solution at the center of the microdonut:

$$\mu_{P,\text{donut}}(0, 0) = \int_0^{2\pi} \int_0^{\infty} L(\rho, \phi) W(\rho, \phi) \rho d\rho d\phi = 2\pi a r_h + 2\pi a (r_o - r_i) = \mu_{P,\text{hole}} + \mu_{P,\text{ann}}. \quad (4.40)$$

The first term in (4.40) represents the self-loading of the donut hole and the second term represents the loading of the center of the donut hole by the annulus. The etch rate at the center of the microdonut is

$$ER_{Si}(0, 0) = (1 - \mu_{P,\text{hole}} + \mu_{P,\text{ann}}) ER_{\text{unloaded}}, \quad (4.41)$$

which can be re-expressed as

$$ER_{Si}(0, 0) = ER_{Si,\text{hole}} - \mu_{P,\text{ann}} ER_{\text{unloaded}}, \quad (4.42)$$

where

$$ER_{Si,\text{hole}} = (1 - \mu_{P,\text{hole}}) ER_{\text{unloaded}}. \quad (4.43)$$

In practical terms, it is not possible to determine the unloaded etch rate ER_{unloaded} because a structure of finite size must be used to measure the depth at any point. Normalizing (4.42) by $ER_{Si,\text{hole}}$ gives

$$\frac{ER_{Si}(0, 0)}{ER_{Si,\text{hole}}} = 1 - 2\pi a (r_o - r_i) \frac{ER_{\text{unloaded}}}{ER_{Si,\text{hole}}}. \quad (4.44)$$

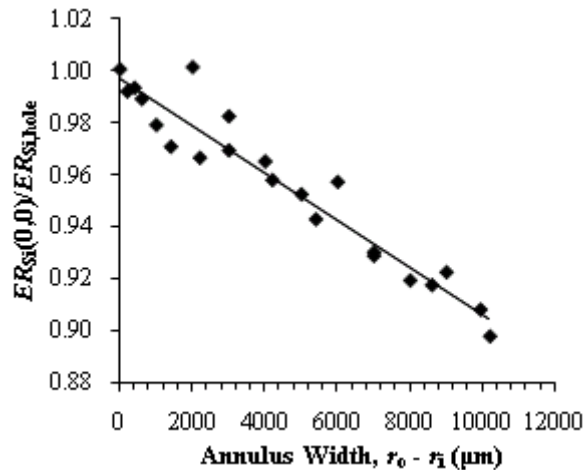
As the radius of the hole decreases, $ER_{Si,\text{hole}}$ approaches ER_{unloaded} and

$$\frac{ER_{Si}(0,0)}{ER_{Si,hole}} \approx 1 - 2\pi a(r_o - r_i) \quad (4.45)$$

which is the linear form used to determine empirically the value of a by varying the width of the annulus of the microdonut.

Two sets of microloading test structures were used to extract a . In the first set, $r_i = 60 \mu\text{m}$ and $200 \mu\text{m} \leq r_o \leq 10,200 \mu\text{m}$ (see Figure 4.14 (d)). In the second set, $60 \mu\text{m} \leq r_i \leq 8,000 \mu\text{m}$ and $r_o = 10,000 \mu\text{m}$ (see Figure 4.14 (e)). The data for both sets of structures are shown in Figure 4.22. LSR is used to fit the line $ER_{Si}(0,0)/ER_{Si,hole} \approx 1.0 - 9.1(r_o - r_i)$ ($r_o - r_i$ in m), with $R_c^2 = 0.93$, from which the value $a = 1.4 \text{ m}^{-1}$ was extracted. The linearity of the data suggests Hill's function is valid, though there is still 7% variation in the data not explained by the variation in annulus width. Some of this inaccuracy arises from the test structure layout. The data points far below the line correspond to small microdonuts that were most close to microdonuts with large annulus widths (see Figure 4.14 (d)) and it is felt that these data points represent unaccounted microloading perturbations. These perturbations over a distance of 20 mm and the form of W suggest Jensen et al.'s [94] depletion radius concept is not appropriate for this chamber/process.

FIGURE 4.22 Variation in the normalized etch rate $ER_{Si}(0,0)/ER_{Si,hole}$ at the center of a microdonut hole with the annulus width $r_o - r_i$. The solid line is fitted to the data using LSR with an $R_c^2 = 0.93$. The equation of the fitted line is $ER_{Si}(0,0)/ER_{Si,hole} = 1.0 - 9.1(r_o - r_i)$ ($r_o - r_i$ in m).



The self-loading of trench structures at the center of isolated trenches is similarly derived:

$$\mu_{P,trench}(0,0) = \int_0^{2\pi} \int_0^{\infty} L(\rho, \phi) W(\rho, \phi) \rho d\rho d\phi = 4a \left[\int_0^{\phi_c} \int_0^{\frac{w_o}{2 \cos \phi}} d\rho d\phi + \int_{\phi_c}^{\frac{\pi}{2}} \int_0^{\frac{l_o}{2 \sin \phi}} d\rho d\phi \right], \quad (4.46)$$

where,

$$\phi_c = \text{atan} \left(\frac{l_o}{w_o} \right). \quad (4.47)$$

Equation (4.46) evaluates to

$$\begin{aligned} \mu_{P,trench}(0,0) &= 2aw_o \left\{ \ln \left(\cos \frac{\phi_c}{2} + \sin \frac{\phi_c}{2} \right) - \ln \left(\cos \frac{\phi_c}{2} - \sin \frac{\phi_c}{2} \right) \right\}, \\ &+ \frac{l_o}{w_o} \left[\ln \left(\cos \frac{\phi_c}{2} \right) - \ln \left(\sin \frac{\phi_c}{2} \right) \right] \end{aligned} \quad (4.48)$$

which, for the trenches used in this study (i.e. $l_o = 10w_o$), reduces to $\mu_{P,trench} = 8aw_o$.

4.4.6 ARDE Characterization

The final element needed for the implementation of the depth model is the reaction probability S . To determine S , three wafers each, of donut hole and trench ARDE structures, were processed for 5, 10, 30 and 60 min, which correspond to $\tau = 91, 188, 578$ and 1164 s, respectively. The depth data from these wafers are shown in Figure 4.23 and follow the trend reported by previous authors [67][75][81][78]. The model in (4.30) was fitted by LSR to the entire data set (see Figure 4.24 (a) and (b)) using a single value of $S_D' = 0.24$ with an $R_c^2 = 0.84$. The maximum model error is $\pm 10\%$. The model predicts greater depths for donut holes than is observed, but lesser depths for trenches. Empirical values of R_D , calculated using the depth of smallest feature (circular hole) subtracted from the

depth of the largest feature (rectangular trench), are plotted against the secondary axis of Figure 4.24 (b).

FIGURE 4.23 Etch depth data for a set of donut hole and trench test structures processed for 5, 10, 30 and 60 min, corresponding to total Si etch times $\tau = 91, 188, 578$ and 1164 s, respectively. The solid markers represent depths for donut hole structures. The hollow markers represent depths for trench structures.

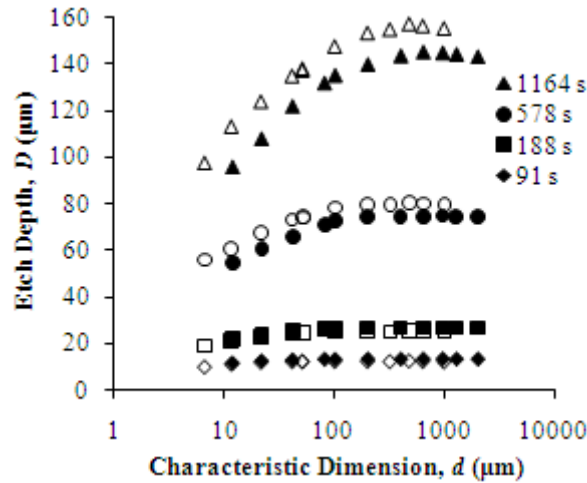
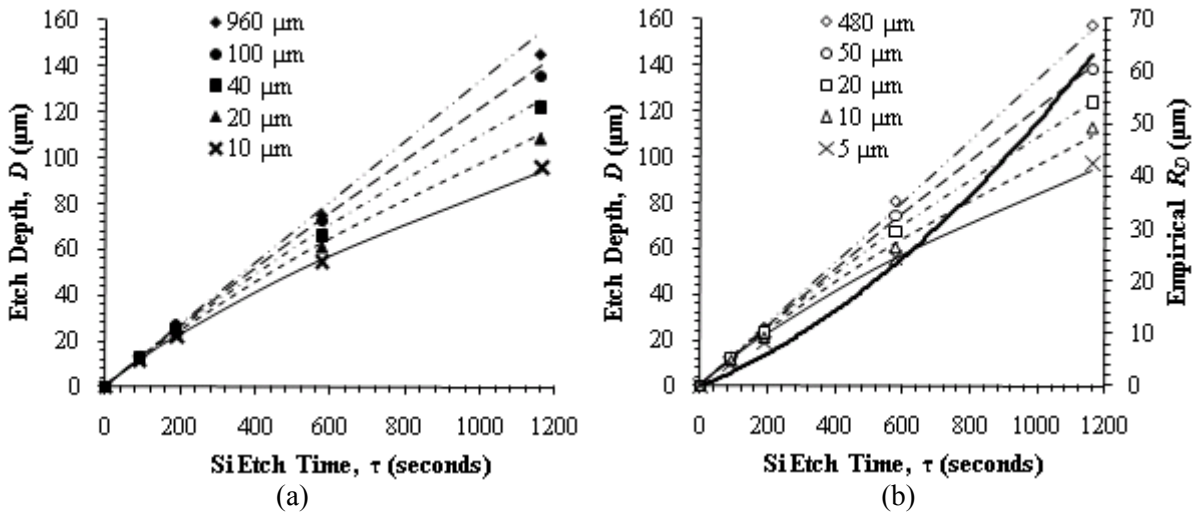


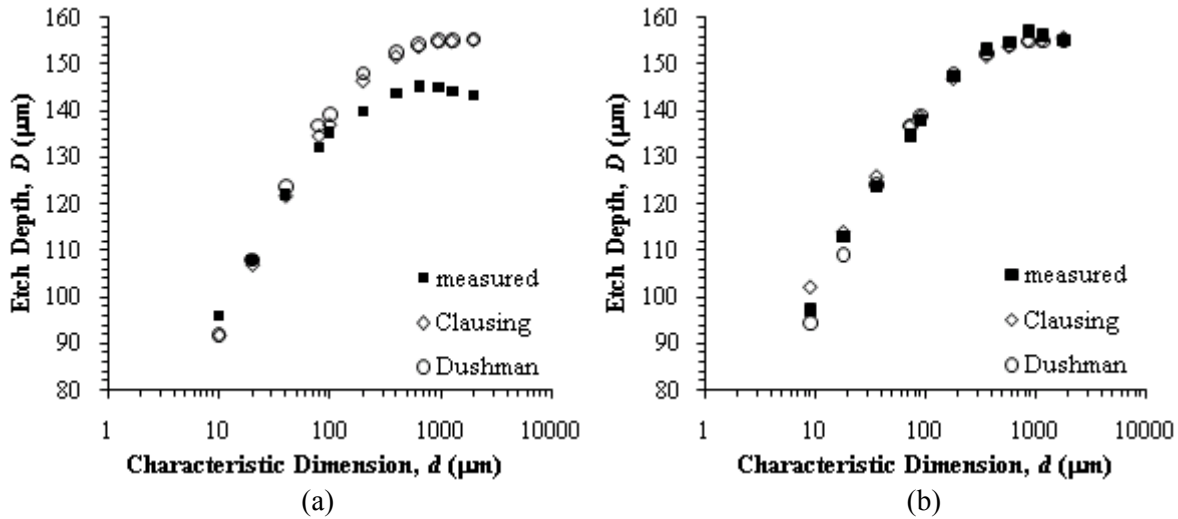
FIGURE 4.24 Comparison of experimental etch depth data and the semi-empirical unified etch model prediction from (4.30) with $S_D' = 0.24$ for (a) donut hole test structures of varying diameter and (b) trench test structures of varying width. The empirical ARDEM range R_D plotted on the secondary axis is calculated by subtracting the depth of the smallest donut hole feature from the depth of the largest trench feature.



As a comparison to the Dushman approximation, numeric integration is used to fit (4.26) to the data using the Clausing factor K_C with S_C' being varied to obtain the best fit by LSR. The maximum error for this model is also $\pm 10\%$ but with a best fit value of reaction probability $S_C' = 0.22$ with an

$R_c^2 = 0.85$. The numeric model using the Clausing factor and the analytic model (4.30) match to within 10% over all structures and the full range of depth. The predictions of (4.30) using the Dushman approximation and the numeric model using Clausing's factor are shown in Figure 4.25.

FIGURE 4.25 Comparison of measured etch depth and modeled etch depths D_D and D_C with characteristic dimension d after a 60 min anisotropic process time (i.e. 1164 s of Si etch time) for (a) circular holes and (b) trenches.

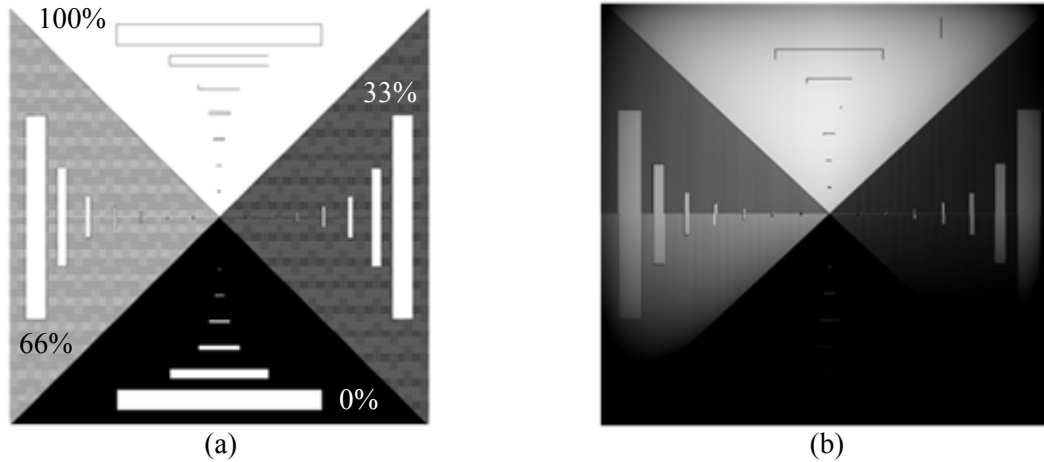


4.4.7 Full Model Validation

The isolated holes, microdonuts and trenches used to characterize the process and validate the depth model from (4.30) and the numeric model using the Clausing factor are too simplistic to represent true IC layouts. A more complex layout was generated to emulate variations in density and feature dimension that might be encountered in a typical IC layout. The layout shown in Figure 4.26 (a) comprises four sets of trenches of varying width from 10 μm to 1000 μm , but constant $l_o:w_o = 10$. The sets of trenches are placed in regions of different local pattern density 0%, 33%, 66% and 100%. Pattern density is varied using square holes of varying size on a constant 10 μm pitch.

FIGURE 4.26 (a) Varying pattern density layout for validating the use of the convolution in (4.21) to determine μ_p . The pattern density of each of the four quadrants is varied using square holes of varying width on a constant 10 m pitch. (b) Numerically computed image of μ_p for the layout in (a). Lighter regions have larger microloading.

white = Si, $L = 1$ black = resist, $L = 0$

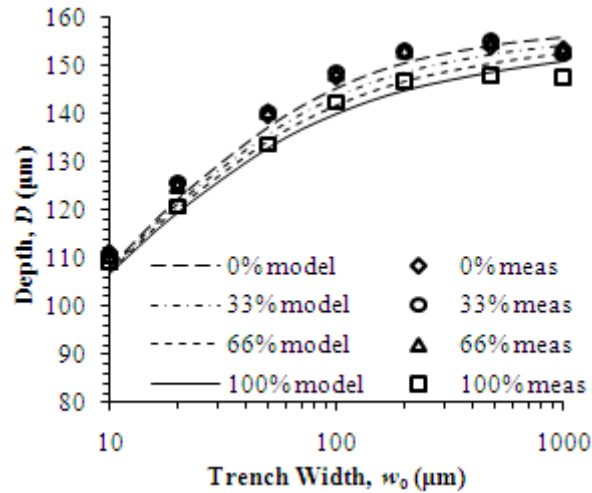


The microloading of each structure is calculated using the convolution in (4.21) and applied in the numeric model using K_C to predict the final etch depth. The convolution to determine $\mu_p(x,y)$ is implemented in Matlab[®] R2008a using the Fast Fourier Transform (FFT). The resulting microload map is shown in Figure 4.26 (b). Due to system memory constraints, the spatial filter and maximum layout dimension is 20,480 μm with a 10 μm pixel size. As mentioned in Section 4.2.3, the center pixel in the spatial filter is given a constant value and the scaling parameter $a = 14 \text{ pixel}^{-1}$.

Three wafers were lithographically patterned and processed for 60 min each using the anisotropic conditions in Appendix C.2. The depth was measured on cross-sections using SEM. Graphs of the predicted etch depths and the actual depths are shown in Figure 4.27. The most striking result of this test is that the magnitude of the difference between the trench depths in the 100% density quadrant and the 0% density quadrant is accurately predicted by the numeric model compared to the measured data (4.3 μm and 5.2 μm , respectively), yet there is no significant difference between the measured trench depths of the 0%, 33% and 66% quadrants. This suggests the process regime is affected locally by the balance of species from the etching of Si and resist and is dependent on the proportion of Si and resist

in the vicinity of the structure. A subsequent test was performed using a coarser pitch of $100\ \mu\text{m}$ to explore this possibility. A significant separation in etch depth was observed between the 0%, 33% and 66% quadrants but the variation with pattern density was still non-linear. Unfortunately, the etch rate in the chamber was 20% lower than in previous tests, indicating a problem with the hardware, so this result may not be a wholly valid comparison.

FIGURE 4.27 Graph of the depth data for the trenches in the layout in Figure 4.26 after an anisotropic etch process time of 60 min and the depths predicted by (4.26) in the numeric model using K_C .



The numeric model underestimates the trench depth for trench widths up to $480\ \mu\text{m}$, which is consistent with the analytic model error for isolated, single trenches in Section 4.4.6; however it overpredicts the depth for the $1000\ \mu\text{m}$ wide trench. The shape of the numeric model prediction for the complex layout is not consistent with the increase in self-loading observed in the measured data for complex and simple layouts and for the analytic model prediction of depths for simple structures. The likely cause of this error is the separation of macroloading and the microloading into independent terms. In theory, they arise from the same mechanism, i.e. the reduction in available F for etching due to the amount of Si exposed to the plasma, and could be combined together in a single term. For layouts that have a uniformly distributed pattern across the wafer the separation of these terms may not be an issue, but for heavy, non-uniform density localizations this simplification may introduce additional errors.

4.5 ARDEM Summary

A unified, semi-empirical model of a time-multiplexed Bosch-type Si etch process is developed for an STS-ASE ICP etcher operating in a neutral-flux-limited process regime. The analytic model using the Dushman vacuum conductance correction factor comprises terms for spatial variation, Si macro-loading, microloading and ARDE and is accurate to within $\pm 10\%$ for donut hole and trench test structures ranging in size from $5\ \mu\text{m}$ to $2000\ \mu\text{m}$ for a fitted reaction probability $S_D' = 0.24$. A numeric model that captures the same sources of variation but which uses the Clausing factor in place of the Dushman factor is accurate to the same degree and matches the analytic model to within 10% over the parameter space with a fitted reaction probability of $S_C' = 0.22$. The trend of decreasing depth with increasing feature size above a critical feature size, an effect of structure self-loading, is accurately predicted by both models. The CW model of ARDE captures the variation in etch depth with time and the relative difference in etch rate of circular holes and rectangular trenches. Hill's $1/\rho$ microloading weighting function is shown to be valid by the linearity of the normalized etch rate for microdonut test structures, however other weighting functions may also prove valid.

It is shown that the analytic model has an advantage over the numeric model in that tapered structures can be accommodated within its framework. The prediction of the tapered model has yet to be tested and provides an opportunity for a future researcher to determine its validity. Alternatively, validation of these predictions could be made by driving the process conditions into a regime that leads to tapered profiles.

The validity of the numeric model using FFT convolution to compute microloading is tested for a complex layout comprising trench test structures embedded in four quadrants of varying pattern density. The errors in the numeric model predictions for the complex layout are consistent with the models for simple, isolated structures and the difference in depth between quadrants of maximum and minimum density are accurately predicted. No significant difference in etch depth is observed between the quadrant with minimum density (i.e. 0%) and those with 33% and 66% density suggesting a non-linear

effect of the local etchant and product composition on process regime and F availability is at play. More work is needed in this area to identify the chemical dynamics that produce this effect and incorporate them into the model. A simple first step would be to repeat this part of the study using oxide and Al masks that would produce a different chemical mix around the etching structure.

The practical issues of ARDEM mask generation are discussed and the method for manually sizing the features on the mask for both structure formation and uniformity enhancement is presented. There is a distinct opportunity and a discernible path for automating the generation of these masks for both applications but much work is necessary to encode a desired 3-D structure, define the constraints that limit the solution space and develop the algorithm to compute the solution and convert it to layout. The issue of 2-D space partitioning is critical and may prove the most difficult part of this task.

A final caveat to the reader: the model structure and characterization methodology are portable but the model parameters are not and must be determined for each process-chamber combination before designing ARDEM masks. Determining whether or not the Rangelow criteria is met and whether free molecular flow models can be applied is the first step.

5

Etch Heating

“It’s not the heat; it’s the humility”

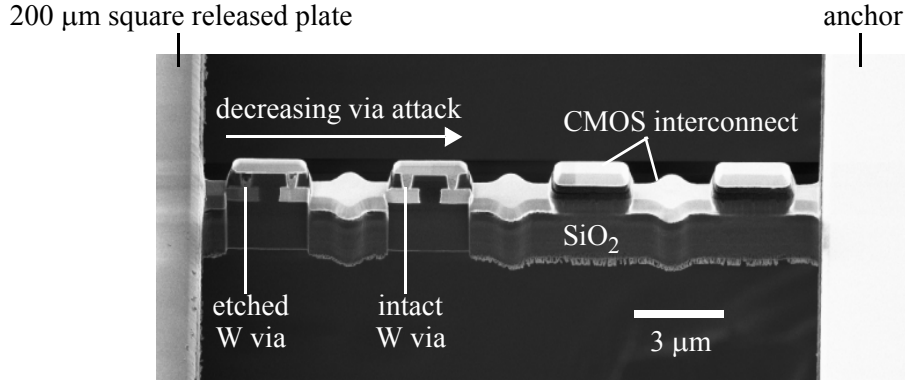
- Yogi Berra

Process flows are complicated objects and as such their failure modes can be subtle and unexpected. At times it is only when devices change in scale that certain failure modes become manifest. The unserendipitous discovery of such failure modes is a humbling experience for the process developer but is stimulating fodder for the researcher. The example of ARDE described in Chapter 4 illustrates this well. Chin et al. [67] were investigating the challenges of an expected device shrink and discovered that structures with very small openings etched slower than those with larger openings. At that time ARDE had not yet been observed because the hole dimensions had not been small enough compared to the film thicknesses to distinguish ARDE from background etch variation.

In this work, the goal of large mirrors with large scan angles and low power consumption drove the release etch process into a regime in which catastrophic electrical failure was caused by the loss of process selectivity to the TiW in the interconnect stack and to the W vias connecting different metal layers. The selectivity loss resulted in these materials being etched away as shown in Figure 5.1. It was discovered that the loss of selectivity is caused by a rapid increase in suspended device temperature after the Si under the suspensions is undercut. Related failure mechanisms, such as loss of DRIE anisotropy and CD loss have been reported by Qu and Xie [98] and Alper et al. [99], respectively. Qu

and Xie [98] made an estimate of a 100 °C temperature rise due to ion bombardment, but did not experimentally validate their estimate or consider other heating, or cooling mechanisms.

FIGURE 5.1 *FIB* cross-section and image of *W* via attack in a via chain suspending a 200 μm square plate. The via farthest to the left is open circuit.



This chapter details the investigation of etch heating and the loss of etch selectivity during plasma release etch. The plasma regime of the release etch process is established in order to identify the appropriate models to apply in the analysis. *In situ* infrared imaging is applied to demonstrate the magnitude of the temperature increase on suspended devices. A model is derived and fit to the device temperature data by LSR using the proportion of reaction heat ν absorbed by the structure as the sole fitting parameter. The relative contributions of the different heating and cooling mechanisms are quantified.

5.1 Effect of Temperature on Etch Selectivity and Temperature

Flamm [83] reported a decrease in selectivity with increasing temperature for the etching of Si and SiO₂ by F. The mechanism arises from the Arrhenius' relation describing the etch rate ER_m of a material in a plasma:

$$ER_m = \frac{\Gamma_m}{c_m} = A c_e T^{0.5} \exp\left(-\frac{E_A}{k_B T}\right), \quad (5.1)$$

where, Γ_m is the flux of the etched material out of the surface in $\text{mol}\cdot\text{m}^{-2}\text{s}^{-1}$, c_m is the molar density of the etching material $\text{mol}\cdot\text{m}^{-3}$, T is the temperature at the etching surface in K, A is the pre-exponential

factor in $\text{m}^4\text{K}^{-1/2}\text{s}^{-1}\text{mol}^{-1}$, c_e is the molar concentration of etchant species at the etching surface in $\text{mol}\cdot\text{m}^{-3}$, E_A is the activation energy of the reaction in $\text{J}\cdot\text{particle}^{-1}$ and k_B is Boltzmann's constant in $\text{JK}^{-1}\text{particle}^{-1}$. The selectivity of an etch process for two materials, X and Y, where Y is the more slowly etched material, is expressed as

$$S_{XY} = \frac{ER_X}{ER_Y} = \frac{A_X}{A_Y} \exp\left(\frac{E_{A,Y} - E_{A,X}}{k_B T}\right) \quad (5.2)$$

and decreases toward the ratio of the pre-exponential factors as T at the etching surface increases.

Flamm's analysis is assumed to represent the phenomena causing the via attack shown in Figure 5.1. The next step is to identify the mechanisms by which heat is introduced to the structure. Ion bombardment and exothermic reaction heat are identified as candidates. Whenever heat flows into a structure its temperature will rise indefinitely unless there are channels through which heat flows out of the structure. Radiation to the surrounding chamber and the ambient and solid conduction through the device suspensions to the cooled substrate are identified as the cooling mechanisms. The power balance is then formed using appropriate expressions for the heating and cooling terms.

5.2 Plasma Regime

5.2.1 Plasma Parameters

Plasmas for material processing straddle regimes of sheath type (collisional to collisionless), flow type (laminar to turbulent) and plasma frequency (low, in which the ions follow the changing fields, to high, in which the ions can only respond to the DC field component) [97]. The equations describing the movement of ions and neutral species in the plasma are specific to the plasma regime and process chamber type in which they are found, so the establishment of the plasma regime is critical to the correct mathematical description of the plasma.

The plasma regime depends on several factors such as the chamber shape and size, the excitation type and frequency, the chemical constituents of the plasma, the flow rate and the pressure [97]. In turn, these conditions determine the gas density c_g , the composition profile of species in the plasma (profile - because species and their relative concentrations are necessary), the gas temperature T_g and the electron temperature T_e . With the knowledge of these parameters and the materials exposed to the plasma, the regime can be identified and the process fully characterized. Unfortunately, with the exception of c_g , the other parameters are not known *a priori* and must be measured for each plasma. The measurement equipment and expertise were not available for this investigation so it is necessary to refer to the literature and make inferences about the aforementioned parameters.

The plasmas investigated in this chapter are an anisotropic Bosch-type DRIE process and an isotropic etch process listed in Appendix C.2. The test die is described in Section 5.6, but at this juncture it suffices to state that the bulk of the material exposed to the plasma is Al, Si, SiO₂ with trace amounts of TiW. In the remainder of this section, the process of inferring the defining parameters of the plasma, based on ICP etch systems and SF₆-based plasmas reported in the literature, is detailed. The estimation of the parameters is done to facilitate the qualitative categorization of the plasma regime and provide reasonable numerical accuracy for the analysis of microstructure heating during plasma release etch processes.

5.2.2 Etchant and Product Species

The primary constituent of the gas in-flow to the chamber is SF₆. In the anisotropic step there is a relatively small additional flow of O₂. The neutral F density in the bulk plasma c_{Fb} is estimated to be on the order of 5% of the gas density based on the work of Ryan and Plumb [84].

The gas is introduced to the chamber through a showerhead at a rate between 130 sccm (isotropic step) and 143 sccm (anisotropic step), leading to a stagnation zone over the surface of the wafer in which neutral transport to, and product transport from, the etching surface are dominated by diffusion

processes. Kiehlbauch and Graves [95] simulated this plasma scenario for Cl etching of Si and found no radial flux component for product species over the surface of the wafer, from which we infer the transport of neutral species toward the surface is also predominantly axial. Economou et al. [96] used Monte Carlo simulation of Si etching by Cl in an ICP chamber with a similar flow regime to show that neutral concentration is constant within 50 mm of the wafer centre, which we infer by scaling, translates to a zone of constant F concentration within 25 mm of the wafer centre in this work.

The product stream in the etching of Si by F is predominantly SiF_4 with a significant proportion of SiF_2 . Flamm [83] reported the range of SiF_4 to be from 70% to 95%. With the assumption of 5% neutral F concentration in the plasma, the product flux is not a significant contributor to the transport behavior of neutral F, which is dominated by SF_6 .

The diffusivity of F in m^2s^{-1} in a mixture of F and SF_6 is determined using the formula from Dushman and Lafferty [85]:

$$D_{\text{F-SF}_6} = \frac{4\sqrt{2}}{3p(\delta_{\text{F}} + \delta_{\text{SF}_6})^2} \left(\frac{k_{\text{B}}T_{\text{g}}}{\pi} \right)^{1.5} \left(\frac{1}{m_{\text{F}}} + \frac{1}{m_{\text{SF}_6}} \right)^{0.5}, \quad (5.3)$$

where p is pressure in Nm^{-2} , T_{g} is the gas temperature in K, k_{B} is Boltzmann's constant, δ_{F} and m_{F} are the atomic diameter in m and mass of F in kg, respectively, and δ_{SF_6} and m_{SF_6} are the molecular diameter in m and mass of SF_6 in kg, respectively. The values of $D_{\text{F-SF}_6}$ are calculated using $\delta_{\text{F}} = 100 \times 10^{-12}$ m [87], $\delta_{\text{SF}_6} = 550 \times 10^{-12}$ m [88], $m_{\text{F}} = 3.16 \times 10^{-26}$ kg and $m_{\text{SF}_6} = 2.11 \times 10^{-25}$ kg [87].

5.2.3 Arrhenius Relation Parameters

The Arrhenius relation in (5.1) contains two parameters, the pre-exponential factor A and the activation energy E_{A} that must be known in order to predict the etch rate for a given temperature. The determination of these parameters is straightforward as shown by Manos and Flamm [101]. The etch

rate is measured over a range of temperatures and plotted against the logarithm of the temperature. The gradient of the plot is used to extract E_A and the intercept is used to extract A . This is done for the anisotropic and isotropic etch processes from 10 °C to 35 °C and the values are given in Table 5.1.

5.2.4 Ionic Flux Composition

The ionic composition of the plasma and the relative densities of each species are inferred from the mass spectrometric work of Goyette et al. [102] who studied the ionic composition and ion energy distributions in inductively-coupled SF₆ and SF₆/O₂ plasmas at 5 mT and 200 W and an SF₆/Ar plasma from 5 mT to 20 mT and 100 W to 300 W. The dominant trend of ionic composition with pressure is used to predict the ionic composition of the SF₆ and SF₆/O₂ plasmas in the CMU STS-ASE at 50 mT and 25 mT, respectively. For example, they reported that S⁺ was the predominant ion in a SF₆ plasma at 5 mT and 200 W but that for an SF₆/Ar plasma, a similar high S⁺ proportion at 5 mT rapidly decreased with pressure until it reached trace levels in comparison to SF₃⁺ and SF₅⁺. This trend in S⁺ proportion is assumed valid for the other plasmas they studied.

Goyette et al. found O containing ions in the SF₆ plasma, which they attributed to etching of the quartz chamber hardware. The CMU STS-ASE uses ceramic hardware, so O containing ions are not expected except when O₂ is added to the gas stream. By comparing the relative changes in the ionic species of the SF₆ and the SF₆/O₂ plasmas they reported, it is inferred that the absence of SO⁺ and SOF⁺ in the CMU SF₆ plasma translates to a commensurate increase in the proportions of SF⁺ and SF₂⁺, respectively, with a corresponding decrease in F⁺. The ionic species expected in the CMU STS-ASE and their relative densities and plasma frequencies are listed in decreasing order of density in Table 5.1. SF₅⁺ is the largest ion expected. Data on ionic cross-sections from [97] are used to make a very conservative estimate of collision cross-section for the calculation of ionic mean free path.

5.2.5 Gas Temperature

The gas temperature T_g is estimated from the work of Piejak et al. [86] who analyzed the problem by considering the mechanisms by which the gas in a low pressure discharge chamber can heat and cool. They state that electron-atom elastic conditions and ion-atom charge exchange collisions are the main ways that electrical energy is transformed to heat in the bulk gas through the kinetic energy of the charged species. Electrons have a distribution of energies that Piejak et al. assumed to be Maxwellian so the power transferred through elastic collisions with atoms was integrated over the electron velocity space. Ions have a more narrowly defined velocity, and hence a more narrowly defined energy that depends on the ion mass, its mean free path and the electric field generating the plasma. With the concept of mean free path, the probability that an ion transfers its charge to an atom in the plasma, prior to colliding with the walls of the chamber, was defined and the rate of energy transfer was calculated. Piejak et al. went on to show that at low pressures (i.e. the mT pressure regime) the energy transferred to the gas by ion-atom charge exchange dominates with a maximum at ~ 1 mT. They solved the heat equation to determine the gas temperature at the center of the plasma.

As stated above, the main species in the DRIE process is SF_6 and the main ion is SF_3^+ , or similarly heavy ions, for both isotropic and anisotropic processes. This leads to a factor-of-two reduction in the energy lost per ion-molecule collision compared to Piejak et al.'s calculation, with a commensurate reduction in gas temperature. The values of T_g for the anisotropic and isotropic steps are listed in Table 5.1. Using the estimated values of T_g from Table 5.1, the ideal gas law is applied to determine the gas density c_g .

5.2.6 Electron Temperature and Ion Density

Bhardwaj and Ashraf [65] reported ion density and electron temperature at the centre of the plasma generation region in an STS-ASE ICP chamber in which the wafer was raised to within 10 mm of the bottom plane of the RF coil (cf. the CMU chamber in which the coil-wafer separation is 130 mm). Their work explored an Ar plasma from 1 mT to 10 mT over a range of coil powers from 10 W to

800 W. From their report, the electron temperature $T_e = 2.8$ eV and the ion density $c_i = 2.7 \times 10^6$ mol·m⁻³ at 600 W coil power and 5 mT pressure.

Hori et al. [103] explored the magnitude and spatial distribution of T_e and c_i for an Ar plasma formed in a proprietary ICP reactor over a wider range of process pressures up to 20 mT. Their data indicates that T_e is roughly constant with coil power but follows a power law for pressure and that c_i saturates above 500 W but varies roughly linearly with pressure. Those trends are used to extrapolate the values extracted from Bhardwaj and Ashraf's work up to 25 mT and 50 mT for the anisotropic and isotropic processes, respectively and are shown in Table 5.1.

Rauf et al. [104] plotted the axial variation in SF_3^+ density in an ICP chamber and showed a decrease of almost an order of magnitude for SF_3^+ over a 20 mm distance from the centre of the plasma. Given a distance of 130 mm from the bottom of the RF coil in the CMU STS-ASE chamber, c_i is estimated to decrease by three orders of magnitude between the plasma generation region and the wafer surface. The values of c_g for the anisotropic and isotropic processes are given in Table 5.1.

5.2.7 Sheath Type

Sheaths can be collisional (i.e. ions experience collisions as they traverse the sheath) or collisionless, high frequency (i.e. the ion frequency is less than the frequency of the electric field variation in the sheath) or low frequency. The sheath classification depends on the ions in the plasma, the electron temperature, the frequency of the source and the sheath thickness. This section assesses the plasma characteristics to infer the sheath type.

The Debye length, which represents the distances over which electric field differences can be sustained, characterizes the plasma. Its value in m is given by [97]

$$\lambda_{De} = \left(\frac{\epsilon_0 T_q}{q N_A c_i} \right)^{0.5}, \quad (5.4)$$

where ϵ_0 is the permittivity of free space, T_q is the electron temperature in eV, c_i is the molar ion density $\text{mol}\cdot\text{m}^{-3}$, N_A is Avogadro's number and q is the electronic charge.

The sheath thickness is derived from λ_{De} using the Child law of space-charge-limited current in a plane diode [97]. For a given voltage across the sheath, which is approximated by the bias voltage V_b , the sheath thickness t_s is

$$t_s = \frac{\sqrt{2}}{3} \lambda_{De} \left(\frac{2V_b}{T_q} \right)^{0.75}. \quad (5.5)$$

The mean free path of an ion in the plasma is determined using

$$\lambda_i = \frac{1}{N_A c_g \sigma_i}, \quad (5.6)$$

where c_g is the gas density in $\text{mol}\cdot\text{m}^{-3}$ and σ_i is the total collision cross-section for the ion in m^2 comprising elastic scattering and charge-transfer interactions. The collision cross-section can only be measured experimentally and could not be found independently for the ions identified as constituting the plasma in this study. Lieberman and Lichtenberg [97] provide a set of graphs for the cross-section of atoms varying in size from He to Ar for a range of voltages. These graphs are used to infer the collision cross-section.

The ion frequency f_i represents the speed with which the ions can respond to time varying fields in the plasma. It is given by

$$f_i = \frac{1}{2\pi} \left(\frac{q^2 N_A c_q}{\epsilon_0 m_i} \right)^{0.5}, \quad (5.7)$$

where c_q is the electron density in $\text{mol}\cdot\text{m}^{-3}$ and m_i is the ion mass in kg.

Table 5.1 lists the relevant plasma parameters for the determination of sheath type and the etch heating behavior for the structures in this investigation. The parameter values have been inferred for an

SF₆-based plasma in an ICP chamber for a particular set of process conditions and cannot be taken as representative of DRIE processes *in toto*.

TABLE 5.1 Plasma parameters characterizing the Si etch steps of the Bosch-type, DRIE process in Appendix C.2 for an STS-ASE chamber.

Parameter	Anisotropic	Isotropic	Units
c_g , gas density	1100	2100	$\times 10^{-6} \text{ mol}\cdot\text{m}^{-3}$
c_{Fb} , F bulk density	50	110	$\times 10^{-6} \text{ mol}\cdot\text{m}^{-3}$
c_i , ion density	0.013	0.027	$\times 10^{-6} \text{ mol}\cdot\text{m}^{-3}$
T_g , gas temperature	350	380	K
T_q , electron temperature	1.9	1.6	eV
λ_{De} , Debye length	0.11	0.07	$\times 10^{-3} \text{ m}$
t_s , sheath thickness	2.0	1.8	$\times 10^{-3} \text{ m}$
Ion species	SF ₃ ⁺ , SF ₅ ⁺ , SiF ₃ ⁺ , SOF ⁺	SF ₃ ⁺ , SF ₂ ⁺ , SF ₅ ⁺	
$\sigma_{SF_5^+}$, collision x-section	50	50	$\times 10^{-18} \text{ m}^{-2}$
λ_i , SF ₅ ⁺ mean free path	3.0	1.8	$\times 10^{-3} \text{ m}$
$y_{i,j}$, relative ion density	0.3, 0.3, 0.2, 0.2	0.5, 0.3, 0.2	%
Γ , ion flux	20 (17 - 22)	35 (29 - 40)	$\times 10^{-6} \text{ mol}\cdot\text{m}^{-2}\cdot\text{s}^{-1}$
$f_{YZ_x^+}$, ion frequency	6, 5, 6, 7	9, 10, 7	MHz
D_{F-SF_6} , diffusivity	0.5	0.3	$\text{m}^2\cdot\text{s}^{-1}$
E_A , activation energy	6	11	$\times 10^{-21} \text{ J}$
A , pre-exponential factor	240	480	$\times 10^{-6} \text{ m}^4\text{K}^{-1/2}\cdot\text{s}^{-1}\cdot\text{mol}^{-1}$

Based on the estimated parameter values shown in Table 5.1, the ion mean free paths are approximately equal to the sheath thicknesses and the ions are unable to respond to the time varying sheath potential. Thus, the CMU STS-ASE processes can be approximated as operating in a high frequency plasma regime with a collisionless sheath.

5.3 Etch Heating Mechanisms

Ion bombardment and chemical reaction heat have been cited as significant sources of heat flux for substrates during plasma etch processes [86], [105], [106], [107], [108]. The relative magnitude of each contribution to the total heat flux into the substrate is dependent on the plasma chamber type, process conditions, process regime and reaction kinetics for a given gas mixture and substrate composition (i.e. both the materials to be etched and the masking materials).

Qu and Xie's analysis [98] of the temperature increase of a suspended microstructure during release etch considered only ion bombardment. That assumption is based on cited references [107], [109] that do not consider etching of Si by F in an STE-ASE ICP chamber using a SF₆-based plasma. In the STS-ASE chamber, the bias voltage on the substrate is controlled independently and the etch rate is significantly higher (on the order of m·min⁻¹) than in parallel plate reactors [107], or in the etching of Ir and Pt in CF₄/O₂ plasmas at substrate temperatures less than 100 °C [109]. Thus, the appropriate mechanisms to include in the analysis of etch process heating of suspended microstructures are reconsidered here.

5.3.1 Reaction Exothermicity

Kersten et al. [105] obtained data on F etching of Si in a parallel plate reactor that suggests reaction heat contributes to the temperature increase of a substrate, but their study does not analyze or quantify the effect. Kersten et al. [106] later reported that exothermic reaction heat contributes significantly to substrate heating in the cleaning of organic contaminants from a metal surface using a DC O₂ plasma. Given these reports, the high etch rate of Si by F in an ICP chamber and the large amount of heat ΔH released in the formation of the main reaction products, SiF₄ and SiF₂ [101] ($\Delta H_{\text{SiF}_4} = -1615 \text{ kJmol}^{-1}$ and $\Delta H_{\text{SiF}_2} = -588 \text{ kJmol}^{-1}$ [110], cf. $\Delta H_{\text{CO}_2} = -393.5 \text{ kJmol}^{-1}$ and $\Delta H_{\text{CO}} = -110.5 \text{ kJmol}^{-1}$ [111]), the contribution of reaction heat to microstructure heating during Si release etch must be included in an etch heating analysis.

Etch rates typically vary over a surface, so the heat released by the etch reaction must be considered for a differential area and integrated over the surface to find the total heat released by the etch reaction. For a Si etch rate ER_{Si} , given by (5.1), the rate dP_e at which energy is released into a structure from a small etching area dA_e is

$$dP_e = \upsilon dA_e ER_{\text{Si}} c_{\text{Si}} \sum_k x_k \Delta H_k, \quad (5.8)$$

where υ is the proportion of reaction heat absorbed by the structure ($1 - \upsilon$ is the proportion carried off as translational, rotational and vibrational kinetic energy by the volatilized product species), c_{Si} is the molar density of Si and x_k is the fractional yield of the k^{th} product species with reaction heat ΔH_k in Jmol^{-1} . For Si etching in F plasmas

$$\sum_k x_k \Delta H_k = x_{\text{SiF}_4} \Delta H_{\text{SiF}_4} + x_{\text{SiF}_2} \Delta H_{\text{SiF}_2}, \quad (5.9)$$

where x_{SiF_4} is expected to lie in the range from 70% to 90% [83]. Using (5.9), the product weighted reaction heat released in the etching of Si by F is between -1307 kJmol^{-1} and -1564 kJmol^{-1} , a 20% variation. The product mix and the values of x_k are assumed constant with temperature and process conditions. The value of υ is unknown and the authors do not know of any analysis of this parameter in the literature. υ is assumed to be constant across all etch products and over all temperatures for the purposes of this study.

The integrated form of (5.8) depends primarily on the shape of the surface being etched; however, the reality of the etching situation is convoluted by microloading, ARDE and ion and neutral shadowing, effects that are known to cause etch rate variation across structures. Pattern-based and spatial etch rate variations are dependent on the etch process and pattern being etched and therefore must be ana-

lyzed on a case-by-case basis. This aspect of the problem is analyzed in Section 5.8 where the test structure geometry and topography are presented in detail.

5.3.2 Ion Bombardment

For a high frequency, collisionless sheath, the ion motion is determined by the DC fields. The flux of the j^{th} ionic species at the edge of the plasma sheath is

$$\Gamma_{i,j} = c_{i,j} v_{B,j}, \quad (5.10)$$

where $v_{B,j}$ is the Bohm velocity in ms^{-1} , given by [97]

$$v_{B,j} = \left(\frac{qT_q}{m_{i,j}} \right)^{0.5}. \quad (5.11)$$

For collisionless sheaths, the flux at the wafer surface is equal to the flux at the sheath edge and is also given by (5.10). The total flux due to all ionic species is

$$\Gamma_i = c_i (qT_q)^{0.5} \sum_j \frac{y_{i,j}}{m_{i,j}^{0.5}}, \quad (5.12)$$

where $y_{i,j}$ are the fractional ion densities. Estimated values of Γ_i are given in Table 5.1 for the anisotropic and isotropic processes. The flux values in parentheses in Table 5.1 represent the fluxes that would be obtained if the heaviest or the lightest ion were the only species contributing to the flux. From these values, the uncertainty in the composition of the plasma leads to a maximum relative flux error of 17%.

For a bias voltage V_b applied to the wafer, the power incident on a structure of plan view area A_p is

$$P_i = qA_p \Gamma_i V_b = qc_i A_p V_b (qT_q)^{0.5} \sum_j \frac{y_{i,j}}{m_{i,j}^{0.5}}. \quad (5.13)$$

The uncertainty in c_i is the largest source of error in P_i and even with the good faith estimate put forward in Table 5.1, it is possible these values could still be off by as much as an order of magnitude. As P_i is a linear function of V_b , the variation in structure temperature T with V_b is a good indicator of the magnitude of the flux and provides validation of the magnitude of the estimate.

5.4 Etch Cooling Mechanisms

Piejak et al. [86] considered radiation and plasma conduction as the significant cooling paths for the probes in their study as they were able to reduce conductive cooling through the probe shaft to a negligible value. In the present study, the test structures, which are described in Section 5.6, are designed so conduction through a suspension of known geometry is the main cooling path at temperatures < 75 °C, while radiation becomes significant only at temperatures > 100 °C. Analysis of cooling by plasma conduction for these structures using Dushman's formula for free molecular conduction [85] shows this mechanism leads to a heat flux at the ICP chamber platen temperature that is three orders of magnitude smaller than those due to radiation and solid conduction and its contribution decreases with increasing temperature. Plasma conduction is neglected in further analysis and heat transfer by solid conduction and radiation are considered exclusively.

5.4.1 Radiation

The net power transfer by a diffusely radiating structure of surface area A_r and uniform emissivity ε at uniform temperature T with respect to its surroundings at temperature T_0 is

$$P_r = \varepsilon \sigma A_r (T^4 - T_0^4), \quad (5.14)$$

where σ is the Stefan-Boltzmann constant. Emissivity varies from material to material and also with the condition of the emitting surface, whether polished, rough, oxidized, etc. For Al, ε values from 0.01 to 0.5 [111], [112] have been reported and for Si, values around 0.1 [113]. The test structure sur-

faces are rough and darkened by the processing, a characteristic noted in all cases to be dominant and to increase emissivity, so the approximation of equal emissivities is reasonable.

A more contentious issue is the variation of ε with T . Bartl and Baranek [112] reported on Al emissivity variation with a number of parameters including T , for which ε varied from 0.025 to 0.032 from 300 K to 400 K. They note that previously published empirical relations are not universal. In light of the lack of agreement in the literature over the functional form of the relation between ε and T , it is necessary to make the unsatisfactory assumption of constant ε over the range of temperatures observed in etch heating, with the awareness that this is a source of error.

5.4.2 Solid Conduction

A released microstructure has some form of suspension, or tether, preventing it from floating away and the suspension serves as a solid conduction path during processing when convection and gas conduction through the plasma is negligible. For a microstructure at temperature T suspended by N beams of length l and rectangular cross-section of width w and thickness t , the power flowing through the suspension to thermal ground at temperature T_a is

$$P_c = G_{\text{th},s} \Delta T = \frac{N \kappa_{\text{eff}} w t}{l} (T - T_a), \quad (5.15)$$

where $G_{\text{th},s}$ is the lumped, 1-D thermal conductance of the suspension and κ_{eff} is the effective thermal conductivity of a multilayer suspension.

5.5 Etch Heating Power Balance

The determination of the steady state temperature of a suspended microstructure is found by considering the power balance between heat input (P_i and P_e) to and heat output (P_r and P_c) from the microstructure:

$$P_i + P_e = P_r + P_c. \quad (5.16)$$

Detailed expressions for P_i , P_r , P_c and P_e , from (5.13), (5.14), (5.15) and the integrated form of (5.8), respectively, depend on the type and shape of the structure being etched. Section 5.6 to Section 5.8 describe the test structures used in this study and develops the power balance equation for two periods of interest during the release etch process.

5.6 Etch Heating Test Structures

The test structures used in this study are designed to mimic the CMOS-MEMS structures on which the loss of selectivity is observed (see Figure 5.1). The test structures are fabricated using a process flow that closely followed the post-CMOS process. The test structures and process flow are described in this section.

Two time periods in the release etch process are targeted for investigation: the anisotropic overetch and the isotropic overetch. Overetching is a necessary evil in any plasma etch process because the end-point (i.e. that point in time when the etching film breaks through) is not constant from run to run, across a wafer, a chip or even a structure, due to effects like incoming mask and film thickness variation, spatial variation, microloading and ARDE. In a release etch process, the overetch is that time period between the first structure on a wafer releasing and the last structure on the wafer releasing. In practice, these points in time are unknown, so the process developer adds a small amount of time to cover statistical variations. It is surmised that the damage to the vias in Figure 5.1 and the artifacts observed by Qu and Xie [98] and Alper et al. [99] are created during one of these overetches.

5.6.1 Etch Heating Test Structure Concept

In the final steps of CMOS-MEMS fabrication with backside ARDEM processing (see Section 3.3.2 and Section 3.3.3), the microstructures are released from the constraints of the substrate

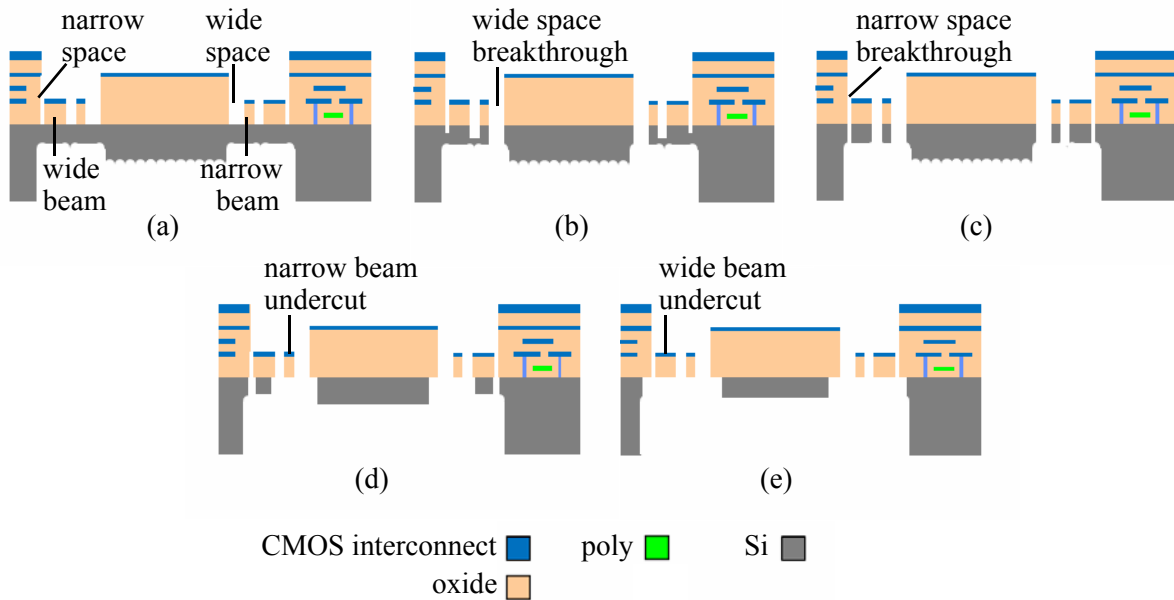
by anisotropically etching through the thinned Si in the device regions (Figure 5.2 (b) and (c)) and isotropically removing the Si under the suspensions of the microstructures (Figure 5.2 (d) and (e)).

Aspect ratio dependent etching (ARDE) adversely affects this part of the process such that the Si under narrow spaces breaks through later in the process than the Si under wide spaces. The isotropic release etch rate is also aspect ratio dependent, so microstructures next to narrow spaces release later than those next to wide spaces, and is exacerbated if wide beams are next to narrow spaces in the same structure that has narrow beams next to wide spaces. The result is a wide range of release times for different microstructures and a varied set of process conditions experienced by them.

FIGURE 5.2 Detail of impact of anisotropic and isotropic ARDE on the overetch times of the CMOS-MEMS fabrication flow with backside ARDEM. (a) Before the start of the release etch process. (b) Widest space breakthrough. (c) Narrowest space breakthrough. (d) Widest space, narrowest beam undercut. (e) Widest beam, narrowest space undercut.

images not to scale

relative dimensions for indication only



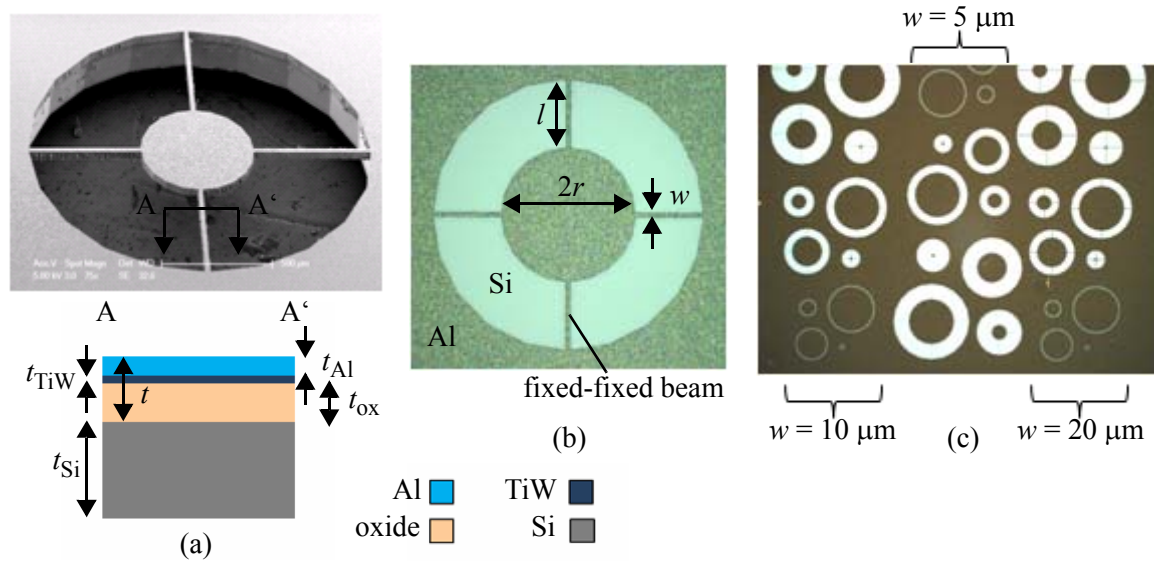
The test structures for the etch heating investigation are designed to capture the variation in Si thickness that lead to a variation in breakthrough time in the anisotropic etch step and the variation in suspension beam width that lead to a variation in the undercut time in the isotropic etch step. The thickness of the Si is varied also to change $G_{th,s}$ in the anisotropic step. Convolution of these effects

with beam spacing is eliminated by isolating individual beams. A circular disc is chosen to emulate the device because of the simplifications it provided in temperature calculations and the elimination of corner curling.

5.6.2 Etch Heating Test Structure Fabrication

The detailed process flow used to fabricate the etch heating test structures is given in Appendix B.9. What follows is a brief description of the flow with figures to illustrate the structure topology. The test structures are formed on thermally oxidized, double-sided-polished <100>, 100 mm diameter Si wafers with thickness $t_w = 220 \mu\text{m}$. The thermal oxide thickness $t_{\text{ox}} = 1.5 \mu\text{m}$. The test chips comprise discs suspended by $N = 4$ fixed-fixed beams as shown in Figure 5.3 (a). To eliminate the need to plasma etch the backside oxide, the wafers are coated on the frontside with resist and buffered HF is used to remove the backside oxide before beginning test structure fabrication. To mimic the JAZZ CMOS metal stack, a $t_{\text{TiW}} = 0.1 \mu\text{m}$ layer of TiW is sputter deposited on the frontside, followed by a $t_{\text{Al}} = 0.7 \mu\text{m}$ layer of Al. The resultant stack of oxide/TiW/Al (see Figure 5.3 (b)) with $t = 2.3 \mu\text{m}$ approximates the relative dimensions of the layers in a m1 CMOS-MEMS beam. The upper layer of TiW on foundry CMOS-MEMS chips is etched away during the frontside oxide etch and the anisotropic Si etch, which is why the test structure is capped by Al and not TiW.

FIGURE 5.3 *Suspended disc test structures for etch heating investigation. (a) SEM of suspended disc and cross-sectional schematic of the beam structure. (b) Optical microscope image of a disc structure after patterning. (c) Optical microscope image of the disc array on a single test structure die.*



The test structure wafer is photolithographically patterned with arrays of disc test structures (see Figure 5.3 (c)). The Al and TiW are wet etched. The backside ARDEM pattern is formed photolithographically at the wafer-level. The wafer is then diced into individual test structure chips that are processed using the flow shown in Figure 3.6 and Figure 3.7. An exception occurs because the metal structures are not embedded in oxide but formed on top of it and so the oxide removal step of Figure 3.7 is modified. The test structure geometric design space is detailed in Table 5.2 and explores all 108 combinations of the geometric parameters.

TABLE 5.2 *Geometric parameter space of the etch heating test structures.*

Parameter	Values (μm)
l	25, 250, 500
w	5, 10, 20
r	50, 250, 500, 750
t_{Si}	25, 40, 80

5.7 Etch Heating Scenarios

Four scenarios occur in which the temperature of the microstructures is affected by the heating processes described in Section 5.3. These scenarios correspond to the periods in the release etch process shown in Figure 5.2 (b) to (e). The scenarios shown in Figure 5.2 (b) and (d) are characterized by evolving thermal isolation as the Si thins in the open areas of the structure, or is etched away under narrow structures. The scenarios shown in Figure 5.2 (c) and (e) are characterized by approximately constant heat fluxes and thermal conductances, provided anisotropy is maintained during the period shown in Figure 5.2 (c) and the Si under the suspension is not undercut.

A 1-D analysis of the time varying thermal conductance to ground, for a group of test structures through these four periods of the release etch, highlights the evolution of thermal isolation in suspended microstructures.

5.7.1 Anisotropic Si Etch to Breakthrough

The structure shown in Figure 5.3 (a) is decomposed into a thinning Si annulus surrounding the suspended disc, four metal/oxide multi-layer beams and the Si under the metal/oxide beams. During the anisotropic etch to breakthrough (Figure 5.2 (b) and (c).), the exposed Si thins continuously over time, while the Si beams under the metal develop. The thermal conductance of the thinning Si annulus is modeled as

$$G_{\text{th,ann}} = 2\pi\kappa_{\text{Si}}(t_{\text{Si}} - ER_{\text{Si}}\tau_{\text{aniso}}) \left[\ln\left(\frac{r+l}{r}\right) \right]^{-1}, \quad (5.17)$$

where κ_{Si} is the Si thermal conductivity and τ_{aniso} is the elapsed time in the anisotropic etch step. The thermal conductance of the developing Si beam is

$$G_{\text{th,Sibeam}} = \frac{Nw\kappa_{\text{Si}}ER_{\text{Si}}\tau_{\text{aniso}}}{l}. \quad (5.18)$$

The total thermal conductance, $G_{th,1}$ of the structure during this period (Figure 5.2 (b)) is found by adding (5.17) and (5.18) to the lumped conductance of the metal-oxide suspensions:

$$G_{th,1} = \frac{Nw}{l}(\kappa_{eff}t + \kappa_{Si}ER_{Si}\tau_{aniso}) + 2\pi\kappa_{Si}(t_{Si} - ER_{Si}\tau_{aniso})\left[\ln\left(\frac{r}{r+l}\right)\right]^{-1}, \quad (5.19)$$

where κ_{eff} for the test structure suspension is

$$\kappa_{eff} = \frac{\kappa_{Al}t_{Al} + \kappa_{TiW}t_{TiW} + \kappa_{ox}t_{ox}}{t}. \quad (5.20)$$

5.7.2 Anisotropic Overetch

After the Si breaks through in all areas there is an overetch period (Figure 5.2 (c)) whose duration depends on the uncertainty in t_{Si} and etch rate variation of the process. The thermal conductance during the overetch, assuming no loss of anisotropy, is given by

$$G_{th,2} = \frac{Nw}{l}(\kappa_{eff}t + \kappa_{Si}t_{Si}) \quad (5.21)$$

and is constant until the end of the anisotropic etch step.

5.7.3 Isotropic Etch to Release

The conductance at the beginning of the isotropic process $G_{th,3}$ is equal to $G_{th,2}$, however, as the etch proceeds (Figure 5.2 (d)) the Si under the beams becomes narrower and thinner and the conductance of the structure develops as

$$G_{th,3} = \frac{N}{l}[w\kappa_{eff}t + \kappa_{Si}(w-2ER_{Si}\tau_{iso})(t_{Si}-ER_{Si}\tau_{iso})], \quad (5.22)$$

where t_{iso} is the elapsed time in the isotropic etch step.

5.7.4 Isotropic Overetch

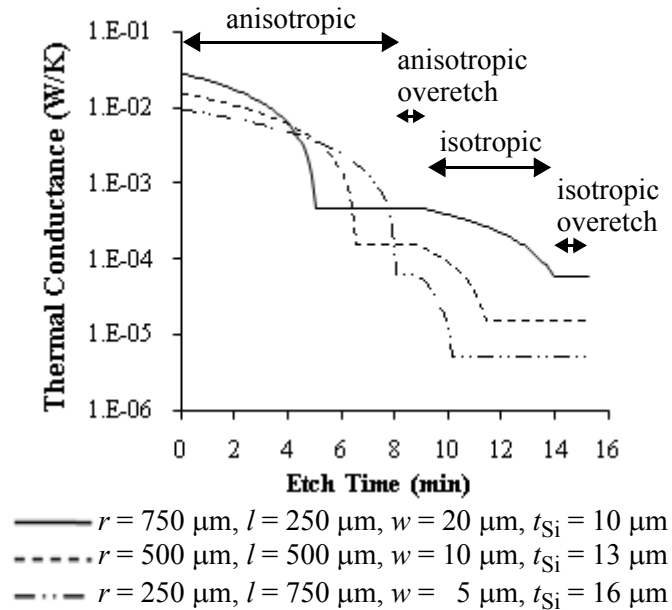
After all the structures are released there is an overetch period (Figure 5.2 (e)) whose duration depends on the uncertainty in the process. The conductance during the over-etch period, provided there is no barrier metal attack, is

$$G_{th,s} = \frac{Nw\kappa_{eff}t}{l}. \quad (5.23)$$

5.7.5 Thermal Conductance Variation During Processing

A plot of the structure conductance over the course of the release etch process, based on the above analysis, is shown in Figure 5.4. A Si etch rate of $ER_{Si} = 33 \text{ nms}^{-1}$ is assumed for the purpose of calculation, so gradients and absolute times are for indication only.

FIGURE 5.4 Graph of the variation in thermal conductance during the release etch process for several different geometries of suspended disc test structure.



5.8 Power Balance for Suspended Disc Test Structures

The two periods of constant conductance, corresponding to the over-etch periods of the anisotropic and isotropic process steps, shown in Figure 5.2 (c) and (e), respectively, are targeted in this study.

Assuming those scenarios, the power balance equation from (5.16) is resolved using expressions for the area parameters specific to the suspended disc test structure.

5.8.1 Anisotropic Overetch Power Balance

Provided the temperature of the structure remains low enough that there is no loss of anisotropy during the over-etch portion of the anisotropic process, ion bombardment is the only contributor to the heat flux into the structure. In this case, for the suspended disc structure, the area parameters from (5.13) and (5.14) become

$$A_p = \pi r^2, \quad (5.24)$$

and

$$A_r = 2\pi r(r + t_{Si}). \quad (5.25)$$

Because there is no Si etching during this period dA_e and hence dP_e are zero.

Substituting (5.24) and (5.25) into (5.13) and (5.14), respectively, into the power balance equation (5.16) gives

$$T^4 - T_0^4 + \frac{N\kappa_{\text{eff}}wt}{2\pi\epsilon\sigma r l(r + t_{Si})}(T - T_a) - \frac{qc_i r V_b (qT_q)^{0.5}}{2\epsilon\sigma(r + t_{Si})} \sum_j \frac{y_{i,j}}{m_{i,j}^{0.5}} = 0, \quad (5.26)$$

which is the form of a quartic equation that can be solved analytically [114].

5.8.2 Isotropic Overetch Power Balance

At the start of the overetch in the isotropic process, the radiating surface area is approximated by (5.25) and the plan view area of the structure is given by (18). The etching surface at the start of the overetch is approximated by

$$A_e = \pi r(r + 2t_{Si}). \quad (5.27)$$

The radiating and etching areas are approximations because the Si under the disc etches laterally and vertically as the suspensions are undercut, however, if $r \gg w/2$ and $t_{\text{Si}} \gg w/2$ then the approximations are valid. The Si etch rate may vary over this area so P_e must be determined by integrating (5.8) over the etching surface. Substituting (5.1) for Si into (5.8) and integrating gives

$$P_e = \int \nu K_1 c_F dA_e, \quad (5.28)$$

where

$$K_1 = AT^{0.5} \exp\left(-\frac{E_A}{k_B T}\right) c_{\text{Si}} \sum_k x_k \Delta H_k \quad (5.29)$$

To proceed, it is assumed that ν , A , E_A and the product mix are constant over the etching surface for all T . These assumptions may not be valid, but no guidance on the variation of these parameters has been found in the literature, so they must suffice for now. Two potential sources of spatial etch rate variation, F concentration c_F and temperature T , suggested by (5.28) are analyzed at this time.

5.8.3 Temperature Variation Within the Suspended Disc

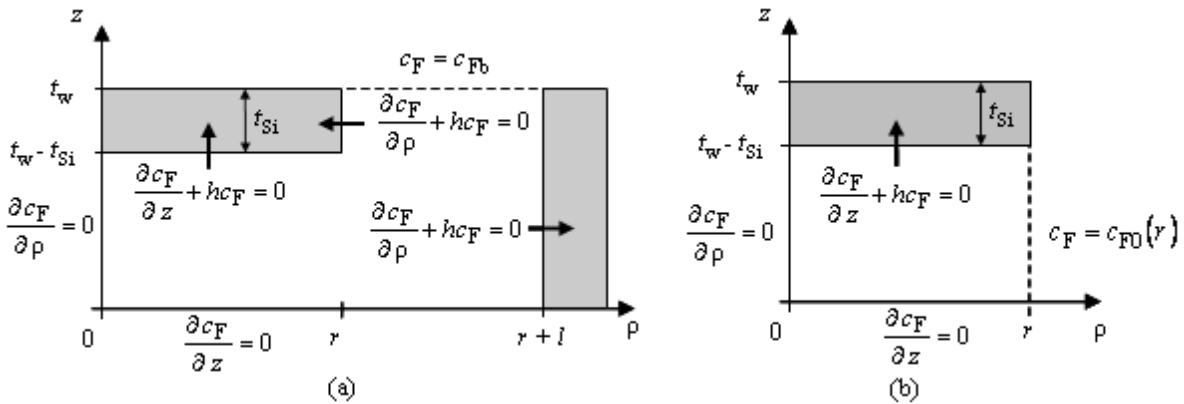
A simple 1-D analysis shows that for the minimum suspension length $l_{\text{min}} = 25 \mu\text{m}$, 94% of the temperature drop in the structure occurs across the suspension and increases to more than 99.99% as r , t_{Si} and l increase and w decreases. The temperature is approximately constant within a suspended disc after the suspensions are undercut and therefore the impact of temperature gradients on cross-disc etch rate variation is negligible.

5.8.4 F Concentration Variation Along the Suspended Disc Sidewall

Analysis of c_F along the sidewalls of the disc and across the underside of the suspended disc structure is more detailed and requires the use of finite element analysis (FEA) and simplified solutions of the diffusion equation to derive functional forms for c_F that relate it to the structure geometry.

An abstracted cross-section of the radially symmetric suspended disc structure is shown in Figure 5.5 (a). The coordinates in the disc reference frame are z , the vertical distance from the bottom of the test structure chip and ρ , the radial distance from the geometric centre of the disc. Solution of the diffusion equation for the region adjacent to the sidewall of the disc leads to solutions containing Bessel functions of the second kind, which are not suitable for inclusion in the following analytic treatment, so the variation in c_F in this region is modeled using a function extracted from FEA data.

FIGURE 5.5 Abstracted cross-section with boundary conditions of the suspended disc test structure for (a) analysis of c_F along the sidewall of the disc and (b) for the analysis of c_F along the underside of the disc.



The boundary conditions of the FEA are given in Figure 5.5 (a). A constant F concentration boundary condition equal to c_{Fb} is applied at the gap between the suspended disc and the anchor, a simplification supported by the neutral transport and concentration data presented in [84] and [95] discussed in Section 5.2. Homogeneous boundary conditions of the third kind are applied at the exposed Si surfaces with the generalized transport coefficient h modeling the flux of F into the Si due to etching. The derivation of h is given below in Section 5.8.5. The symmetry plane at $\rho = 0$ and the surface at $z = 0$ are modeled as insulation with no F flux. A parametric linear solver is used in Comsol Multiphysics[®] (3.5a with Matlab[®]) to solve the system over the geometric parameter space for a range of $T = 300$ K to 450 K. A Comsol script written in Matlab[®] R2008a was used to run the model and iterate over the geometric parameter space. The Matlab[®] script is listed in Appendix D.3.

The extracted data is linear in t_{Si} and T but non-linear in l , with an interaction between l , r and t_{Si} . The l dependence and its interactions are modeled with an aspect ratio ($AR = t_{Si}/l$) factor using the Dushman vacuum correction factor [85] and a loading term comprising the ratio of the suspended disc plan area to the total structure plan area. The F concentration along the sidewall of the disc, from the surface ($z = t_w$) to the bottom of the disc ($z = t_w - t_{Si}$) is modeled using the function

$$c_F = c_{Fb} (1 + C_1 (t_w - z) T) \left[\left(1 + C_2 \frac{t_{Si}}{l} \right) \left(1 + C_3 \left(\frac{r}{r+l} \right)^2 \right) \right]^{-1} \quad (5.30)$$

where C_1 , C_2 and C_3 are fitting parameters. The test function is fitted to the FEA using LSR data using the FindFit function in Mathematica[®]6 where the fitting parameters are $C_1 = 1.897$, $C_2 = 0.245$ and $C_3 = 0.194$. The correlation coefficient R_c^2 for the fit is 0.89. The Mathematica[®]6 notebook used to perform the fit is given in Appendix D.4.

5.8.5 F Concentration Variation Under the Suspended Disc

The problem of solving the diffusion equation for the F concentration under the disc is simplified by approximating $c_F(r, z) = c_F(r, t_{Si}) = c_{F0}(r)$. Given the radial symmetry of the test structure, and assuming the plasma is isotropic, the steady state distribution of c_F is the solution of

$$\frac{\partial^2 c_F}{\partial \rho^2} + \frac{1}{\rho} \frac{\partial c_F}{\partial \rho} + \frac{\partial c_F}{\partial z} = 0. \quad (5.31)$$

The abstracted 2-D space over which c_F is defined ($0 \leq \rho \leq r$ and $0 \leq z \leq t_w - t_{Si}$) is shown in Figure 5.5 (b) along with the conditions at each boundary. The boundary condition of the 3rd kind at $z = t_w - t_{Si}$ links the flux of F into the Si to c_F .

From Fick's Law, Γ_F , the flux of F is related to c_F by

$$\Gamma_F \Big|_{z = t_w - t_{Si}} = -D_{F-Si} \frac{\partial c_F}{\partial z}. \quad (5.32)$$

Assuming SiF_4 is the only etch product

$$\Gamma_{\text{F}} \Big|_{z = t_{\text{w}} - t_{\text{Si}}} = 4\Gamma_{\text{Si}} \quad (5.33)$$

based on reaction stoichiometry, where Γ_{Si} is the flux of Si out of the surface. From (5.1),

$$\Gamma_{\text{Si}} = c_{\text{Si}} ER_{\text{Si}} = A c_{\text{Si}} c_{\text{F}} T^{0.5} \exp\left(-\frac{E_{\text{A}}}{k_{\text{B}} T}\right). \quad (5.34)$$

Substituting (5.34) and (5.33) into (5.32) and rearranging to solve the boundary condition at $z = t_{\text{w}} - t_{\text{Si}}$ yields

$$h = 4c_{\text{Si}} \frac{A}{D_{\text{F-SF}_6}} T^{0.5} \exp\left(-\frac{E_{\text{A}}}{k_{\text{B}} T}\right). \quad (5.35)$$

The general solution of c_{F} under the suspended disk is adapted from Özisik [115]

$$c_{\text{F}}(\rho, z) = \sum_{m=1}^{\infty} c_{\text{F}0} \frac{\cos(\beta_m z) I_0(\beta_m \rho)}{N(\beta_m) I_0(\beta_m r)} \int_0^{t_{\text{w}} - t_{\text{Si}}} \cos(\beta_m z') dz', \quad (5.36)$$

where

$$I_0(x) = 1 + \frac{1}{4}x^2 + \frac{1}{64}x^4 + \frac{1}{2304}x^6 + \text{higher terms} \quad (5.37)$$

is the modified Bessel function of the zeroth order,

$$N(\beta_m) = \left(2 \frac{\beta_m^2 + h^2}{(t_{\text{w}} - t_{\text{Si}})(\beta_m^2 + h^2) + h} \right)^{-1} \quad (5.38)$$

is the norm of the eigenfunction and β_m is the m^{th} eigenvalue and the root of

$$\beta_m \tan[\beta_m(t_{\text{w}} - t_{\text{Si}})] = h. \quad (5.39)$$

The roots of (5.39) are determined using the FindRoot function in Mathematica^{®6} over the temperature range from 300 K to 425 K for each value of t_{Si} (ex. for $t_{Si} = 25$ mm and $T = 425$ K, $\beta_m = 462$, 16,124 and 32,228 m^{-1} , $m = 1, 2, 3$). The Mathematica^{®6} notebook for extracting the eigenvalues is listed in Appendix D.5. Evaluating the integral in (5.36) and substituting (5.37), (5.38) and the roots of (5.39) into the resulting expression, it is found that the 1st order eigenvalue term dominates 99.7% of the solution at a minimum, such that

$$c_F(\rho, t_w - t_{Si}) \approx K_2 c_{F0} \frac{I_0(\beta_1 \rho)}{I_0(\beta_1 r)}, \quad (5.40)$$

where

$$K_2 = \frac{\sin[2\beta_1(t_w - t_{Si})](\beta_1^2 + h^2)}{\beta_1[(t_w - t_{Si})(\beta_1^2 + h^2) + h]}. \quad (5.41)$$

Equation (5.40) is substituted into (5.28) and integrated in cylindrical coordinate space to obtain the etch reaction heat power from the underside of the Si disc:

$$P_{e,underside} = \frac{\nu c_{F0} K_1 K_2}{I_0(\beta_1 r)} \cdot \int_0^{2\pi} \int_0^r \left(1 + \frac{1}{4}(\beta_1 \rho)^2 + \frac{1}{64}(\beta_1 \rho)^4 + \frac{1}{2304}(\beta_1 \rho)^6\right) \rho d\rho d\phi. \quad (5.42)$$

Evaluating (5.30) at $z = t_w - t_{Si}$ to obtain an expression for c_{F0} and substituting this into (5.42) gives

$$P_{e,underside} = \pi \nu c_{Fb} K_1 K_2 r^2 (1 - C_1 t_{Si} T) \left[\left(1 + C_2 \frac{t_{Si}}{l}\right) \left(1 + C_3 \left(\frac{r}{r+l}\right)^2\right) \right]^{-1} \left(1 - \frac{1}{8}(\beta_1 r)^2 + \frac{1}{48}(\beta_1 r)^4 - \frac{1}{288}(\beta_1 r)^6\right) \quad (5.43)$$

The contribution to etch reaction heat from the sidewall of the disc is determined by substituting (5.30) into (5.28),

$$P_{e,\text{sidewall}} = \upsilon c_{\text{Fb}} K_1 r \left[\left(1 + C_2 \frac{t_{\text{Si}}}{l} \right) \left(1 + C_3 \left(\frac{r}{r+l} \right)^2 \right) \right]^{-1} \cdot \int_0^{2\pi} \int_{t_w - t_{\text{Si}}}^{t_w} (1 + C_1(t_w - z)T) dz d\phi, \quad (5.44)$$

which evaluates to

$$P_{e,\text{sidewall}} = 2\pi \upsilon c_{\text{Fb}} K_1 r t_{\text{Si}} \left(1 + \frac{C_1 t_{\text{Si}} T}{2} \right) \left[\left(1 + C_2 \frac{t_{\text{Si}}}{l} \right) \left(1 + C_3 \left(\frac{r}{r+l} \right)^2 \right) \right]^{-1}. \quad (5.45)$$

The total etch reaction power is

$$P_e = P_{e,\text{underside}} + P_{e,\text{sidewall}}. \quad (5.46)$$

The power balance model comprising (5.13), (5.14), (5.15), (5.43) and (5.45) does not have an analytic solution. However, each parameter is known, has been measured, derived or inferred, with the exception of υ . The model contains five independent variables: suspension width w and length l , Si thickness t_{Si} , disc radius r and bias voltage V_b . To determine a value for υ , Mathematica[®]6 is used to fit the model to the experimental data using LSR with υ as the fitting parameter. The Mathematica[®]6 notebook for performing this fit is listed in Appendix D.6. For any given value of υ , the temperature solution T for each set of geometric and process conditions is found iteratively because it depends on the eigenvalues β_m which are dependent on the generalized transport coefficient h which in turn is dependent on T . The convergence tolerance for the solution algorithm is < 0.5 °C. The initialization temperature is 27 °C for all structures. Convergence is achieved within two iterations for most structures and within 15 for all.

5.9 Etch Heating Experiment

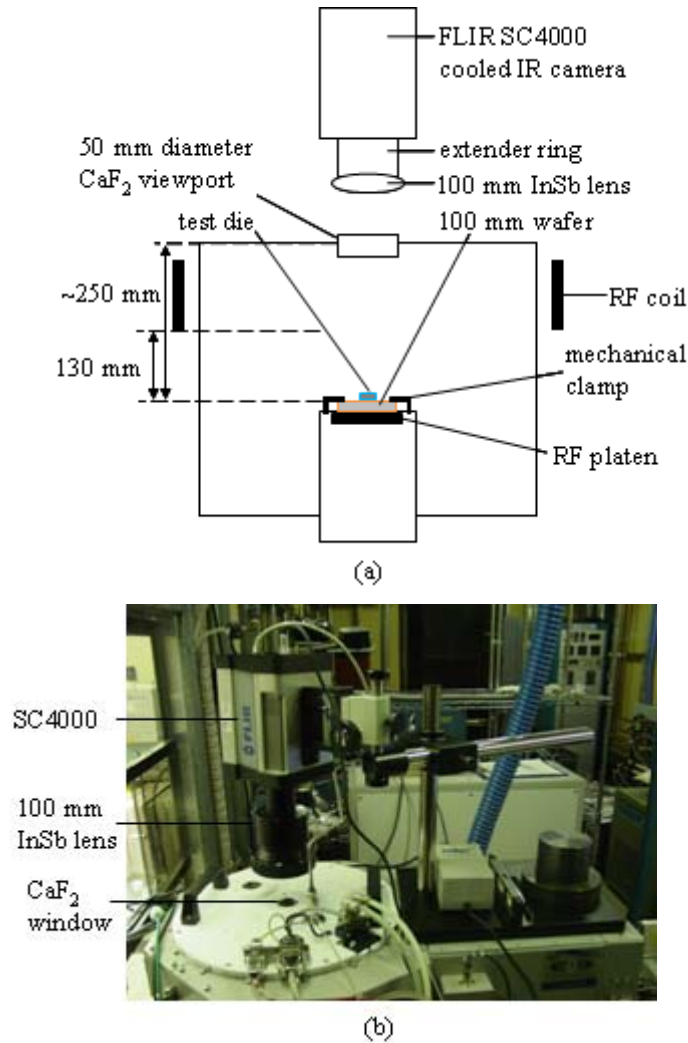
5.9.1 Infrared Camera Configuration

The experimental setup for IR imaging of the suspended disc test structures is shown in Figure 5.6. An SC4000 IR camera from FLIR with InSb lens is used, which is sensitive in the range 3 μm to 5 μm [116]. For valid thermometric measurements, the emissivity ε , the object distance from the lens l_o , the reflected temperature from the object T_{refl} , the ambient temperature T_{amb} , the relative humidity RH of the atmosphere, the temperature of the external optics T_{win} and the transmission τ_{win} of the external optics (i.e. the CaF_2 window) are needed. The system parameters are determined using two different objects on the ICP chamber platen: an oxide coated Si wafer and a test structure chip mounted on an oxide coated Si wafer. The values of these parameters for the test chip setup are given in Table 5.3.

TABLE 5.3 SC4000 IR camera configuration parameters.

Parameter	Value	Units
ε , emissivity	0.95	
l_o , object distance	0.25	m
T_{refl} , reflected temperature	45	$^{\circ}\text{C}$
T_{amb} , ambient temperature	20	$^{\circ}\text{C}$
RH , relative humidity	30	%
T_{win} , CaF2 window temperature	45	$^{\circ}\text{C}$
τ_{win} , CaF2 window transmission	0.95	
Preset frame rate	2	Hz
Preset range 1	10 - 90	$^{\circ}\text{C}$
Preset range 2	50 - 150	$^{\circ}\text{C}$
Preset range 3	150 - 350	$^{\circ}\text{C}$

FIGURE 5.6 Infrared camera setup on plasma etch chamber. (a) Schematic cross-section. (b) Image in service corridor.



A transmission of $\tau_{\text{win}} = 0.95$ is used for the CaF₂ window [117] and it is assumed to have the same temperature as the chamber lid in which it is mounted. The camera is positioned above the ICP viewport in the service corridor of the cleanroom as shown in Figure 5.6 (b). The ambient temperature T_{amb} and humidity RH in this area is controlled to within ± 1 °C and $\pm 3\%$, respectively. With no plasma formed in the chamber it is assumed that the surface temperatures of the wafer and the test chip equals the platen temperature. The SC4000 has a single emissivity value for the object, which comprises all the materials in the field of view. For the test chip setup in this study, the field of view contains the test chip (Al and Si) and the carrier wafer (oxide). A single emissivity value is determined for each calibra-

tion object by adjusting the emissivity until the measured temperature of the surface (Al in the case of the test chips) equals the platen temperature. The emissivity value of $\varepsilon = 0.95$ for the Al surface of the test chips is very high for Al compared to published values [111], but is consistent with the rough, grainy surface of the Al and the darkness of its appearance. A lower value would lead to unrealistically high output temperatures. The reflected temperature T_{refl} is assumed to equal the ICP chamber lid temperature (see Appendix C.2). For both calibration objects, no temperature change was observed when the plasma was turned on so it was concluded that the plasma did not affect the reflected temperature and no adjustment was needed to the transmission value of the external optics.

The parameters in Table 5.3 are used to calculate the structure temperature T according to

$$T = \left(\frac{V_{\text{cam}}}{\varepsilon \sigma \tau_{\text{win}} g_{\text{cam}}} - \left(\frac{1}{\varepsilon} - 1 \right) T_{\text{refl}}^4 - \frac{1}{\varepsilon} \left(\frac{1}{\tau_{\text{win}}} - 1 \right) T_{\text{amb}}^4 \right)^{0.25} \quad (5.47)$$

where V_{cam} is the camera output voltage and g_{cam} is the proprietary camera gain [118].

5.9.2 Etch Heating Test Structure Etch Process

The test chips were etched using the process in Appendix C.2. During each step, the SC4000 captured the IR emissions from the Al surface of the test chips at a frame rate of 2 Hz. The camera and software are able to operate up to 420 Hz, but the data connection used in the setup results in too many dropped frames above 2 Hz. Following the anisotropic process, a 2 min polymer removal process was performed to remove all sidewall inhibitor polymer. This was done to ensure equivalent sidewall conditions on all suspended disc test structures and to avoid convolution of temperature driven loss of selectivity and anisotropy with temperature driven variations in sidewall inhibitor thickness and etch rate. To ensure that all suspended disc test structures were released during the isotropic process, the step was run for ≥ 9 min, even though it resulted in the destruction of many suspended disc test structures. The isotropic process was run at the platen power listed in Appendix C.2 on one set of test die

and at two other platen powers. For each platen power in the isotropic process, the bias voltage V_b was recorded as an experimental variable.

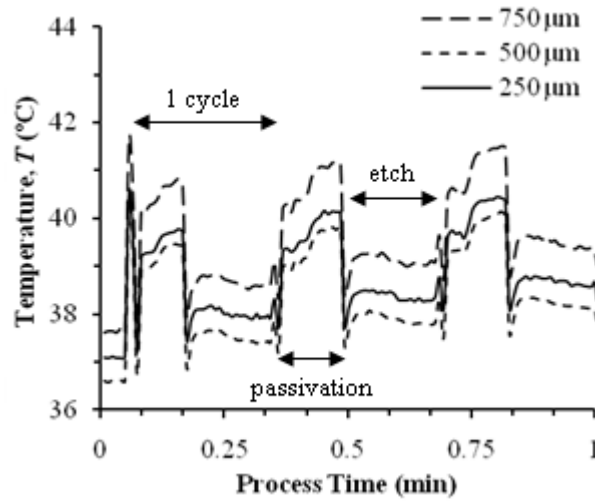
The temperature of a structure during processing is found from the thermometric IR data by defining multi-pixel regions-of-interest (ROIs) on the structure and extracting the pixel-averaged temperature of the area. The temperature difference of a suspended disc, with respect to the anchor, is determined by subtracting the temperature of the anchor of the disc from the disc temperature. The extraction is done for each preset range. The extracted data for each preset range is compiled into a single table and the transitions across the preset ranges are identified to partition the data into a single continuous data set representing the temperatures and temperature differences with respect to the anchor temperature. The PERL (v5.6.1) script used to extract, process and compile the temperature data is listed in Appendix D.2.

5.10 Etch Heating Temperature Profiles

5.10.1 Temperature Profile During Anisotropic Etch

Figure 5.7 shows the measured temperature for a small set of suspended disc test structures during the anisotropic etch process. The temperature difference with respect to the anchor has no distinctive features and is less than 2 °C in all cases. It is postulated that the higher temperature during the passivation step compared to the etch step is caused by the inhibitor species giving up their kinetic energy as they condense on the suspended discs.

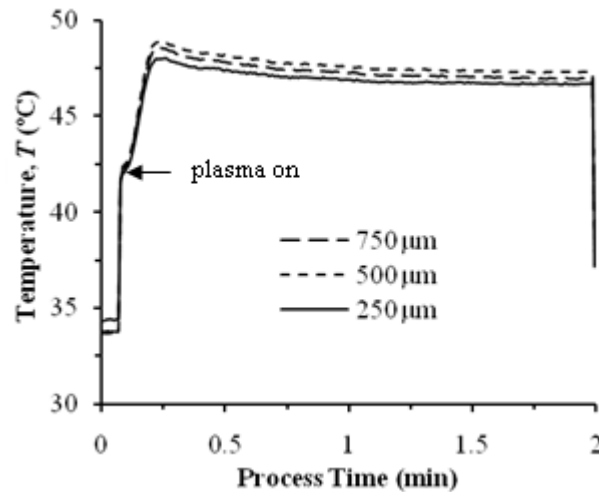
FIGURE 5.7 Temperature profile of a suspended disc test structure during the final three cycles of the anisotropic etch step for various disc radii. Each test structure has a suspension width $w = 10 \mu\text{m}$, length $l = 500 \mu\text{m}$ and a Si thickness $t_{\text{Si}} = 40 \mu\text{m}$.



5.10.2 Temperature Profile During Polymer Removal

The suspended disc temperature during the polymer removal step is shown in Figure 5.8. Similar to the anisotropic process, the temperature difference with respect to the anchor is featureless but less than 1°C . After the plasma turns on in the polymer removal process, there is a rapid rise followed by a gradual decrease in temperature. This may represent the oxidation of the polymer in an exothermic reaction.

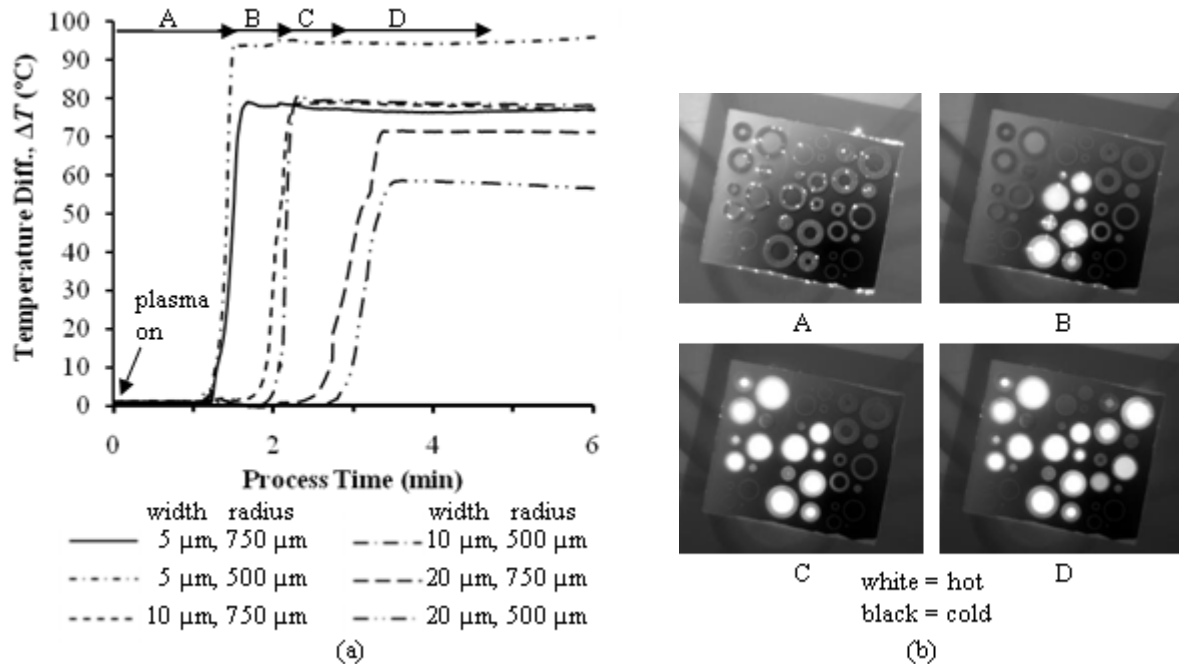
FIGURE 5.8 Graph of the temperature of a subset of suspended disc test structures from a single chip during the polymer removal step for various disc radii. Each test structure has a suspension width $w = 10 \mu\text{m}$, length $l = 500 \mu\text{m}$ and a Si thickness $t_{\text{Si}} = 40 \mu\text{m}$.



5.10.3 Temperature Profile During Isotropic Etch

The measured temperature differences with respect to the anchor during the isotropic etch process, for a representative sample from a single test chip with $t_{Si} = 80 \mu\text{m}$, are shown in Figure 5.9 (a). IR images taken from the chip are shown in Figure 5.9 (b). The images are taken from four different time intervals in the isotropic etch process. In the IR images, the increase in temperature is indicated by a change from black to white. As expected, based on the process schematic in Figure 5.2 (d) and (e), the structures with the narrowest suspensions (i.e. $5 \mu\text{m}$) release first (Figure 5.9 (b) image B) and the structures with the widest suspensions (i.e. $20 \mu\text{m}$) release last (Figure 5.9 (b) image D).

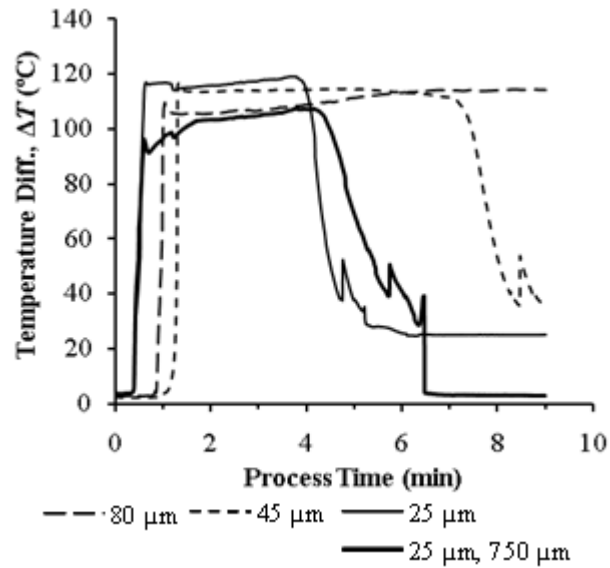
FIGURE 5.9 (a) Graph of the temperature difference ΔT with respect to the anchor for a number of suspended disc test structures of varying dimensions during the isotropic release etch process. The suspension length $l = 500 \mu\text{m}$ and Si thickness $t_{Si} = 80 \mu\text{m}$. (b) A series of IR images of the test structure chip during release etch. White is hot, black is cold.



The graph in Figure 5.10 shows the temperature difference with respect to the anchor from the same structure on three separate chips with different values of t_{Si} . The temperature remains high only while there is Si under the disc. Once the Si is etched away the temperature drops, which occurs earlier in the process for smaller t_{Si} . The temperature drops later in the process on the test structure with the 750 μm radius disc compared to the same thickness disc with 500 μm radius because of variation in

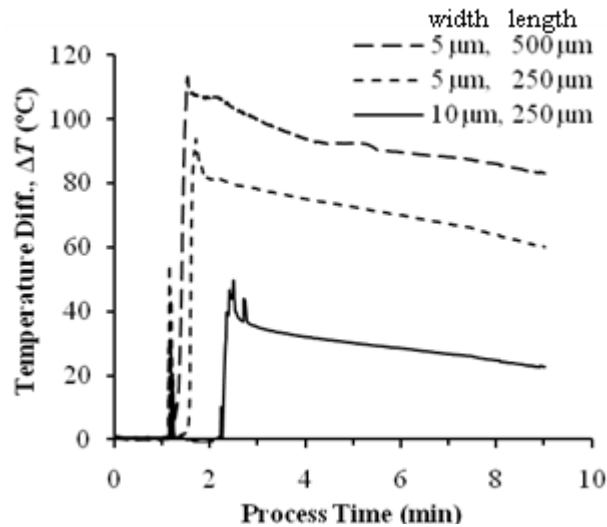
etch rate under the disc due to reactant transport along the underside of the disc. Si remains under the disc at the end of the process for the thickest Si layer (i.e. 80 μm).

FIGURE 5.10 Graph of the temperature difference ΔT with respect to the anchor for a number of suspended disc test structures from chips with varying t_{Si} . The test structures each has a suspension length $l = 500 \mu\text{m}$ and a disc radius $r = 500 \mu\text{m}$, except where indicated. The spikes in the graphs after the temperature drop are artifacts from the transitions between IR camera presets.



The graph in Figure 5.11 shows the temperature difference with respect to the anchor from a single chip, for structures with radius $r = 250 \mu\text{m}$ but different suspension widths and lengths. Figure 5.9, Figure 5.10 and Figure 5.11 illustrate the characteristic types of temperature profile observed throughout the isotropic release etch process. Causes of the different profiles and the data that point to them are discussed in Section 5.10.4.

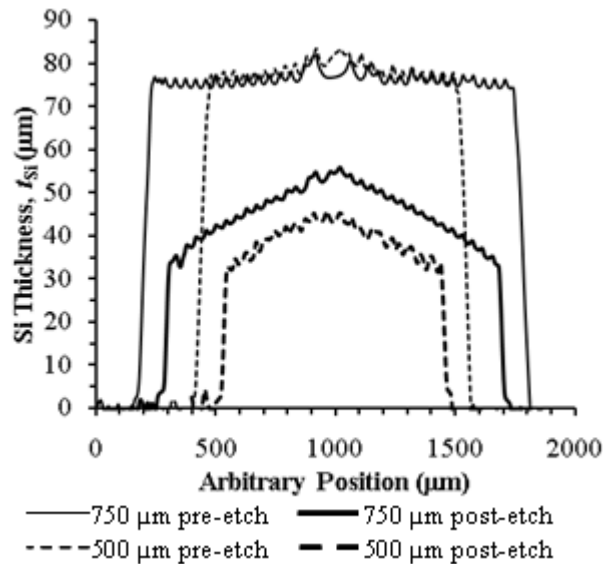
FIGURE 5.11 Graph of the temperature difference ΔT with respect to the anchor for a number of suspended disc test structures of radius $250\ \mu\text{m}$ from a single chip but with varying suspension width and length. The transient spike in the temperature at the time of release is currently unexplained and requires further investigation.



5.10.4 Causes of Variation in Etch Temperature Profile

Following the release process, a subset of the test chips was demounted from the oxide carrier wafer and flipped over to measure the remaining backside Si thickness and the Si and TiW undercuts. Surface profile scans of the Si on the underside of the discs were made after etch using a KLA-Tencor P15 and compared to the surface profile before etch (see Figure 5.12 for comparison of the two discs). The change in the shape of the Si disc from cylindrical before etch to conical after etch is indicative of etch rate variation along the underside of the suspended disc during processing and is attributed to F concentration variation. The Si shapes support the analysis of the source of etch rate variation made in Section 5.8. This evidence coupled with the lack of temperature increase during the anisotropic and polymer removal etch processes, the significant rise in temperature during the isotropic etch process and the significant decrease in temperature as the Si under the discs is etched away (see Figure 5.10) leads to the conclusion that the exothermic reaction heat of the Si-F reaction is the dominant heat source for this chamber and process.

FIGURE 5.12 Surface profile measurements of the Si on the underside of a 750 μm and a 500 μm suspended disc before and after etch. The ripples are the remnants of the sacrificial ARDEM pattern used to improve thickness uniformity over large open areas.

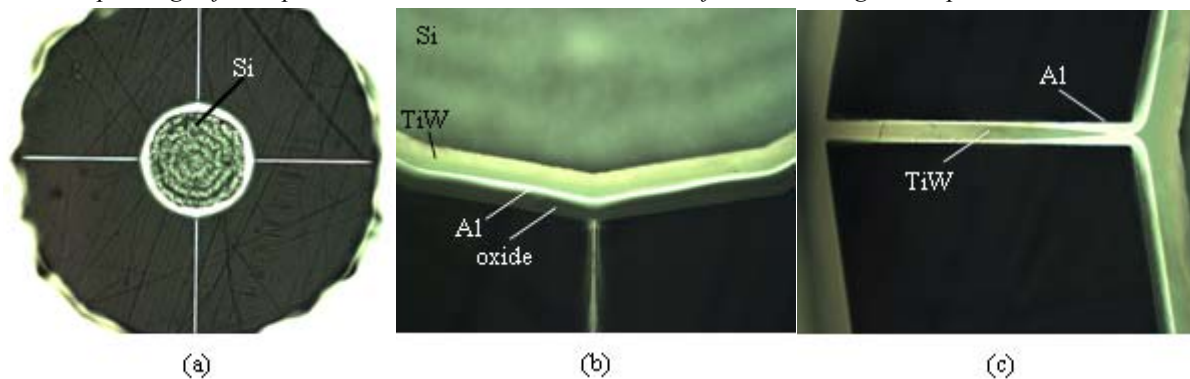


Optical microscope images of the backside of the structures are shown in Figure 5.13. The edge of the remaining Si is not in the same focal plane as the backside of the oxide/TiW/Al discs and the suspensions because of the thickness of the Si and the depth of focus limitation of the microscope. While not accurately measurable, the lateral etching of the Si under the disc is clearly visible. On the disc shown, Si remains at the end of the process, but on other discs and other chips, the Si is completely removed by the end of the isotropic process. In Figure 5.13 (b), the edges of the laterally etched TiW and Si and the unetched oxide are shown. The edge of the Al is not coincident with the edge of the oxide because it is curled up under the action of residual stress. The TiW in the suspension at the anchor side is the full width of the suspension in Figure 5.13 (c) but is laterally etched away completely near the connection to the disc.

The post-etch appearance of the TiW in the suspensions is due to lateral, thermally accelerated etching and loss of selectivity per (5.2). The lateral TiW tapering is a reflection of the temperature gradient along the suspension. Lateral etching of Si and TiW, modulated by the temperature of the suspended structures and dependent on the process conditions and the geometry of the structures are the

cause of the various temperature transients in Figure 5.9, Figure 5.10 and Figure 5.11. The exothermic reaction power input to the structure decreases throughout the process as the surface area of the Si reduces and the distance the F must diffuse to reach the remaining Si increases. At the same time, the thermal conductance is decreasing as the TiW is etched away.

FIGURE 5.13 (a) Optical microscope image of the backside of a suspended disc test structure after release etch. (b) Optical microscope image of the suspension connection to the disc. Due to the magnitude of the TiW undercut and the stress in the Al, the Al is curling up so its edge is not coincident with the edge of the oxide. (c) Optical microscope image of a suspension in which the variable erosion of the TiW along the suspension is visible.



5.11 Temperature Model Compared to Thermometric Data

A series of graphs is shown in Figure 5.14 to Figure 5.18. The graphs are a digest of the complete dataset designed to show the key trends in disc temperature and to demonstrate that the fitted power balance model captures the important qualitative characteristics of the experimental data and is a reasonable first order numerical match to the data. The model is fit to the data using LSR with α as the only fitting parameter. The Mathematica[®]6 notebook for performing this fit is listed in Appendix D.6. The best fit of the model to the data was achieved with $\nu = 0.26$, which resulted in a $R_c^2 = 0.89$.

A consequence of the variation in F concentration along the sidewall and underside of the discs is the maximum in the temperature variation with disc radius. In the model, heat loss by radiation increases at a faster rate than the heat input due to the Si-F reaction and this is reflected in the data for long, narrow suspensions as shown in Figure 5.14. As the suspension decreases in length and increases

in width the overall temperature decreases due to greater conductance and the maximum of temperature shifts to larger radii.

FIGURE 5.14 Variation in suspended disc temperature T as a function of disc radius r for suspensions of various widths w , suspension lengths l of (a) $500\ \mu\text{m}$ and (b) $250\ \mu\text{m}$, both with Si thickness $t_{\text{Si}} = 40\ \mu\text{m}$. The markers represent the measured data and the lines represent the model predictions.

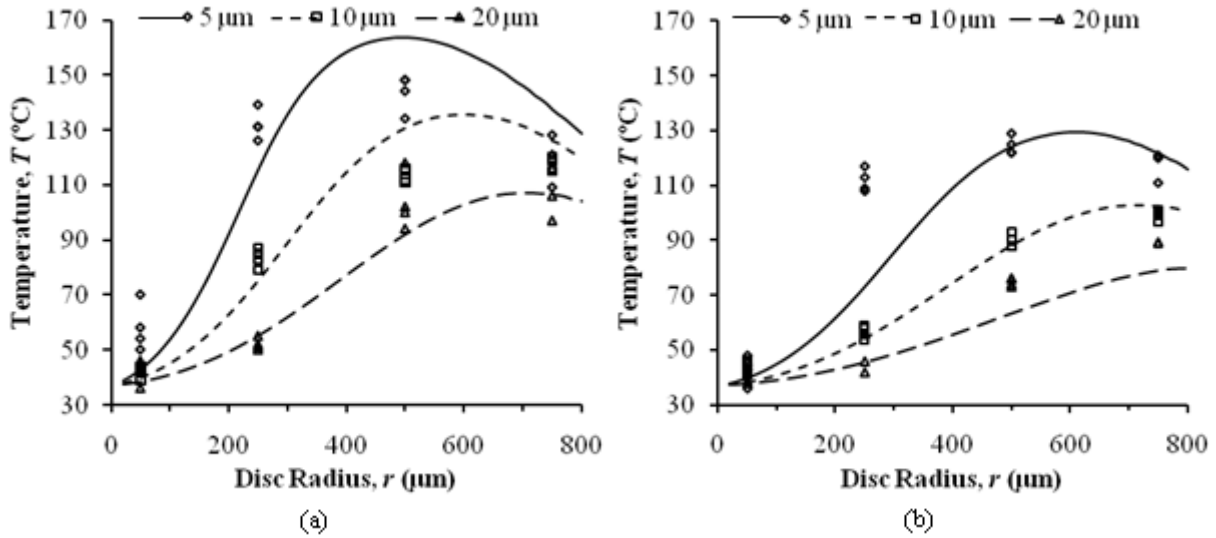


Figure 5.15 and Figure 5.16 show trends of temperature T with suspension length l and width w , respectively. They represent the effect of thermal conduction along the suspension and follow expected trends. For large radius structures, the measured temperature variation with l is non-linear, which is predicted in the model by the interplay of conduction and radiation.

FIGURE 5.15 Variation in suspended disc temperature T as a function of suspension length l for various disc radii r , suspension width $w = 10\ \mu\text{m}$ and Si thickness $t_{\text{Si}} = 40\ \mu\text{m}$. The markers represent the measured data and the lines represent the model predictions.

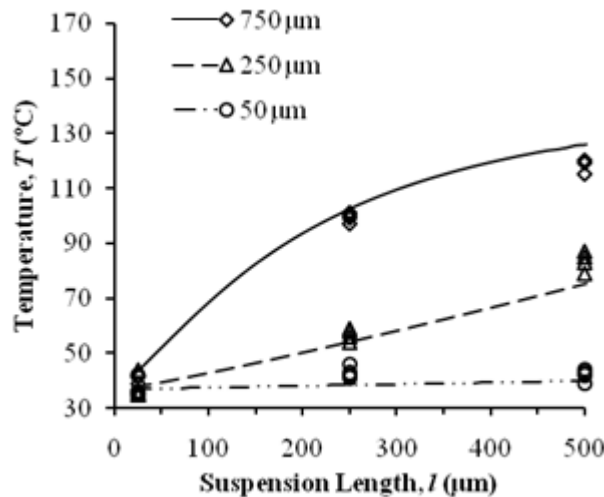
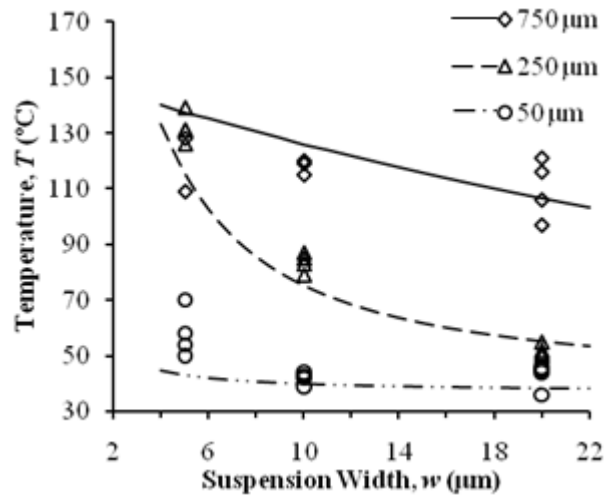


FIGURE 5.16 Variation in suspended disc temperature T as a function of suspension width w for various disc radii r , a suspension length $l = 500 \mu\text{m}$ and Si thickness $t_{\text{Si}} = 40 \mu\text{m}$. The markers represent the measured data and the lines represent the model predictions.



The weakest experimental trends are observed in the temperature variation with bias voltage V_b (Figure 5.17) and Si thickness t_{Si} (Figure 5.18). There is no response of the structure temperature T to V_b across all disc radii. This behavior is consistent across the entire dataset and substantiates the inference of a very low ion flux at the device surface in Section 5.2. The Si thickness has a small impact on structure temperature. There is an obvious model weakness in the prediction of temperature for small values of t_{Si} and small values of r that probably arises from the simplifications needed to model the F concentration along the sidewall and the use of that model in the prediction of F concentration along the underside of the disc.

Across the entire parameter space, the model accuracy ranges from 50% to better than 2%. The errors arise from the estimation of the model coefficients, the simplifications applied in deriving analytic expressions for F concentration, the variations in the temperature profiles of the structures and the extraction of a single characteristic temperature T to represent an evolving thermal profile.

FIGURE 5.17 Variation in suspended disc temperature T as a function of DC bias V_b for various disc radii r , suspension length $l = 500 \mu\text{m}$, width $w = 10 \mu\text{m}$ and Si thickness $t_{\text{Si}} = 40 \mu\text{m}$. The markers represent the measured data and the lines represent the model predictions.

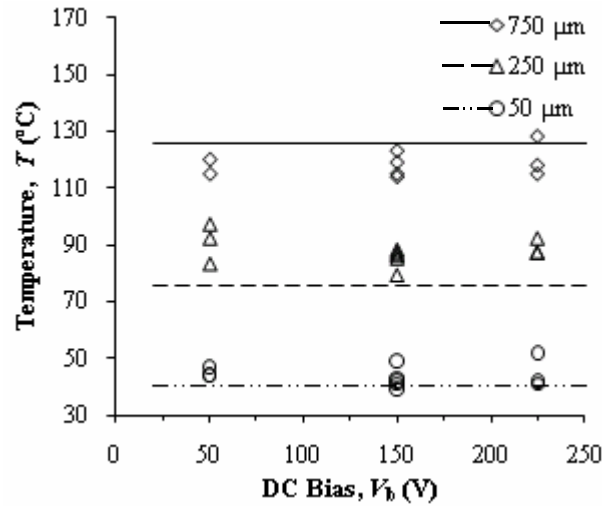
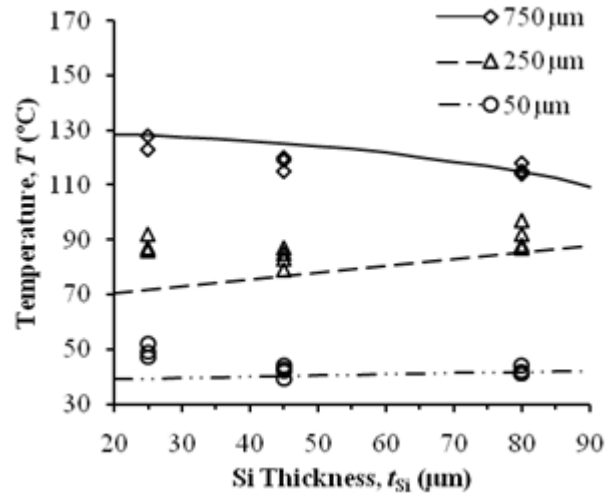


FIGURE 5.18 Variation in suspended disc temperature T as a function of Si thickness t_{Si} for various disc radii r and a suspension length $l = 500 \mu\text{m}$ and width $w = 10 \mu\text{m}$. The markers represent the measured data and the lines represent the model predictions.



5.12 Impact of Etch Heating Model

5.12.1 Relevance to Other Processes and Chamber Types

The dominant cause of undesired temperature increases in suspended microstructures during Si release etch is the exothermic heat of reaction of Si and F in the formation of SiF_4 and SiF_2 . Temperature increases during the anisotropic part of the release etch process are negligible. These results are

shown for a Bosch-type process in a commercially available ICP etcher by measuring suspended microstructure temperatures using *in situ* thermometric IR imaging, analyzing the variation in temperature profiles throughout the process and fitting an analytic model to the data. The conclusion is valid for the process chemistry, process regime and chamber type described in this paper but must be validated for other chamber types, chemistries and regimes. For example, in an ICP etcher in which the wafer is much closer to the plasma generation region than the 130 mm of the tool used here, the ion density could be two to three orders of magnitude higher than inferred for this analysis and the contribution of ion bombardment to suspended microstructure temperature increases could predominate. In such a case, the temperature rise during the anisotropic part of the process may become significant. In that respect, the conclusions of this work can be applied only narrowly to a small set of etch process chambers.

5.12.2 Scope of Power Balance Model

The power balance model includes heating by reaction heat and ion bombardment and cooling by conduction through the solid suspension and by radiation to the reactor body. Thermal conduction is the main cooling mechanism for small structures with wide, short suspensions while radiation increases in significance as the suspensions narrow and lengthen and the surface area of the structure increases. The trend of decreasing structure temperature with increasing structure area above a certain critical dimension is captured in the model by vacuum conductance limited F concentration variation along the sidewalls and underside of the structures. In effect, as structures increase in area, the volume of Si reacting per unit time does not increase as fast as the radiating surface area.

The power balance model explains 89% of the variation seen in the measured data using the reaction heat absorption coefficient $\nu = 0.26$ as the fitting parameter. This work is thought to be the first time that the reaction heat absorption coefficient has been quantified and it serves as a "stake in the ground" for future refinement and understanding of this parameter. The model fits the suspended

microstructure temperatures with an accuracy from 2% to 50%, depending on the radius of the disc and the conductance of the suspension. Agreement between model and experiment improves when solid conductance dominates the heat loss mechanism and the disc temperatures are low. This suggests that more work is needed to identify the exact reaction product mix, its temperature variation and the temperature and product dependence of ν .

5.12.3 Implications for Device Design and Process Choice

The power balance model, and the means by which it is built up, provide to the microsystem design and processing community a degree of insight into the mechanisms of selectivity and anisotropy loss during the critical process step of microstructure release etch. Trade-offs in the size of a suspended structure, the amount of thermal isolation and the etch rate are brought to light that were previously appreciated only intuitively. For example, design rules can be developed using the power balance model to provide a maximum limit on thermal isolation for a given size structure, but, if a large structure must be highly thermally isolated, the process developer is guided to reduce the etch rate significantly.

5.12.4 Directions for Further Research

In developing the model, many inferences are needed to quantify the model coefficients and simplistic approximations are made in the derivation of the F concentration variation along the structures. Much refinement is possible by researchers with the equipment and know-how to measure ion flux, electron temperature, plasma temperature, F concentration, product composition, etc. directly and feed these accurately measured values back in to the model to truly test its validity. The variety of microstructures, device topologies and fabrication technologies ensures that the evolution of thermal isolation during processing will continue to be an area of concern and of fruitful research in the design of reliable, manufacturable devices.

The propensity of the microsystems researcher to exploit secondary etch effects leads one to envision a scenario in which selective structure heating during release etch is used to achieve desirable process outcomes that are currently impractical to achieve by conventional means. To make use of the effect in a predictable and scientifically repeatable way, the power balance model needs to be refined, the fixed inputs to the model must be determined with greater accuracy and the variations in etchant concentration, species mix and temperature across the etching structure must be modelled more exactly. In the final case, an iterative, coupled FEA model would seem to provide the only means by which these parameters can be calculated to the required degree of accuracy.

6

Device Characterization

“A man who carries a cat by the tail learns something he can learn in no other way.”

- Mark Twain

The moment of truth in the life cycle of a MEMS device arrives when the voltage is applied to the terminals and the output is measured and compared with theory. It is often an occasion to ponder what more needs to be understood about the physics of the device for the theoretical models to be representative of the observations. But when the device doesn't perform as expected, the lack of match between theory and experiment may be due to a divergence in the assumed and actual values of a parameter, such as a geometric dimension or a material property. Thus, in characterizing MEMS devices and validating theoretical models, it is insufficient to measure the performance of the device alone; the parameters that populate the models must be known with reasonable accuracy.

With CMOS-MEMS and its variants the reality must be faced that while the semiconductor foundry processes used to fabricate the devices are stable and robust, the properties controlled for in the production environment are those that directly impact the electrical performance of the device and hence its production yield [119]. Semiconductor process integration engineers, whose responsibility it is to ensure that the performance of the finished devices adhere to specification, monitor many end-of-line parameters, some of which have conflicting requirements (like power and speed), but few of the parameters they monitor are mechanical, and therein lies the rub.

The clearest example in this chapter of a CMOS parameter not controlled for mechanical performance is the variation of the thickness of the CMOS interconnect and the relative proportions of the Al and barrier metal layers in the interconnect stack. From an electrical perspective, the resistance of an interconnect layer is important. However, the elastic modulus of Al and common barrier metals such as TiW and TiN are very different and their proportions directly impact the spring constant of suspensions and the mechanical behavior of the MEMS device they suspend.

To address the issues described above, this chapter first covers characterization of the geometric parameters and material properties of the theoretical models. The data is presented, where appropriate, in the form of Shewart charts which graphically represent the stability of a process with respect to its historical or desired behavior [120]. In this chapter, the mean and 3σ control limits of the Shewart charts are based only on historical data and the assumption of a stable state of control in which only common causes of variation are present (i.e. the measured data represents the normal variation of a stable process). Shewart charts are used in this dissertation to frame the issue of control of MEMS performance in a semiconductor foundry technology. Electrothermomechanical response of actuator test structures is characterized and finally micromirror device performance. The measured variation in model parameters is used to predict the expected variation of the fabricated micromirror arrays.

6.1 Measurement Summary

Table 6.1 summarizes the parameters measured in this work, the measurement methods and equipment and the precision of the measurement. All measurements are made after the Si release etch process and hence represent variations intrinsic in the CMOS foundry process coupled with variation introduced by the post-CMOS processing of the MEMS device. Where these two sources of variation can be separated the magnitudes of the respective effects are described. Where they cannot be separated, a single value is given.

TABLE 6.1 Method of measuring the parameters presented in this chapter and their precision.

Measured Parameter	Measurement Method	Equipment	Precision
Layer thickness t_i	FIB image with offboard software calibrated against profilometer	FEI Sirion SEM	10 nm
Beam width w_b	SEM image analysis	FEI Sirion SEM	10 nm
CD bias Δw	SEM image analysis	FEI Sirion SEM	10 nm
Beam length l_b	SEM image analysis	FEI Sirion SEM	100 nm
Spring constant k_z	Gradient of linear fit to Triboin-denter force vs. displacement data	Hysitron TI 900	5%
Young's modulus E	Matrix inversion of geometric parameters and spring constants	Hysitron TI 900	2 GPa
Radius of curvature ρ_b	White light interferometry	WYKO NT 3300	25 μm
Lateral curl y_{sa}	SEM image	FEI Sirion SEM	10 nm
Thermal sensitivity γ	White light interferometry with heated stage	WYKO NT 3300	$\text{m}^{-1}\text{K}^{-1}$
Electrothermal mirror scan angle θ_m	Laser reflectance projected onto translucent screen	Optical bench and HeNe laser	1°
Mirror rest angle	White light interferometry	WYKO NT 3300	0.1°
Mirror radius of curvature	White light interferometry	WYKO NT 3300	0.01m
Mirror smoothness Ra	White light interferometry	WYKO NT 3300	1 nm
Thermal cross-talk	White light interferometry	WYKO NT 3300	10 ppm
1st mechanical mode frequency f_1	Image processed stroboscopy	Microvision	20 Hz
Thermal cutoff frequency $f_{c,th}$	Image processed stroboscopy	Microvision	10 Hz

6.2 Foundry CMOS Layer Thickness

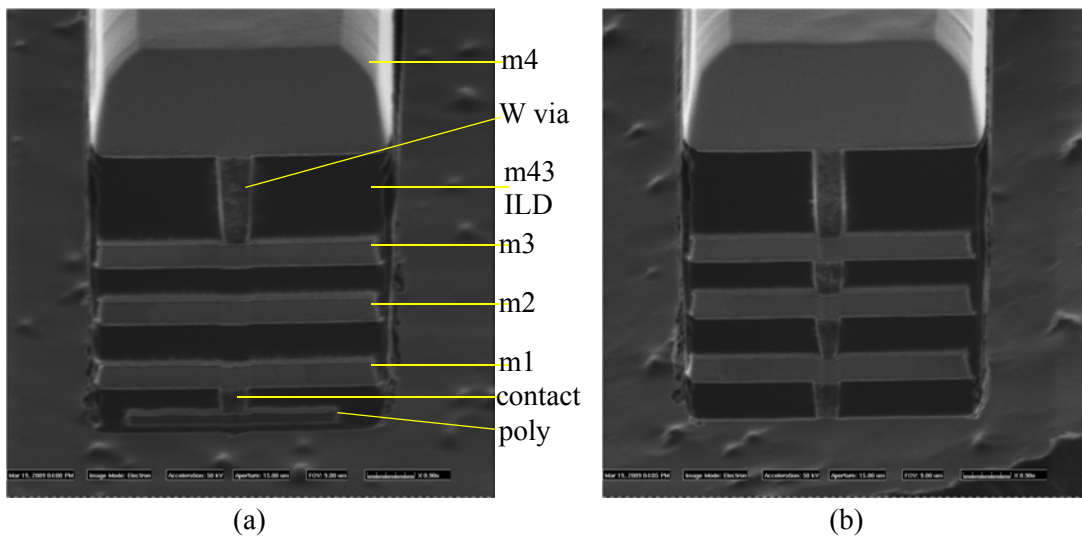
The mechanical properties of MEMS devices depend on the properties of the materials they are made of and the dimensions of the structures. CMOS-MEMS are made of the metal interconnect layers and the ILD layers of foundry CMOS but their thicknesses are not typically provided to customers on a run-to-run basis so they must be measured for each foundry run.

6.2.1 Thickness Measurement Method

The thickness of the foundry CMOS layers are measured from FIB images like those shown in Figure 6.1. A set of beams {m4321pf, m321pf, m4321a and m321a}, all with every via layer, are measured on a profilometer to determine the height difference between pairs of beams on the same base oxide, field or gate. These height differences are used to “calibrate” the measurement of the individual layer thicknesses of the beams.

To achieve a successful profilometer measurement the following conditions are required: 1. the beams are nominally 50 μm long so a single scan line can be defined that passes over each beam but the difference in the vertical curl of the released beams is negligible, 2. 4 μm wide beams so the beam has a flat top (n.b. the chamfering of the top metal in Figure 6.1) that is observable at low image zoom, and 3. a 20 μm separation between beams so the profilometer probe tip touches down on exposed Si between the beams. A single vertical FIB cut is done at the free end of the beam with a 250 μm to 400 μm aperture. The beam is tilted to 45° and imaged continuously with a 50 μm to 75 μm aperture for several minutes to delineate the different material layers as each mills at a different rate.

FIGURE 6.1 FIB images of m4321 beams on (a) field oxide and (b) active area. The beam in (a) has an internal poly layer.



6.2.2 Foundry CMOS Thickness Trends

A summary of the layer thicknesses and their variation is given in Table 6.2 and the trends in layer thickness data extracted from the beams in Figure 6.1 are shown in Figure 6.2 to Figure 6.4. The reader should note that the chips used for thickness extraction are selected randomly, without knowledge of the region of the wafer they are taken from. For this reason, it is possible that the variations documented here are actually cross-wafer variations and not run-to-run variations. The nominal thicknesses of the layers are not provided due to a confidentiality agreement with the foundry however the difference between nominal ILD thickness and actual thickness is up to 30% of nominal, while interconnects are ~15% different than nominal. The 10 nm error in layer thickness listed in Table 6.1 arises from the uncertainty in identifying the boundary between different layers. The poly thickness comprises silicided and unsilicided poly but the delineation of the two materials is not distinct enough to separate the quantity into two values.

The impact of geometric variation in the layers of MEMS structures has design significance. When coupled with the variation in parameters such as the modulus, density, thermal conductivity and CTE, the impact on the speed and performance of the device can be quantified. This data makes the case that a MEMS design process can be implemented for a foundry technology only after the actual values of the geometric parameters and the thermal and mechanical properties of the materials are established and that each run must be characterized to ensure valid input to analytic and simulated models.

TABLE 6.2 Mean μ and standard deviation σ of measured JAZZ layer thicknesses across multiple runs. The nominal thicknesses are not provided due to a confidentiality agreement

Parameter	Mean μ (nm)	Std. deviation σ (nm)	Number of Runs
m4 layer	2730	60	5
m4 Al	2630	60	5
m4 bottom TiW	100	20	5
m43 ILD	2030	40	5
m3 layer	690	20	5
m3 top TiW	120	20	5

Parameter	Mean μ (nm)	Std. deviation σ (nm)	Number of Runs
m3 Al	490	30	5
m3 bottom TiW	80	20	7
m3 Al loss	110	40	4
m3 Al top metal	390	50	5
m32 ILD	680	50	7
m2 layer	730	40	7
m2 top TiW	140	30	7
m2 Al	510	20	7
m2 bottom TiW	80	20	7
m21 ILD	800	110	7
m1 layer	690	30	7
m1 top TiW	120	20	7
m1 Al	490	20	7
m1 bottom TiW	80	20	7
m1p ILD on field	510	20	3
silicided poly	380	10	3
m1Si ILD on active	1000	40	5
m1Si ILD on field	1100	50	4
pSi ILD on field	220	20	3

FIGURE 6.2 Metal layer thickness trends across several JAZZ runs in comparison with the mean of the dataset, the $\pm 3\sigma$ limits and the nominal target for the parameter. (a) m4 layer thickness. (b) m3, m2 and m1 layer thicknesses. Error bars are set to the values listed in Table 6.1.

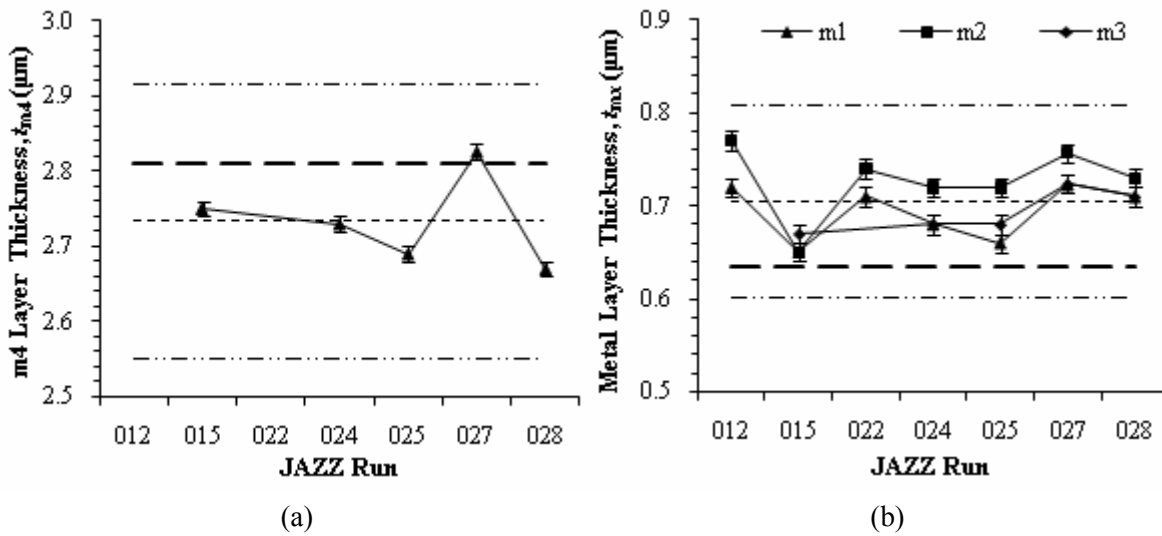


FIGURE 6.3 ILD layer thickness trends across several JAZZ runs. (a) m43 layer thickness. (b) m32 and m21 layer thicknesses. Error bars are set to the values listed in Table 6.1.

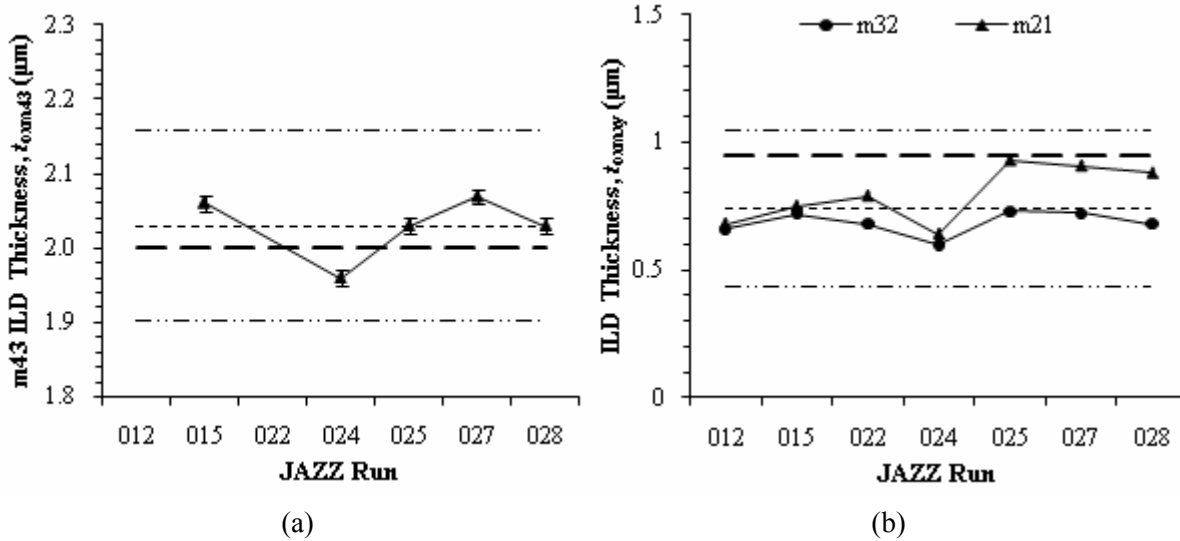
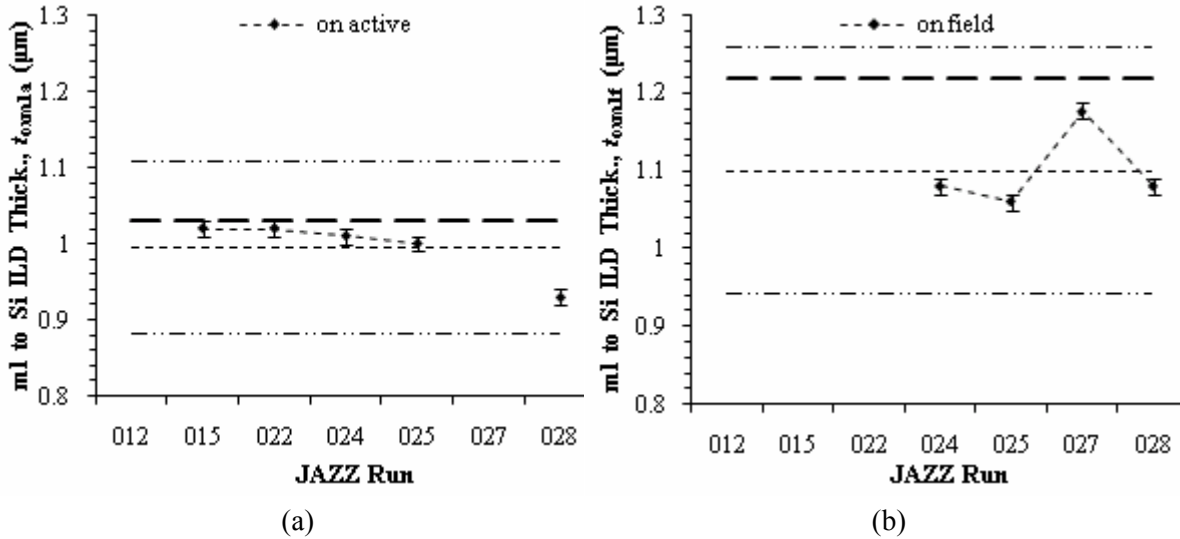


FIGURE 6.4 m1 to Si layer thickness on (a) active area and (b) field oxide. Error bars values given in Table 6.1.

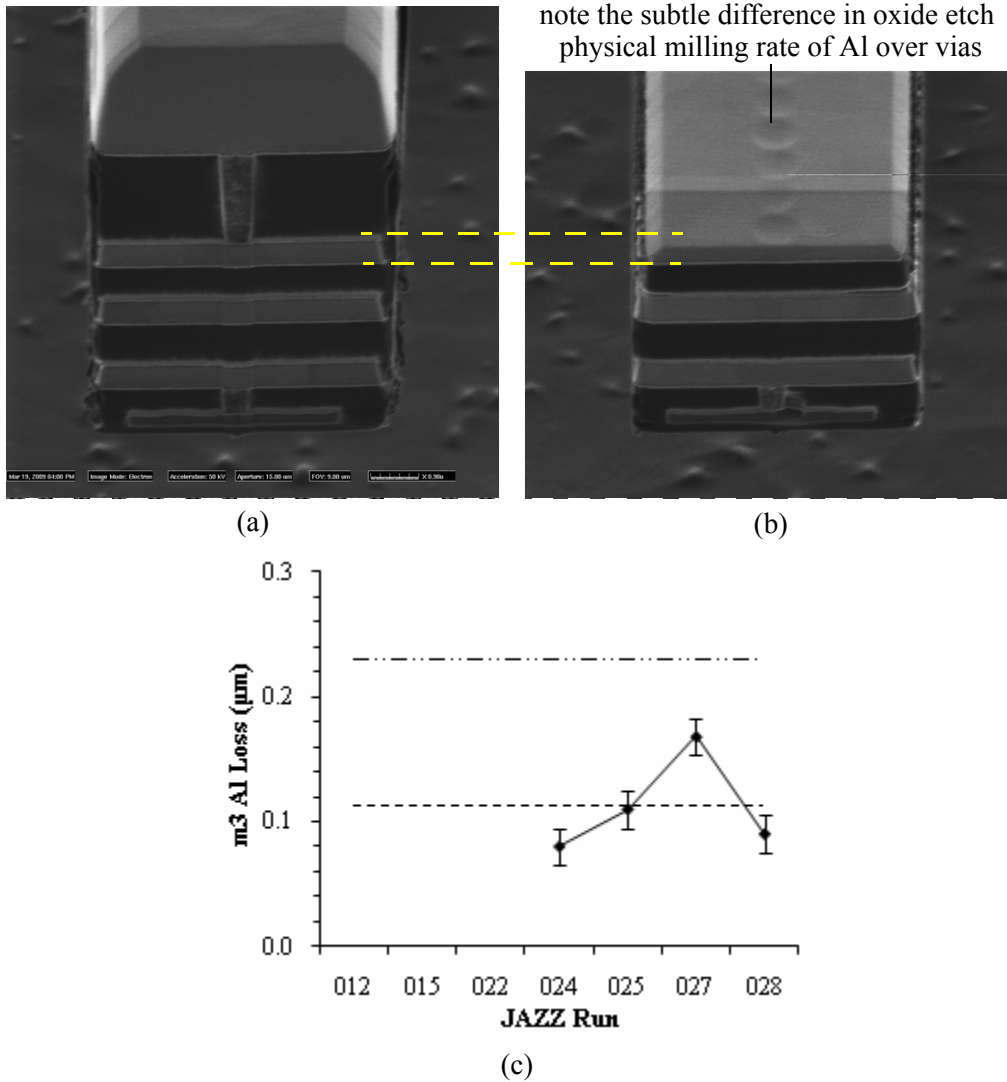


6.2.3 Frontside Oxide Etch Metal Erosion

The values quoted in this section are taken after frontside oxide etch and Si release etch. The impact of this is most noticeable in the thickness of the m3 Al when it is the top metal in a stack. The frontside oxide etch process in Appendix C.3 has a large physical etching component. The top TiW of the m3 layer is etched away during the frontside oxide etch on m3* beams and the Al layer is milled as shown

in Figure 6.5. The variations intrinsic to the foundry CMOS process are convolved with variations introduced by the post-CMOS process. The graph of m3 loss shown in Figure 6.5 highlights this point.

FIGURE 6.5 *m3* layer Al loss on *m3** beams. (a) *m4321pf* beam and (b) *m321pf* beam at equal magnification. (c) Graph of the trend in *m3* Al loss over a number of JAZZ runs. Error bars set to the values listed in Table 6.1.



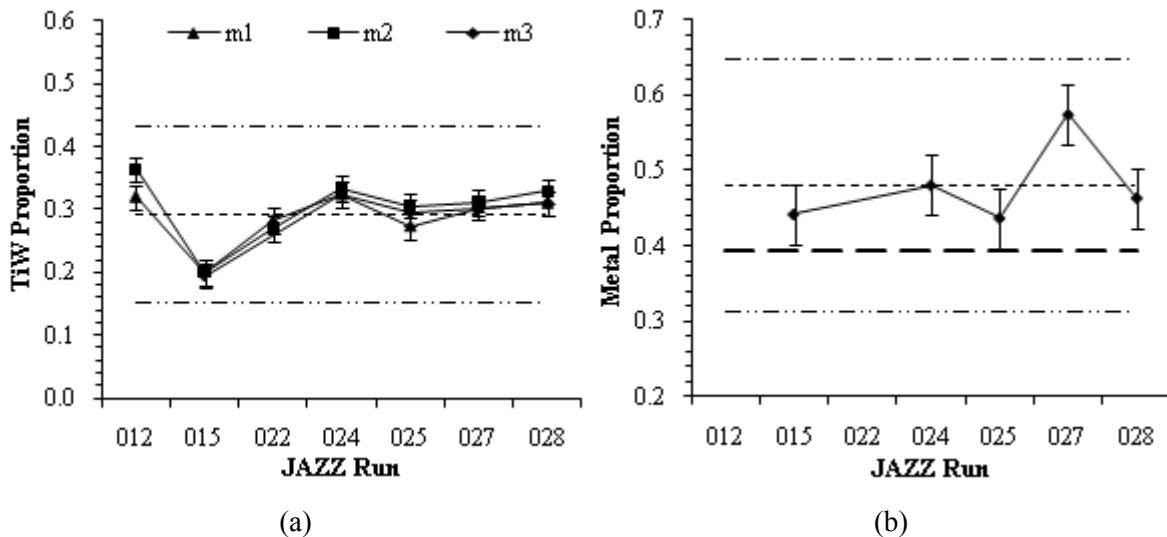
The *m4* Al displays significant chamfering due to milling and while the difference between the nominal and measured values of the *m4* layer can't be taken as representative of the Al loss, it is likely that the Al loss is at least as great as the *m3* Al loss, and is likely much greater. It is not known if the top TiW of *m2** and *m1** beams are etched away completely by the frontside oxide etch process but they are not present after the Si release etch. However, the Al layers do not have a measurable thick-

ness loss, so it is likely that the top TiW layers survive the frontside oxide etch but are then etched chemically in the Si release etch process.

6.2.4 Metal Proportions in Beams

The composition of each interconnect layer varies significantly from run to run. The top and bottom TiW layers and the Al vary in thickness. TiW has a higher modulus than Al so the proportion of TiW in the metal stack impacts the effective modulus of the metal layers. The trend of the TiW proportion of the metal layers is shown in Figure 6.6 (a) and varies from a minimum of 19% to a maximum of 36%. The trend in the total proportion of metal in the beam is shown in Figure 6.6 (b) and varies over a 14% range. The potential impact of the variation in metal layer composition and total proportion of metal in a beam is discussed in Section 6.4 when its impact on effective beam stiffness is analyzed.

FIGURE 6.6 Trends in the proportion of (a) TiW in each metal layer and (b) the metal in a m321a beam.



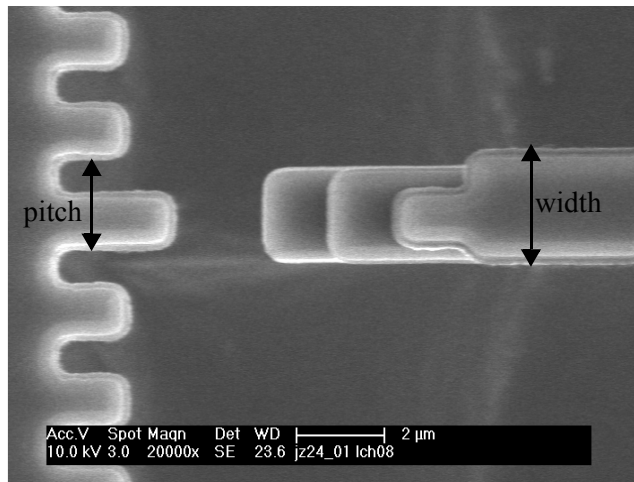
6.3 Beam Dimensions

The dimensions of a beam can differ from layout dimensions due to foundry variation and post-processing variation. This sub-section discusses the measurement of beam dimensions and assesses the difference between layout and on-chip dimensions.

6.3.1 Beam Width and Length

The width w_b and length l_b of each beam are measured using SEM, or FIB, by manually placing cursors on the edges of the structure under test (SUT) like the one shown in Figure 6.7. A pitch measurement is made prior to each width measurement and is used to gauge the error in the SEM itself. This error is reduced to less than 1% before structure dimensions are measured. The dominant error in SEM thickness and length measurements originates in the tilt and rotation of the SUT and the placement of the measurement cursors. These are reduced by adjusting the SEM stage tilt and rotation until symmetry in the left and right (or top and bottom) edge widths is achieved, or by making a differential measurement. The beams being measured typically have $l_b > 25 \mu\text{m}$, the length variation is insignificant compared to the length of the beam and is not presented here.

FIGURE 6.7 *Beam width and pitch measurement structure.*



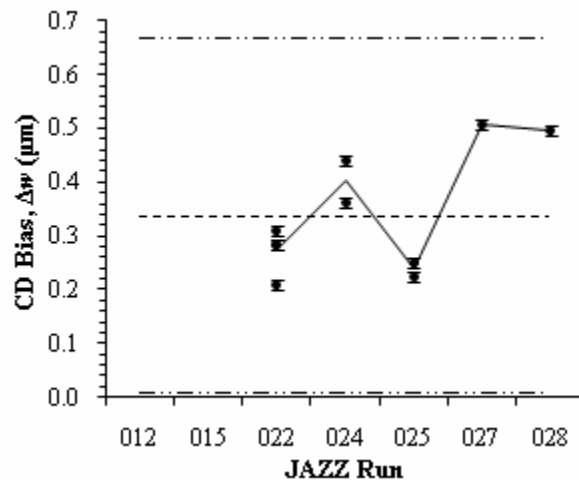
6.3.2 Critical Dimension Bias

The width of a processed structure like a beam is not the same as the layout width due to “process bias”. Process bias during CMOS fabrication introduces a statistically consistent difference at photolithography and etching steps, typically, that can be tuned in the case of performance critical structures like gates, or is allowed to “float”, uncorrected, in the case of structures like power lines. The post-CMOS process introduces bias during frontside oxide removal due to ion milling and ion deflection. In the case of ion milling, the top metal layer is chamfered (see Figure 6.1 and Figure 6.5) and any loss of

verticality in the sidewalls of the metal are transferred into the underlying oxides to an extent dependent on the selectivity of the process to the oxide. It is also possible, when the metals underlying the top metals are slightly misaligned that their exposed edges mask the underlying oxide and increase the beam width, while the metal is milled, slightly reducing the internal metal layer width.

To establish the process bias on a run-to-run basis the width of a number of m321a beams of varying layout dimension are measured using an SEM and their difference to layout is calculated. The resulting mean bias values for each chip are plotted in Figure 6.8. The run-to-run variation is larger than the within-run variation. Further investigation is needed to determine if the run-to-run variation is due to the foundry process or the post-processing.

FIGURE 6.8 *CD bias for m3*a beams across several JAZZ runs in comparison with the mean of the dataset and the $\pm 3\sigma$ limits. Error bars are set to the value listed in Table 6.1.*



6.4 Young's Modulus and Beam Stiffness

The Young's modulus of the oxide, metal stack and poly is determined by measuring the spring constant k_z of cantilever beams of varying composition with a nanoindenter [121] and performing a matrix inversion on the data. The extracted Young's modulus depends on parameters (i.e. spring constant, layer thicknesses, beam width and beam length) that are measured directly, in contrast to resonant beam methods which require the material densities to be inferred [122].

6.4.1 Spring Constant Matrix

The spring constant of a multimorph cantilever for out-of-plane bending is

$$k_z = \frac{3(EI)_{\text{eff},y}}{l_b^3}, \quad (6.1)$$

which, for the j^{th} beam with members of constant width w_b , is re-expressed as

$$k_{z,j} = \frac{3w_{b,j}}{l_{b,j}^3} \int_0^t E_j z_{b,j}^2 dz_{b,j}. \quad (6.2)$$

In its multimorph form, transformed to the beam coordinate system, (6.2) is re-expressed as

$$k_{z,j} = \frac{3w_{b,j}}{l_{b,j}^3} \sum_{\text{members}} \int_{z_{b,ij}}^{z_{b,ij} + \Delta z_{ij}} E_{ij} z_{b,ij}^2 dz_{b,ij}. \quad (6.3)$$

Evaluating the integral for a single beam member leads to the expression of its unique contribution to the spring constant in (6.3):

$$\left[\frac{3w_{b,j}}{l_{b,j}^3} \left((z_{b,ij} - z_{c,j}) \Delta z_{ij}^2 + (z_{b,ij} - z_{c,j})^2 \Delta z_{ij} + \frac{\Delta z_{ij}^3}{3} \right) \right] E_{ij} = T_{ij} E_{ij}. \quad (6.4)$$

There are $m = 4$ multimorph materials in the JAZZ Semiconductor 0.35 mm foundry process are oxide, Al, TiW and poly. Assuming uniform properties for each material, the contribution to $k_{z,j}$ by members of similar materials are grouped together, such that for a cantilever beam in this technology

$$k_{z,j} = E_{\text{ox}} \sum_{\text{oxide members}} T_{ij} + E_{\text{Al}} \sum_{\text{Al members}} T_{ij} + E_{\text{TiW}} \sum_{\text{TiW members}} T_{ij} + E_{\text{poly}} \sum_{\text{poly members}} T_{ij}. \quad (6.5)$$

The coefficient of the Young's modulus terms in (6.5) are replaced by $T_{\text{mat},j}$ to give

$$k_{z,j} = T_{\text{ox},j} E_{\text{ox}} + T_{\text{Al},j} E_{\text{Al}} + T_{\text{TiW},j} E_{\text{TiW}} + T_{\text{poly},j} E_{\text{poly}}, \quad (6.6)$$

which in matrix form is

$$\mathbf{k}_z = \mathbf{T}\mathbf{E}. \quad (6.7)$$

For an array of $N = n_m$ cantilevers, where n_m is the number of possible materials in the beam, (6.7) is solved by matrix inversion. In the case that $N > n_m$ cantilevers, (6.7) is overdetermined and is solved using the pseudoinverse [123]:

$$\mathbf{E} = (\mathbf{T}^T \mathbf{T})^{-1} \mathbf{T}^T \mathbf{k}_z. \quad (6.8)$$

\mathbf{E} is found iteratively because the position of the neutral axis z_c in (6.4) is dependent on E_{ox} , E_{Al} , E_{TiW} and E_{poly} . The model is initialized with a value of $E_i = 70$ GPa for all i and is run until convergence to less than 0.1 GPa is achieved.

For the SOI-CMOS-MEMS process described herein, it is felt the poly layer sidewalls cannot be exposed to the frontside oxide etch or the isotropic release etch process as the F in the plasma might etch the poly, so all poly members are enclosed in oxide. Additionally, the poly is silicided and a method to determine the extent of silicidation after post-CMOS processing has not yet been devised. Because of the relative errors introduced by the silicidation and enclosure of the poly, it is excluded from Young's modulus extraction. However, if a method is found for protecting the poly sidewalls during post-CMOS processing and characterizing the silicidation and its extent, poly can be included in the beams for Young's modulus extraction.

An example of an overdetermined \mathbf{T} for the JAZZ process is shown in Table 6.3. The sensitivity of the inversion of \mathbf{T} and its use in the solution of the problem defined by (6.8) to the measurement errors in \mathbf{k}_z is quantified by its condition number [124]

$$\text{cond}(\mathbf{T}) = \|\mathbf{T}\| \cdot \|\mathbf{T}^{-1}\|, \quad (6.9)$$

where the double vertical bar delimiters represent the norm.

The upper bound on the relative error in the vector of Young's moduli due to numeric calculations is

$$\frac{\|\delta \mathbf{E}\|}{\|\mathbf{E}\|} \leq \frac{\text{cond}(\mathbf{T})}{1 - \|\Delta \mathbf{T}\| \cdot \|\mathbf{T}^{-1}\|} \left(\frac{\|\Delta \mathbf{T}\|}{\|\mathbf{T}\|} + \frac{\|\delta \mathbf{k}_z\|}{\|\mathbf{k}_z\|} \right) \quad (6.10)$$

where, $\|\delta \mathbf{E}\|$ is the norm of the vector of errors of the solution of (6.8), $\|\delta \mathbf{k}_z\|$ is the norm of the vector of errors in the spring constant and $\|\Delta \mathbf{T}\|$ is the norm of the matrix of errors in the geometric coefficients. (6.10) indicates that larger values of $\text{cond}(\mathbf{T})$ lead to larger errors in \mathbf{E} . $\Delta \mathbf{T}$ comprises the error in the layer thicknesses and the member widths and lengths given in Table 6.1. For example, $\text{cond}(\mathbf{T}) = 40$ for \mathbf{T} in Table 6.3 and $\|\delta \mathbf{E}\| = \left\| (\mathbf{T}^T \mathbf{T})^{-1} \mathbf{T}^T \right\| \cdot \|\delta \mathbf{k}_z\| = 2$ GPa, however, if the m321a beam entry is removed from \mathbf{T} , $\text{cond}(\mathbf{T}) = 727$ indicating a significant loss in stability and increase in sensitivity to errors in \mathbf{T} and \mathbf{k}_z . Thus $\text{cond}(\mathbf{T})$ is a tool for identifying the best number and combinations of beams to achieve a compact set of beams while maintaining robustness to error. The smallest set possible is {m1a, m2a, m3a, m321a} with $w_b = 2 \mu\text{m}$ and $l_b = [25, 45, 65, 65] \mu\text{m}$, where the lengths are chosen to produce matrix elements of similar magnitude and minimize $\text{cond}(\mathbf{T})$. With this set $\text{cond}(\mathbf{T}) = 23$. Active area is used under the beams to reduce the radius of curvature and improve target identification on the measurement equipment.

TABLE 6.3 Example of \mathbf{T} for an overdetermined system for the JAZZ process taken from jz60_024 with initial values of 70 GPa for Young's modulus.

Beam Type	w_b (μm)	l_b (μm)	k_z (Nm^{-1})	$T_{\text{ox},j}$ ($\times 10^{11}$ m)	$T_{\text{TiW},j}$ ($\times 10^{11}$ m)	$T_{\text{Al},j}$ ($\times 10^{11}$ m)
m1a	25	2.4	6.4	9.92	0.12	4.35
m2a	75	4.4	3.2	4.34	0.16	1.29
m2a	50	2.4	4.5	7.98	0.30	2.37
m3a	75	4.4	10.4	14.26	0.69	2.38
m3f	50	2.9	19.0	34.28	1.65	5.63
m321a	50	5.4	41.9	46.82	6.71	16.72

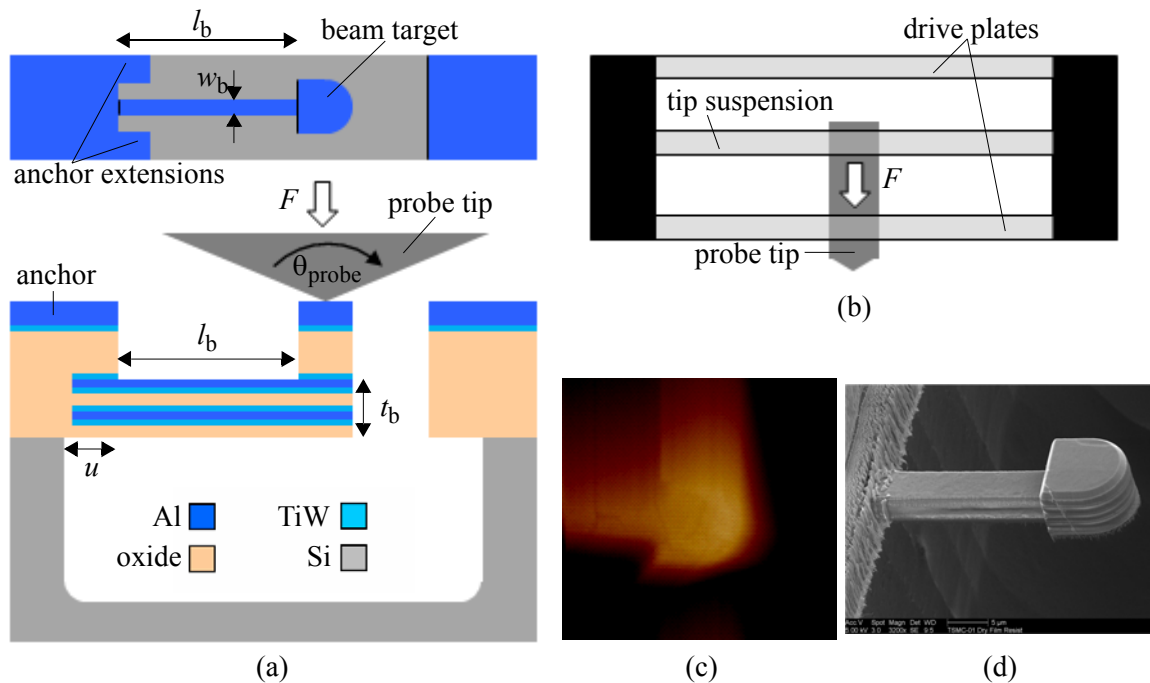
6.4.2 Spring Constant Measurement and Young's Modulus Extraction

A Hysitron TI 900 Triboindenter is used to measure cantilever spring constants $k_{z,j}$ [125]. Sample data from jz60_024 are shown in Table 6.3. The values of Young's modulus extracted using (6.8) for \mathbf{T} and \mathbf{k}_z in Table 6.3 are $E_{\text{ox}} = 38$ GPa, $E_{\text{Al}} = 52$ GPa and $E_{\text{TiW}} = 225$ GPa. The Triboindenter uses a

Berkovich diamond tip mounted on the central plate of a three-plate capacitive transducer. The force is generated electrostatically and applied to the sample after the tip is brought into contact with the beam target using a piezoelectric actuator. A plan view schematic of the cantilever beam, cross-sectional schematics of the beam and the Triboindenter transducer and a scanning image of the beam target are shown in Figure 6.9.

The shallow angle of the probe tip $\theta_{\text{probe}} = 142.35^\circ$ requires that sufficient lateral and vertical clearance be given to the beam target and this is reflected in its design. The top metal of the target is m4 and is designed to be the highest point locally and of higher stiffness than the cantilever. 20 μm of lateral separation is provided between the target and the surrounding features.

FIGURE 6.9 (a) Plan view and cross-sectional schematic of the cantilever test structure. (b) Cross-sectional schematic of the Hysitron capacitive transducer. (c) Raster scan image of the beam target taken by the Triboindenter in a tapping mode similar to an AFM. (d) SEM of a single test structure.



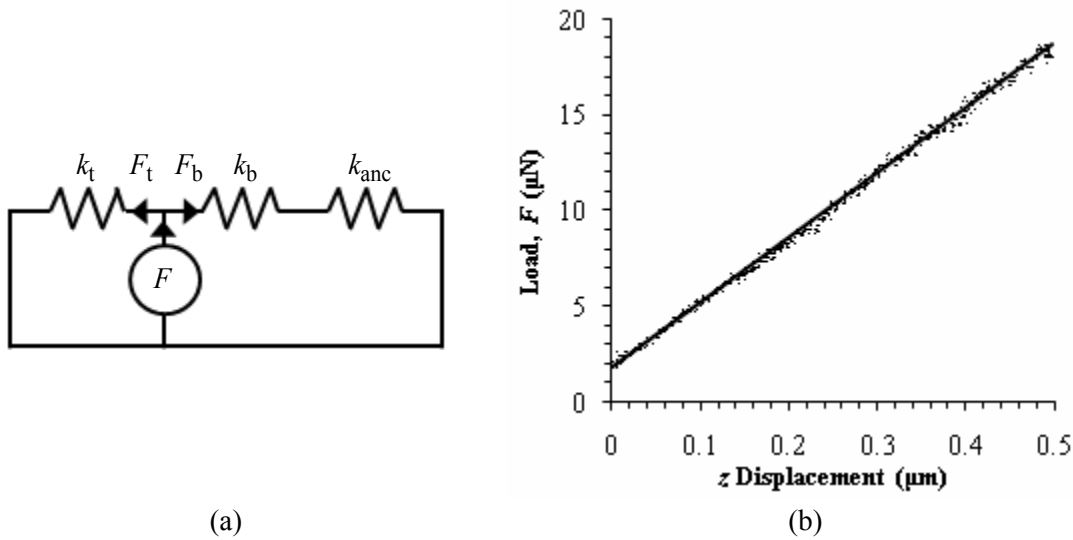
Under test, the force F generated by the transducer is ramped up to 100 μN in 10 s and immediately ramped down to 0 μN in 10 s. The finite stiffness of the tip suspension leads to a force division, such that the load on the cantilever is a fraction of the total load. The stiffness of the anchor also affects the displacement measured by the Triboindenter. In Figure 6.9 (a), the undercut u of the anchor region

reduces the stiffness of the anchor. This is addressed by the anchor extensions shown in the plan view and by using m4 as the top metal layer. Assuming a lumped stiffness model, the impact of the tip suspension and the anchor stiffness can be qualitatively assessed. Given a tip suspension spring constant k_{trans} , a beam spring constant k_b and an anchor spring constant k_{anc} , a simple lumped model is developed and shown in Figure 6.10 (a). The portion of the total load F that appears across the beam and the anchor is F_b , causing a measured displacement z which comprises the beam displacement z_b and any anchor displacement z_{anc} . The extracted spring constant k_z is the gradient of the graph of the applied load F_b versus the measured displacement z shown in Figure 6.10. Given the linearity of the data,

$$k_z = \frac{F_b}{z} = \frac{F_b}{z_b + z_{\text{anc}}} = \frac{k_b}{1 + \frac{k_b}{k_{\text{anc}}}}. \quad (6.11)$$

In the case that $k_{\text{anc}} \gg k_b$, the extracted spring constant $k_z = k_b$.

FIGURE 6.10 (a) Lumped element model of the cantilever beam SUT and the Triboindenter transducer. (b) Load F_b on a m3 cantilever and the measured z -displacement, from which the spring constant k_z is extracted.



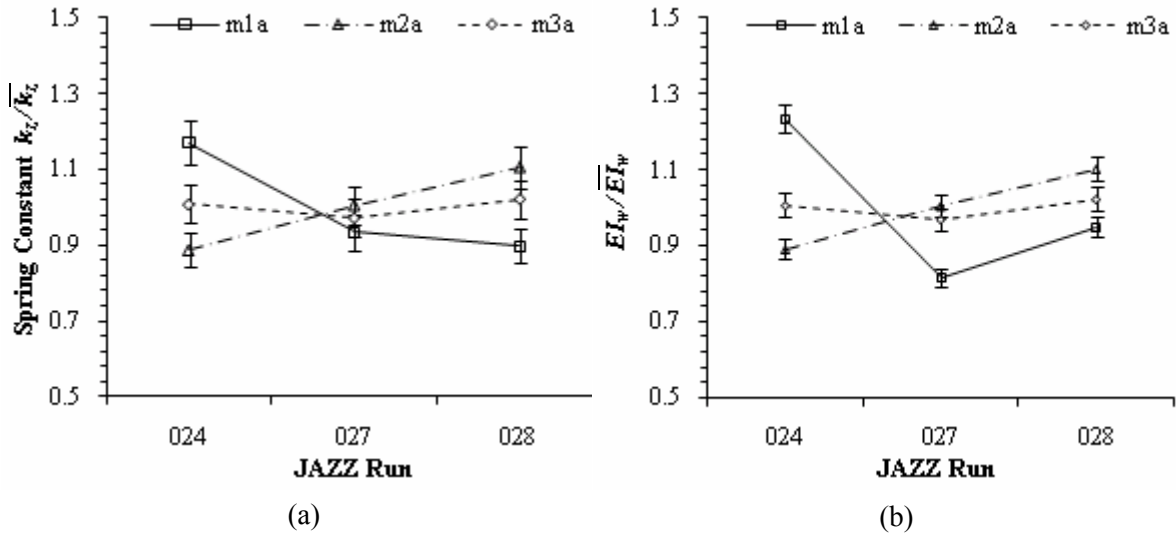
6.4.3 Mechanical Stiffness Process Monitor

For process monitoring, a composite metric, the effective stiffness per unit width EI_w is derived from (6.2):

$$EI_w = \int_0^t E_j z_{b,j}^2 dz_{b,j} = \frac{k_{z,j} l_{b,j}^3}{3w_{b,j}}. \quad (6.12)$$

This parameter combines important information about the material properties and the geometric parameters of the various layers and can be applied directly in the calculation of spring constants.

FIGURE 6.11 Trends of (a) k_z and (b) EI_w for m1a, m2a and m3a beams across several JAZZ runs normalized to the three run mean of each beam type.

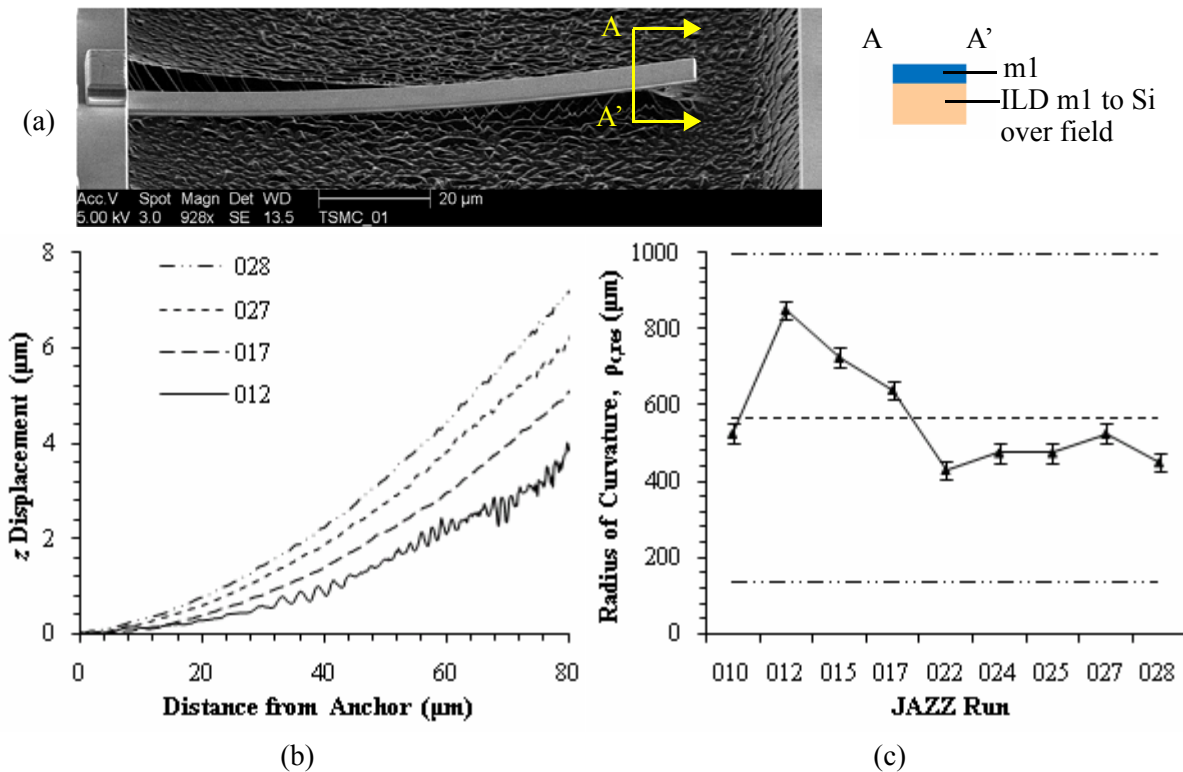


In the interest of reducing the speed of testing and optimization of device area in a chip layout, not all 60 beam combinations are instantiated and measured. Additionally, due to the anchor issue described by (6.11), the spring constant of m4* beams cannot be accurately extracted. For these reasons, the designer is compelled to use the layer thicknesses and Young's modulus for beams outside a basic set. A compromise solution is to provide the trends in k_z and EI_w for m1a, m2a and m3a beams across several JAZZ runs as shown in Figure 6.11 and to extract the Young's modulus for each run from the subset {m1a, m2a, m3a, m321a}. This data is shown in Figure 6.11. It was collected in a single run of the Triboindenter to eliminate error due to machine drift. A Triboindenter repeatability error of 5% was determined by measuring two beam types from separate JAZZ runs several times each.

6.5 Self-Assembly Displacements

Self-assembly in a MEMS device refers to the motion the device displays when it is released due to stresses intrinsic to the materials of which the device is formed. In this sub-section vertical and lateral self-assembly is measured for a CMOS-MEMS process. The radius of curvature ρ_c of a beam is dependent on the stress distribution in the beam and the thickness and biaxial moduli of the materials in the beam, as given by (2.112). An analog of (2.112) is available for lateral, or in-plane, self-assembly. The variation in these displacements run-to-run indicate the composite effect of material property, geometric and stress variations. The residual stresses of the layers of the CMOS stack are not extracted here as the folded actuator structures used in this work negate their impact, however this can be done using ρ_c and a matrix inversion similar to Section 6.4 and [126] provided the condition number is small enough.

FIGURE 6.12 (a) SEM and cross-sectional schematic of a m1f beam used for radius of curvature ρ_c extraction. (b) Vertical displacement along the length of a m1f beam for a representative sample of JAZZ runs. (c) Run-to-run variation in extracted radius of curvature ρ_c .



6.5.1 Vertical Radius of Curvature

The vertical radius of curvature due to residual stress $\rho_{c,res}$ is measured on m1f beams with $w_b = 4 \mu\text{m}$ and $l_b = 80 \mu\text{m}$ (see Figure 6.12 (a)) using a WYKO NT3300 white light interferometer. The vertical displacement along the length of a beam is measured and the arc of a circle is fitted to the data using ρ_c as the fitting parameter. The raw vertical displacement data for a m1f beam over a number of JAZZ runs are shown in Figure 6.12 (b). The processed radius of curvature $\rho_{c,res}$ data are shown in Figure 6.12 (c). The trend suggests a foundry excursion in stress control that was addressed.

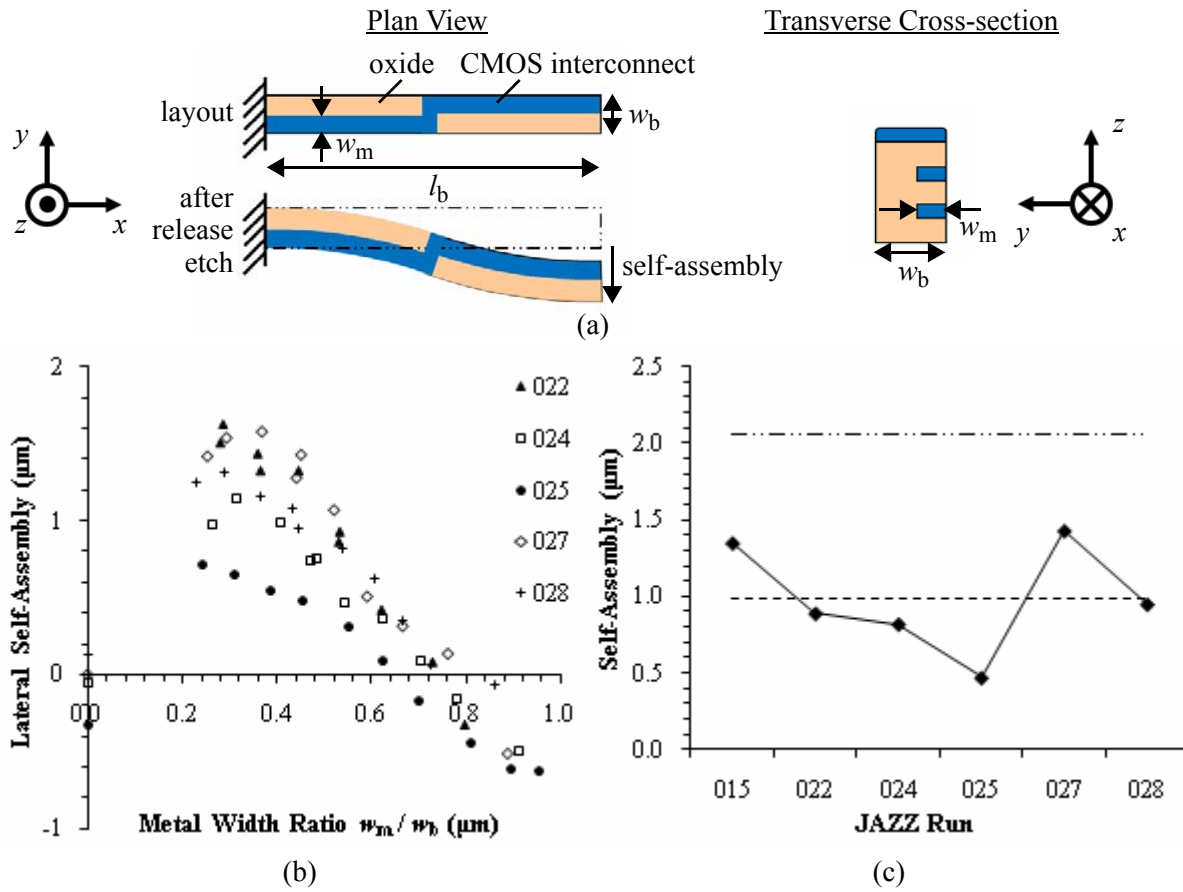
6.5.2 Lateral Self-Assembly

The lateral self-assembly displacement is measured on m321a beams with fixed width w_b but varying internal metal width w_m (see transverse cross-sectional and plan view schematic in Figure 6.13 (a)) using a FEI Sirion SEM. The beams are designed for guided-end motion at their free ends to eliminate measurement error due to tip rotation. For a foundry CMOS process the user cannot control the layer thicknesses to validate the prediction of an optimum metal dimension for maximum stress-induced displacement from (2.15) and illustrated in Figure 2.11 and Figure 2.12; however, varying the width of metal layers in a m321a beam has the same effect as varying the metal thickness in a m1a beam.

Raw lateral displacement data over a range of internal metal widths w_m in a beam with $w_b = 2.2 \mu\text{m}$, $l_b = 100 \mu\text{m}$ and a metal switch point at $l_b/2$ are shown in Figure 6.13 (b). Similar data was presented in [55] but the data shown here explores a wider range of internal metal width ratios w_m/w_b and includes several more JAZZ runs so a picture of the expected variation in residual-stress-induced behavior can be seen. Three of the runs (024, 027, 028) show a maximum in the self-assembly displacement for $w_m/w_b < 0.4$ while the other two have maxima at $w_m/w_b < 0.24$. The variation in the location of the maximum of stress-induced displacement with w_m/w_b is consistent with the relatively compliant oxide and stiffer Al and TiW (see Section 6.4.2) and the variation in the relative thicknesses of these materials from run to run (see Section 6.2.4).

The lack of correlation between the vertical and lateral self-assemblies indicates the post-CMOS process is the dominant source of variation compared to variation in the residual stress of the individual layers. It is noted in Section 6.2.3 that m3 Al is significantly eroded by the frontside oxide etch while no m2 or m1 Al loss is observed. It is likely that the TiW in the m2 and m1 layers acts as a buffer preventing the Al from being eroded. The variation in TiW erosion is eliminated by the chemical etching of TiW by the F of the DRIE process leaving only the variation in the thickness and residual stress of Al and bottom TiW layer thickness to impact vertical self-assembly. On the other hand, lateral self-assembly structures with m3 as the top layer are subject to the variation in thickness and residual stress of all the layers and the variation in m3 Al erosion caused by the frontside oxide etch.

FIGURE 6.13 (a) Transverse and plan view schematics of a m321a beam for lateral self-assembly displacement measurement. (b) Variation in lateral self-assembly displacement of the free end of m321a beams with nominal $w_b = 2.2 \mu\text{m}$ over a range of internal metal width ratios w_m/w_b . (c) Trend of the lateral self-assembly displacement of a beam with nominal $w_b = 2.2 \mu\text{m}$ and nominal $w_m/w_b = 0.5$ over a number a JAZZ runs.



6.6 Vertical Actuator Response Dependencies

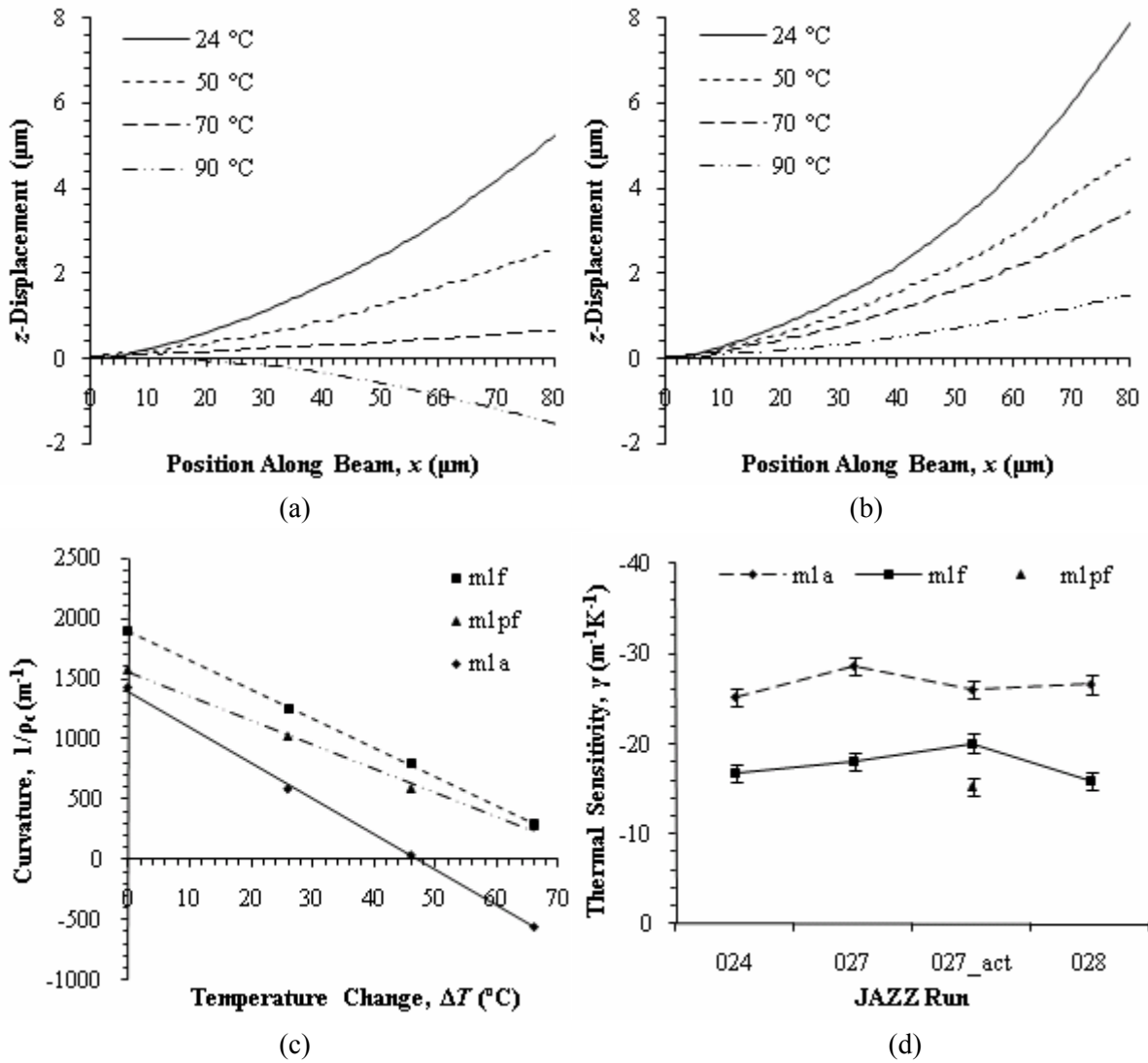
The determination of thermal sensitivity γ for a given beam type is described in this sub-section. The effects on beam shape of a temperature gradient generated in a beam and of a plate of varying dimensions at the end of a beam are used to validate predictions made by the analytic theory in Chapter 2. For example, for a given Joule-heating-induced thermal input power P_h , a larger plate at the end of the beam, representing a mirror pedestal, should result in a smaller deflection angle θ_m because the heat loss P_m would be larger and the temperature rise ΔT_h in the heater would be smaller. Through the use of test structures that isolate the impact of particular characteristics of the system, the contribution to overall device performance is assessed.

6.6.1 Thermal Sensitivity

The thermal sensitivity γ of a beam, defined by (2.17), depends on the dimensions of the members of the beam and the CTE and elastic moduli of the materials in it. The value of γ can be used to approximate the CTE of the layers in the beam under some simplifying assumptions [126]. However, because of the way the analytic expressions are developed in Chapter 2, the values of CTE for m1* actuators would not provide additional insight about device response and are not extracted here.

Thermal sensitivity is measured using a WYKO NT3300 white light interferometer. The radii of curvature ρ_c of m1* beams of equivalent dimension as that in Figure 6.12 are measured over a range of temperature changes ΔT using the technique described in Section 6.5.1 (see Figure 6.14 (a) and (b) for examples of the z -displacement variation). Temperature is varied using a thin film heater mounted on the back of the chip package using thermal grease. The temperature is measured on the top of the package using a Pt resistance temperature detector (RTD) mounted using thermal grease. The temperature difference between the chip surface and the RTD has been measured at < 1 °C.

FIGURE 6.14 Variation in (a) m1a and (b) m1f beam shape over a range of temperatures. (c) Graph of the radius of curvature ρ_c of m1* beams over a range of temperature changes ΔT . (d) Trend of the radius of curvature ρ_c of m1* beams over a number a JAZZ runs.



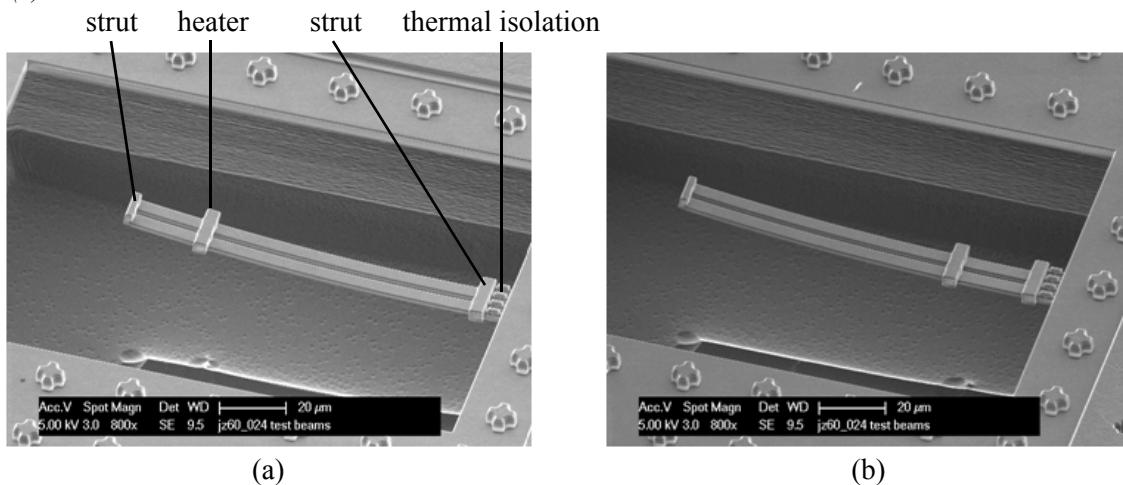
A graph of ρ_c versus ΔT is formed (Figure 6.14 (c)) and the gradient of the graph, γ , is extracted and plotted for m1a and m1f beams over a number of JAZZ runs (Figure 6.14 (d)). Actuator test structures (m1a, m1f and m1pf) of equivalent dimensions are measured similarly and included in Figure 6.14 (d) under the category “027_act”. The relative values of γ for the three beam types are consistent with the predictions of the analytic theory in Section 2.2.2 given the compositional differences of the beams. The measured m1f γ ($20.1 \text{ m}^{-1}\text{K}^{-1}$) matches well with theory ($18.9 \text{ m}^{-1}\text{K}^{-1}$), but the measured m1pf γ ($15.2 \text{ m}^{-1}\text{K}^{-1}$) is lower than predicted ($17.4 \text{ m}^{-1}\text{K}^{-1}$) and the measured m1a γ ($26 \text{ m}^{-1}\text{K}^{-1}$) is higher than

predicted ($20.4 \text{ m}^{-1}\text{K}^{-1}$) based on the Young's modulus values extracted in Section 6.4.2 and CTE and Poisson's ratio values from the literature. For the m1pf beam an explanation may lie in the form of the poly. In Figure 6.5 the poly layer appears to consist of two layers. The upper part is a silicide which could have a higher CTE than pure poly and this would contribute a higher opposing moment below the neutral bending axis. For the m1a beam, it is possible that the extracted value of Young's modulus for the oxide represents a convolution of thermal and LPCVD oxide that may have a large difference in modulus in reality. Thus, the m1a beam which contains no thermal oxide may be much less stiff than the m1f beam.

6.6.2 Heater Placement Impact on Actuator Response

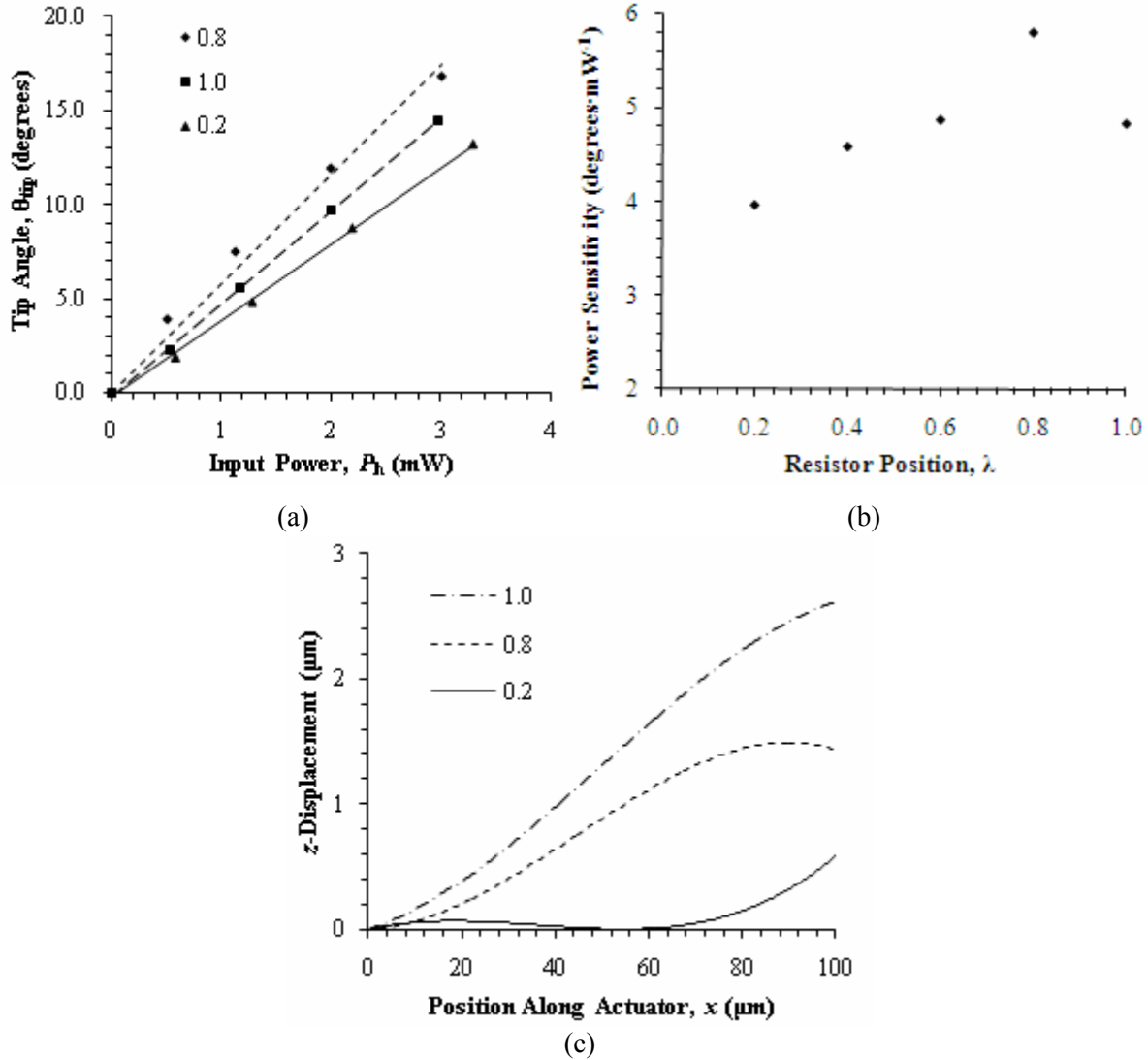
The impact of the placement of the poly heater on the beam shape under thermal stimulation is presented in this section. As predicted in Chapter 2, the heater placement has a significant effect on the performance of the actuator. This is because the thermal resistance of the actuator $R_{\text{th,a}}$ provides a significant proportion of the thermal resistance between the actuator and ground $R_{\text{th,anc}}$ and between the actuators. $R_{\text{th,a}}$ affects the temperature change ΔT for a given power input P_h and also the temperature distribution $T(x)$ in the beam.

FIGURE 6.15 Actuator test structures with $w_b = 4 \mu\text{m}$, $l_b = 100 \mu\text{m}$ and varying heater placement: (a) $\lambda = 0.8$ and (b) $\lambda = 0.2$.



The actuator structures shown in Figure 6.15 (a) and (b) illustrate different heater placements $0.2 < \lambda < 1.0$. The actuator test structures are similar to the micromirror actuators in that they comprise thermal isolation, anchor and end struts and a heater resistor. Two $m1^*$ beams ($w_b = 4 \mu\text{m}$, $l_b = 100 \mu\text{m}$) are used in the actuator test structure to carry current into and out of the heater.

FIGURE 6.16 (a) Actuator tip angle θ_{tip} vs. input power P_h for actuators with $\lambda = 0.2, 0.6$ and 0.8 . (b) Power sensitivity θ_{tip}/P_h over a range of λ . (c) Beam shape $z(x)$ at $P_h = 2 \text{ mW}$ for $\lambda = 0.2, 0.6$ and 0.8 .



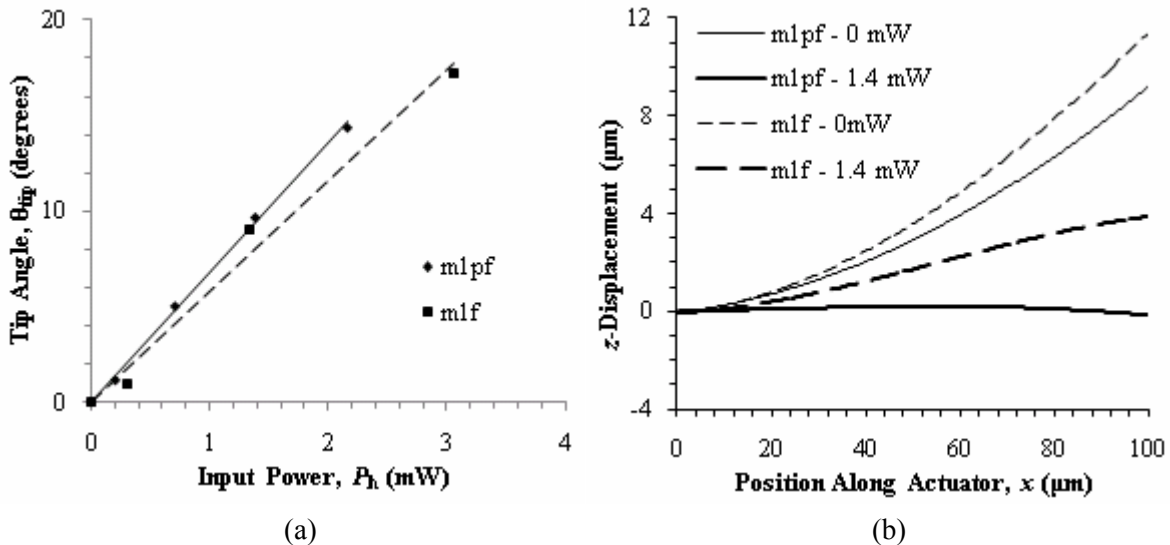
The beam shape $z(x)$ of each actuator is measured over a range of P_h using a WYKO NT3300 white light interferometer. The tip angle θ_{tip} at each P_h is extracted from $z(x)$ using the relation

$$\theta_{\text{tip}} = \left. \frac{dz}{dx} \right|_{x=l_a} \quad (6.13)$$

and plotted in Figure 6.16 (a). The gradient of the LSR linear fit of Figure 6.16 (a) is the power sensitivity θ_{tip}/P_h of the actuator and is extracted and plotted against λ in Figure 6.16 (b). The roughly parabolic dependence of power sensitivity on λ is consistent with the predicted behavior of discrete heater actuators illustrated in Figure 2.23. The beam shape dependence on λ , as predicted by (2.54) to (2.56), is shown in Figure 6.16 (c) for a constant $P_h = 2$ mW and heater placements of $\lambda = 0.2$ and 0.8 .

The loss of power sensitivity due to non-optimal heater placement can negate the inherent electro-thermomechanical gain advantage that the m1f discrete heater actuator has over a m1pf distributed heater actuator. The m1f and m1pf actuators whose thermal sensitivity γ is presented in Section 6.6.1 are compared head-to-head in Figure 6.17. The heater is placed at the end of the m1f actuator (i.e. $\lambda = 1.0$), shown in Figure 6.16 (b) to be non-optimal. The z -displacement is measured as described above and θ_{tip} is extracted and plotted against P_h in Figure 6.17 (a). The beam shape of each actuator is compared at $P_h \approx 1.4$ mW in Figure 6.17 (a). The m1pf distributed heater actuator has a power sensitivity of $6.8 \text{ deg}\cdot\text{mW}^{-1}$ compared to $5.8 \text{ deg}\cdot\text{mW}^{-1}$ for the m1f discrete heater actuator.

FIGURE 6.17 (a) Actuator tip angle θ_{tip} vs. input power P_h for a m1pf distributed heater actuator and a m1f discrete heater actuator with $\lambda = 1.0$. (b) Comparison of m1pf and m1f actuator beam shape at $P_h \approx 1.4$ mW.

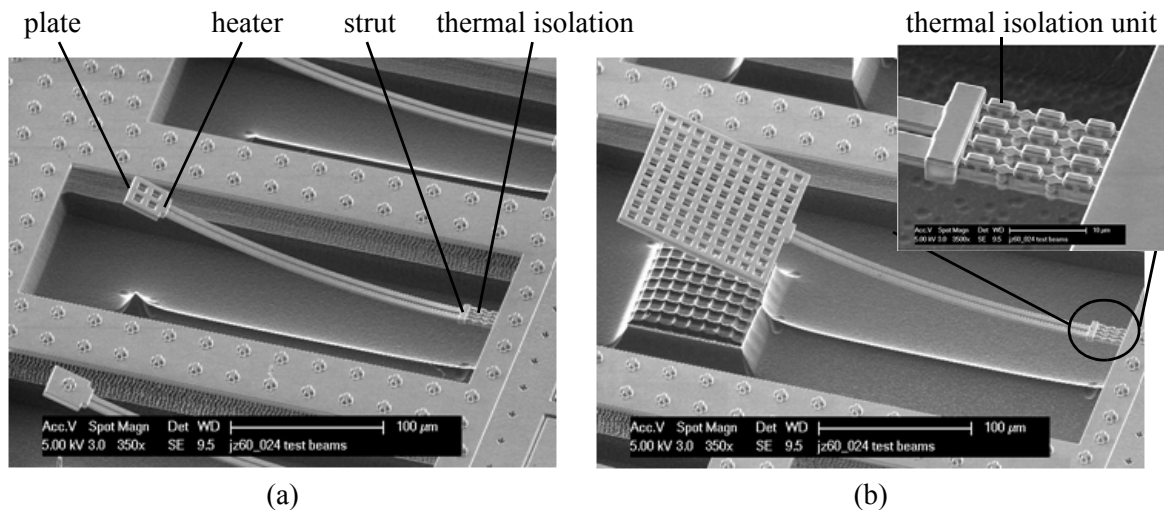


6.6.3 End Plate Impact on Actuator Response

The impact of plates attached to the free end of the actuator is presented in this sub-section. As predicted in Chapter 2, a plate attached to the free end of an electrothermal actuator plays a significant role in cooling the actuator through convection and air conduction. The thermal resistance to ground through the actuator and plate $R_{th,m}$ affects the temperature change ΔT for a given power input P_h and also the temperature distribution $T(x)$ in the beam.

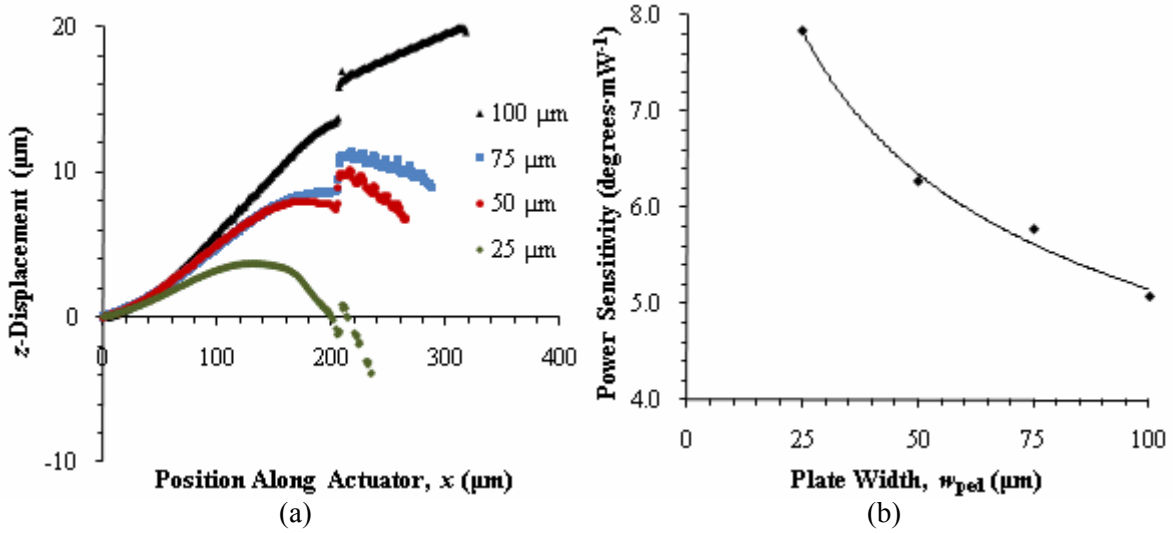
The actuator test structure used to explore the impact of plate dimension w_{ped} is shown in Figure 6.18. The actuator structure is similar to that shown in Figure 6.15 with the exception of a perforated plate at the free end and three thermal isolation units at the anchor to balance solid thermal conduction through the anchor and air conduction and convection through the plate.

FIGURE 6.18 Actuator test structures with $w_b = 4 \mu\text{m}$, $l_b = 200 \mu\text{m}$, $\lambda = 1.0$ and varying plate dimension: (a) $w_{ped} = 25 \mu\text{m}$ and (b) $w_{ped} = 100 \mu\text{m}$.



The beam shape is measured and the tip angle and power sensitivity are extracted as described in Section 6.6.2. Graphs of the deformed beam shape for each plate dimension at a constant input power $P_h = 4.6 \text{ mW}$ is shown in Figure 6.19 (a) and the power sensitivity variation with w_{ped} is shown in Figure 6.19 (b). As expected based on theory, as w_{ped} increases the power sensitivity decreases.

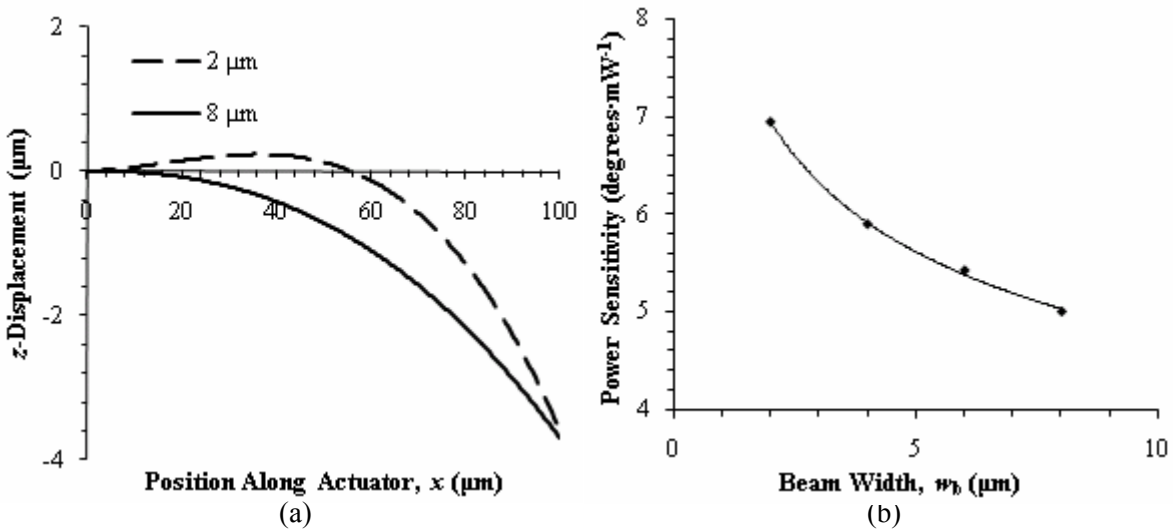
FIGURE 6.19 (a) Comparison of actuator beam shapes at $P_h \approx 4.6 \text{ mW}$ for a range of w_{ped} . (b) Power sensitivity θ_{tip}/P_h over a range of w_{ped} .



6.6.4 Beam Width Impact on Actuator Response

The variation in power sensitivity with beam width w_b is explored using actuators like those described in Section 6.6.2 with a constant $\lambda = 1.0$ to make $R_{th,a}$ the dominant thermal resistance in determining ΔT_h . The method for determining the power sensitivity is the same as described in Section 6.6.2. The beam shape for $w_b = 2 \mu\text{m}$ and $8 \mu\text{m}$ and $P_h = 2 \text{ mW}$ is shown in Figure 6.20 (a). The power sensitivity variation with w_b is shown in Figure 6.20 (b) and decreases with w_b as predicted.

FIGURE 6.20 (a) Comparison of actuator beam shapes at $P_h = 2 \text{ mW}$ for $w_b = 2 \mu\text{m}$ and $8 \mu\text{m}$. (b) Power sensitivity θ_{tip}/P_h variation with w_b .



6.7 Mirror and Actuator Performance

This section covers the performance of SOI-CMOS-MEMS folded electrothermal actuators and micromirror arrays. Actuators are demonstrated with 1-D motion at $\Omega = 1$ mm, 100 μm and 50 μm and with 3-D motion at $\Omega = 500$ μm and 100 μm and their power response, cross-talk, scan range and speed are characterized. A 3 x 3 array of 1 mm pitch micromirrors is characterized also, but additionally the coplanarity of array elements is examined.

6.7.1 Electrothermal Actuator Design Space

The design parameters of the mirror actuators are shown in Table 6.4. Only actuator 1A1K, a 1-D form A actuator with a 1 mm pitch is successfully integrated with an SOI mirror using the SOI-CMOS-MEMS described in Chapter 3. The other forms are either instantiated only as actuators or fabrication issues prevented mirror-actuator integration. SEM images of the electrothermal actuators characterized in this chapter are shown in Figure 6.21 (1-D) and Figure 6.22 (3-D). Figure 6.23 shows the arrays of the actuators in Figure 6.21 and Figure 6.22. Array elements are identified by their row and column, ex. r1c3 = row 1, column 3, the bottom left element in each array being r1c1.

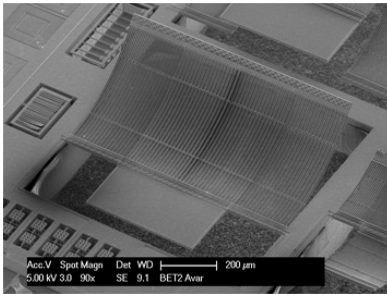
TABLE 6.4 Design parameters of the electrothermal mirror actuators characterized in this section.

Design Parameters (μm)	1A1K	1D1K	1E1K	1E100	1D50	1E50	3C500	3C100
motion type	rot.	rot.	rot.	rot.	rot.	rot.	2 rot. piston	2 rot. piston
actuator beam type	m1a	m1f	m1f	m1a	m1pf	m1pf	m1a	m1a
mirror pitch, Ω_m	1000	1000	1000	100	50	50	500	100
mirror length, l_m	980	980	980	95	46	46	490	95
mirror Si thickness, $t_{m,\text{Si}}$	25	25	25	5	5	5	5	5
mirror Al thickness, $t_{m,\text{Al}}$	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
BOX thickness, t_{BOX}	1	1	1	0.5	0.5	0.5	0.5	0.5
post width, w_p	120	120	120	20	15	15	45	20
post thickness, t_p	500	500	500	150	150	150	150	150
pedestal width, w_{ped}	220	220	220	25	24	24	175	24
pedestal length, l_{ped}	444	220	220	25	24	24	175	24

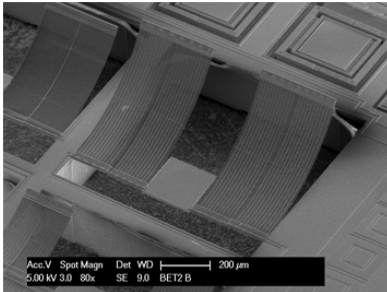
Design Parameters (μm)	1A1K	1D1K	1E1K	1E100	1D50	1E50	3C500	3C100
pedestal-anchor gap, g_{ped}	53	160	340	25	1.7	1.7	n/a	n/a
pedestal Si thickness, $t_{\text{ped,Si}}$	35	35	35	0	0	0	35	0
anchor width, w_{anc}	100	100	100	25	5	5	100	10
isolation width, w_{iso}	1.2	1.2	1.2	n/a	1.2	n/a	n/a	1.2
via enclosure, e_{v}	1.3	0.4	0.4	0.4	0.28	0.3	0.15	0.35
isolation length, l_{iso}	6.6	6.6	6.6	n/a	3.5	n/a	n/a	3.5
isolation in parallel, $N_{\text{p,v}}$	48	40	28	n/a	2	n/a	n/a	10
isolation in series, $N_{\text{s,v}}$	2	2	2	n/a	1	n/a	n/a	1
strut width, w_{s}	20	20	20	3.6	3	2.8	12	3.5
strut length, $l_{\text{s,anc}}$	225	169	113	8	n/a	n/a	n/a	n/a
strut length, $l_{\text{s,a}}$	447	334	222	15	7	4.4	n/a	n/a
strut length, $l_{\text{s,21}}$	n/a	n/a	n/a	n/a	n/a	n/a	746	148
strut length, $l_{\text{s,32}}$	n/a	n/a	n/a	n/a	n/a	n/a	612	115
strut length, $l_{\text{s,43}}$	n/a	n/a	n/a	n/a	n/a	n/a	478	79.4
strut- anchor gap, g_{s}	48	170	141	1.6	1.8	1.9	9	2
beam width, w_{b}	5	5	5	1	3	1.7	1	4
beam length, l_{b}	466	466	452	52	34.7	34.4	66	12.1
beams in parallel, $N_{\text{p,b}}$	32	24	16	4	1	1	96	5
beam-beam gap, g_{b}	2	2	2	1	1	1	1	1
heater width, w_{h}	7	7	7	4.5	n/a	n/a	4.5	2.4
heater length, l_{h}	12	12	12	7	n/a	n/a	7	24
heater poly width, w_{p}	4.8	4.8	4.8	2	2	0.7	2	1
heater poly enclosure, e_{p}	1.1	1.1	1.1	1.25	0.5	0.5	1.2	0.7
heater position, λ	0.25, 0.75	0.25, 0.75	0.125 0.375 0.625 0.875	0.5	n/a	n/a	0.5	0.5
actuator length, l_{a}	480	480	480	61	36.7	35.6	70.5	13.5
Si undercut, u	14	14	14	7	7	7	7	7

FIGURE 6.21 SEM images of 1-D folded electrothermal actuators characterized in this chapter.

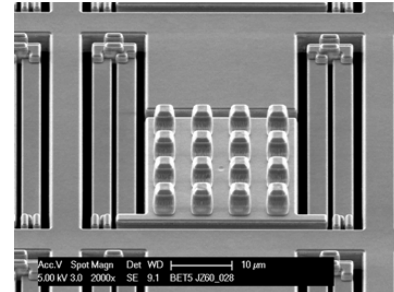
1-D, Form A, $\Omega = 1 \text{ mm}$



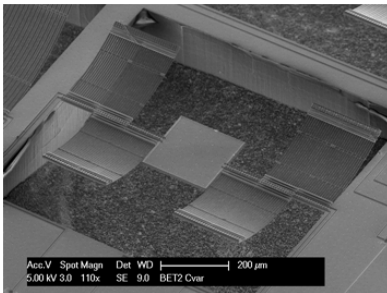
1-D, Form D, $\Omega = 1 \text{ mm}$



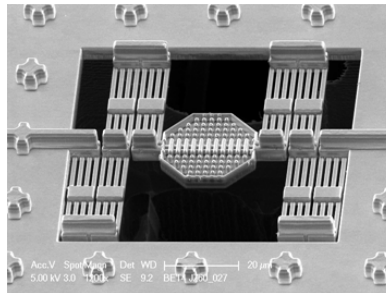
1-D, Form D, $\Omega = 50 \mu\text{m}$



1-D, Form E, $\Omega = 1 \text{ mm}$



1-D, Form E, $\Omega = 100 \mu\text{m}$



1-D, Form E, $\Omega = 50 \mu\text{m}$

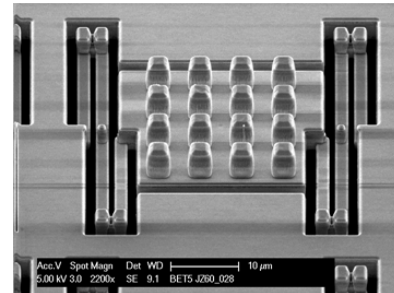


FIGURE 6.22 SEM images of 3-D electrothermal actuators characterized in this chapter.

3-D, Form C nested, $\Omega = 500 \mu\text{m}$ 3-D, Form C nested, $\Omega = 100 \mu\text{m}$

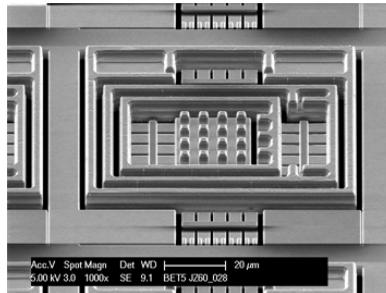
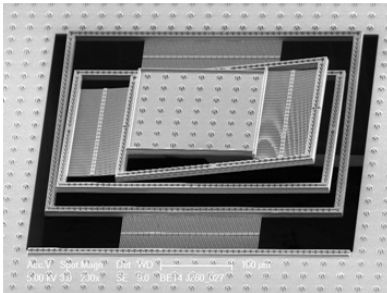
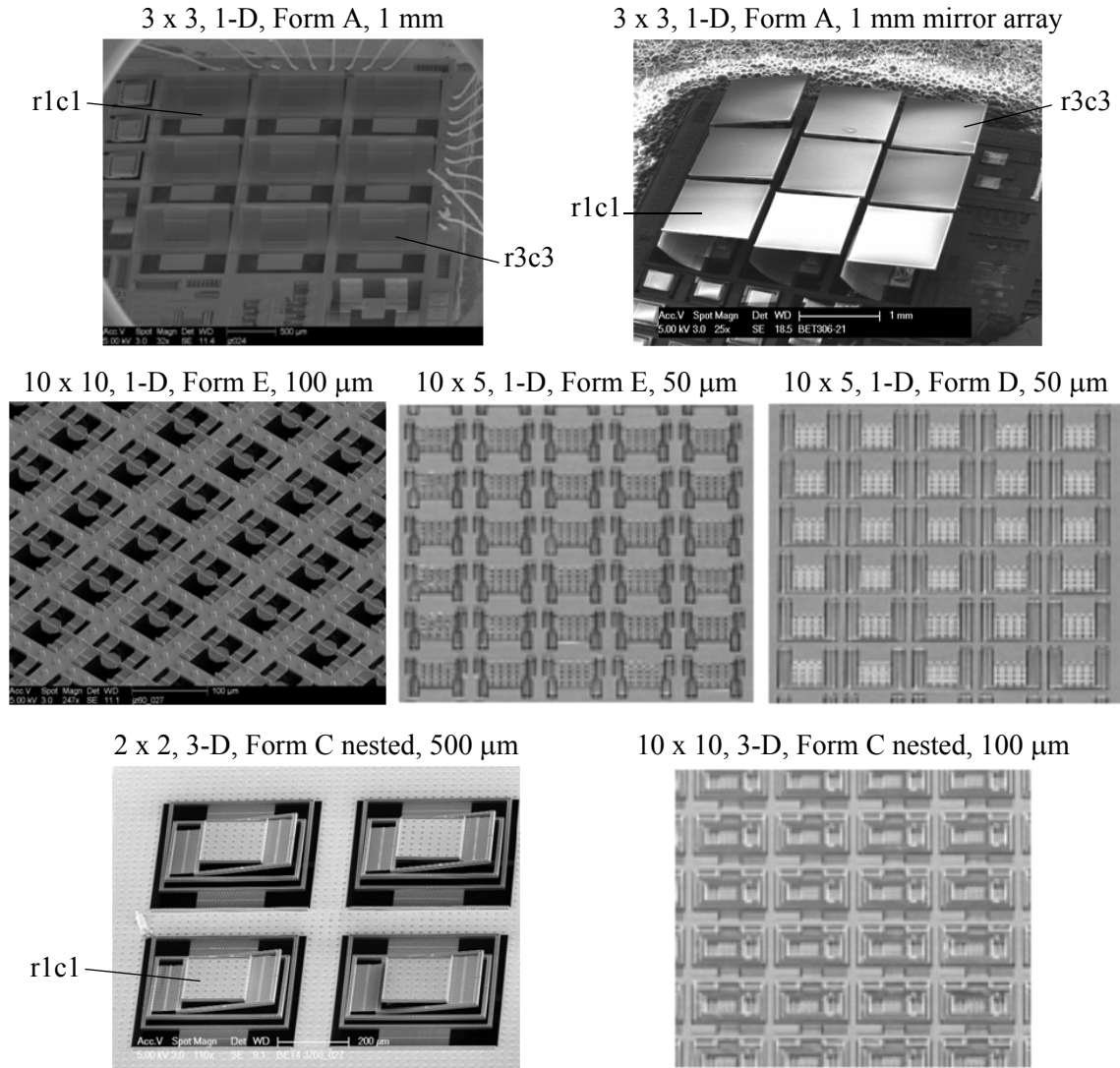


FIGURE 6.23 SEM images of arrays of CMOS-MEMS actuators of the designs shown in Figure 6.21 and Figure 6.22. A SEM image of an SOI-CMOS-MEMS mirror array utilizing 1A1K type actuators is also shown.

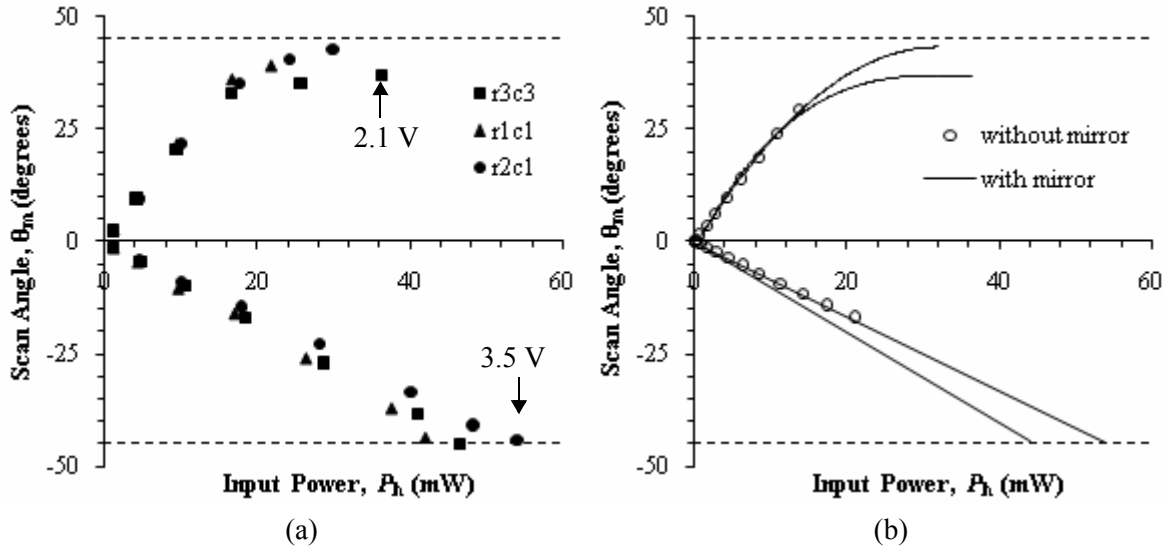


6.7.2 SOI-CMOS-MEMS Mirror Angular Displacement

The scan range is measured in two ways, the choice of which depends on the size of the reflective element. For 1 mm pitch, 1-D devices and the 500 μm 3-D device, a laser is focussed on the mirror, or pedestal and the beam is reflected onto a semi-circular, translucent screen with a radius of 560 mm. The arc length to the reflected beam position is measured with respect to the rest position of the reflected spot. The distance between the device and the screen determines the error in the measurement, with a larger distance giving a smaller error; however if beam divergence is large the spot reso-

lution decreases with distance to the screen. The WYKO NT3300 is used to measure the angular displacement of designs with pedestal dimensions $< 200 \mu\text{m}$. At each value of input voltage, the height variation of the pedestal is measured and its angle with respect to the anchor region is extracted.

FIGURE 6.24 (a) Variation in mirror angular displacement θ_m with input power P_h for SOI-CMOS-MEMS mirrors bonded to a 1A1K design actuator. (b) Comparison of angular displacement response of a 1A1K design actuator with the bounds of the response for the mirrors in Figure 6.24 (a).



Mirror scan angle data for the 1A1K actuator design are shown in Figure 6.24 (a). The condition for chip thickness t_w to enable the designed mirror angular displacement of 45° , given by (2.123), is not met for the JAZZ foundry process, so the chip characterized for θ_m uses a chip carrier, shown in Figure 3.22. On this chip, the additional handling necessary to mount the chip in the carrier resulted in a low array yield and only 3 elements remain for characterization. As predicted by the power scaling argument in Section 2.4.5, the outer actuator of all three mirrors requires a greater power input to achieve the same temperature, and hence scan angle θ_m as the inner actuator. As predicted by (2.57) when applied in (2.98) and (2.99), θ_m is linear in P_h ; however as the actuator approaches the positive sense rotation limit of $\theta_{m+} = 45^\circ$ the relationship becomes non-linear. It is thought that this behavior occurs because the thermal resistance to ground R_{th} decreases significantly as the hot pedestal approaches the substrate and heat loss to the substrate increases. This effect is not accounted for in the device design and the observation needs to be fed back into a subsequent design round.

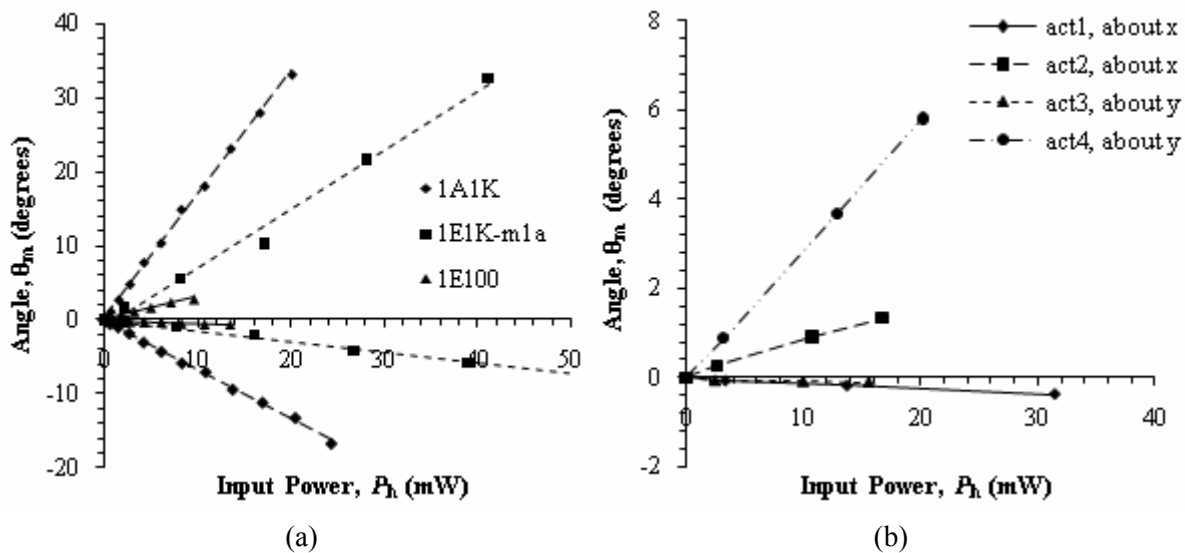
In Figure 6.24 (b) the bounds of the angular displacement response of the elements of the mirror array in Figure 6.24 (a) are compared to the angular displacement response of an actuator with no mirror bonded to it. The response of the actuator without a mirror is not significantly different from the response of the actuators with a mirror which indicates the mirror and the post do not provide a significant heat conduction path to ground for the actuator. It is likely the epoxy used to bond the mirror and the post to the actuator has a low thermal conductivity and the use of m4 standoffs on the pedestal reduces the metal to Si contact at the interface between the post and the pedestal further reducing thermal conduction into the post. The smaller range of θ_m for the actuator without a mirror is an issue of the measurement method; the pedestal moves out of the path of the laser beam as θ_m increases in the negative sense and the laser beam is reflected into the sidewall of the etch pit as θ_m increases in the positive sense.

The power sensitivity for the SOI-CMOS-MEMS mirror array elements in the positive rotation sense is $1.9 \pm 0.1 \text{ deg}\cdot\text{mW}^{-1}$ in its linear range, while in the negative rotation sense it is $0.9 \pm 0.1 \text{ deg}\cdot\text{mW}^{-1}$. The reason for the difference is the different thermal resistances to ground seen by the inner and outer actuator. The inner actuator measures about 2 times more sensitive than the outer actuator. The analysis of the generic system that led to the variation in $\theta_{m,\text{max}}/P_{\text{max}}$, illustrated in Figure 2.29 (a), predicts the inner actuator is approximately 5 times more sensitive than the outer. The main cause of the disparity between the measured ratio of power sensitivities and the system analyzed in Section 2.4.5 is the non-optimal heater positions in the fabricated device. Secondary effects, such as heat conduction through air from the outer actuator to the anchor and from the inner actuator to the outer actuator also reduce this ratio. Another factor whose significance was not considered in the analysis is the constant reduction in the heat loss through air from the pedestal to the substrate as it rotates in the positive sense, i.e. when the inner actuator is powered $R_{\text{th},m}$ decreases monotonically. Conversely, when the outer actuator is powered, the pedestal moves away from the substrate further increasing $R_{\text{th},m}$.

6.7.3 Comparison of Response for Actuators of Various Scales

The pedestals attached to 1-D actuators at 50 μm pitch do not display any motion, although the struts joining the actuators are observed to move. This indicates that at that scale the thermal isolation separating the two legs of the actuators is insufficient to achieve the temperature difference between the legs necessary to achieve differential bending. The pedestals of the 1-D 100 μm pitch devices are observed to move even though the thermal isolation is similar in form and dimension. This points to the significance of the actuator length l_a which both amplifies the intrinsic electrothermomechanical gain and thermally isolates the heaters. Figure 6.25 (a) shows a comparison of the actuator responses for 1-D devices at each scale at which motion is observed. The observed variation in the power sensitivity from 1E1K to 1E100 is $0.80 \text{ deg}\cdot\text{mW}^{-1}$ to $0.31 \text{ deg}\cdot\text{mW}^{-1}$ respectively, for the inner actuator and $0.14 \text{ deg}\cdot\text{mW}^{-1}$ to $0.05 \text{ deg}\cdot\text{mW}^{-1}$ respectively, for the outer actuator which is consistent with the models developed in Chapter 2.

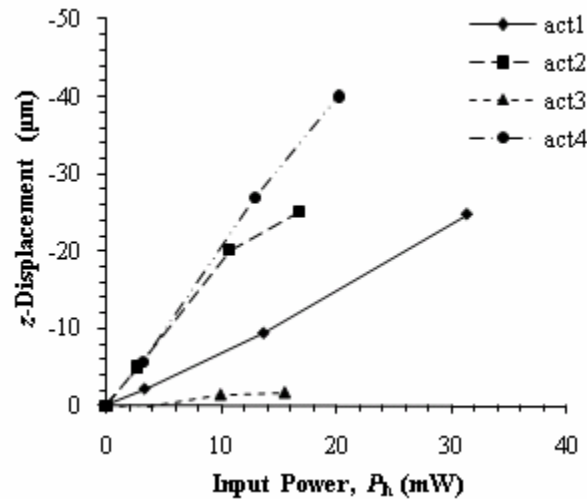
FIGURE 6.25 Comparison of actuator angular power response for (a) 1-D and (b) 3-D actuators.



The 3-D actuators are designed to rotate about the x - and y -axes and translate in the z -direction. These motions are coupled so it is necessary to use the WYKO NT3300 to characterize the power response. The angular displacement response is shown in Figure 6.25 (b) and the piston displacement response is shown in Figure 6.26. The power sensitivity of the actuators is 0.29 and $0.08 \text{ deg}\cdot\text{mW}^{-1}$ for

act2 and act4, respectively, and -0.01 and $-0.006 \text{ deg}\cdot\text{mW}^{-1}$ for act1 and act3, respectively. The power sensitivity of act2 and act4 are comparable to the power sensitivity of the 3E100 actuator, which has a similar l_b , but are lower because thermal isolation units are not used for the 3E100 design to maximize l_b for the design. The act1 actuator is connected directly to the anchor and the lower power sensitivity is due to the lack of thermal isolation from the anchor. The act3 actuator is likely poorly thermally insulated from the act4 actuator and may couple in to act4 through air conduction to the pedestal and through it. The z -displacement power sensitivity ranges from $-2 \text{ }\mu\text{m}\cdot\text{mW}^{-1}$ to $0.1 \text{ }\mu\text{m}\cdot\text{mW}^{-1}$. This actuator is poorly designed for angular displacement and as a result has a very large piston response. Redesign of the thermal isolation of the various legs of the actuator is necessary to better balance these responses.

FIGURE 6.26 *Piston displacement response of the 3C500 actuators.*

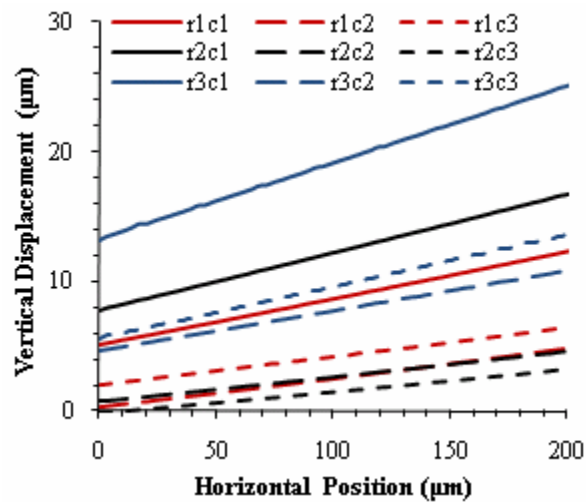


6.7.4 Mirror Array Element Coplanarity

The similarity in the characteristics of the elements of an array of device is important as any difference must be compensated for either through the input or at the output. In an array of mirror devices, the mirror surfaces must all lie in the same plane when the mirrors are at rest i.e. all the mirrors must be coplanar after release etch and packaging. Any deviations in coplanar rest angle, like those visible in Figure 6.23, must be compensated for by a bias voltage, which for electrothermal actuators results in

added power consumption and requires that the planarity deviations be measured to determine a bias correction. An alternative method of correcting for released microstructure variation was demonstrated by Comtois et al. [127] who thermally overstressed their actuators to permanently deform them in a controllable way. Comtois et al. demonstrated this technique in a poly-based process where the microstructure was homogeneous. In CMOS-MEMS, the metal layers of the actuators delaminate when they are thermally overstressed, so the feasibility of the technique for addressing coplanarity deviations is questionable, however a more thorough investigation of this possibility is warranted given the characterization load and increased power consumption imposed by the obvious compensation method described above. Alternatively, the fabrication technology could be modified to make this a non-issue, but this topic is avoided until the final chapter.

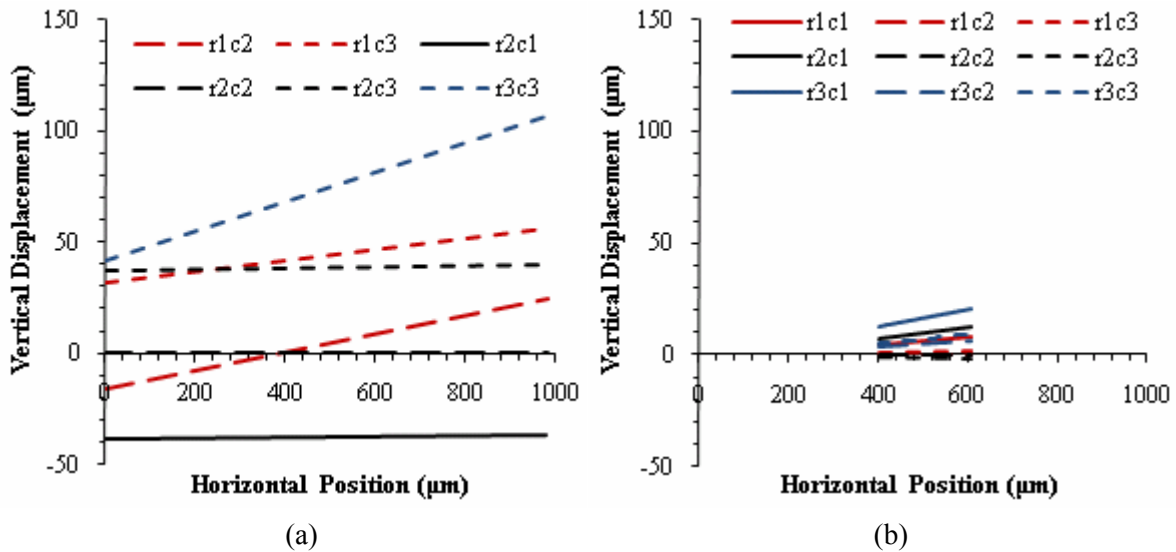
FIGURE 6.27 Coplanarity of the 3×3 1A1K actuator array shown in Figure 6.23.



The WYKO NT3300 is used to characterize the coplanarity of the array elements. The raw height data of the pedestals in the 1A1K actuator array are shown in Figure 6.27. The rest angles of the mirror array and actuator array referenced to the center element are shown in Figure 6.28 (a) and (b), respectively. The center elements (i.e. row 2, column 2) of the 3×3 SOI-CMOS-MEMS mirror array and 1A1K actuator array shown in Figure 6.23 are used to define reference planes and the rest angles of the other elements in the array are measured with respect to them. The two datasets are plotted in Figure 6.28 with the same horizontal and vertical scales to facilitate direct comparison. Not all mirror

elements are plotted in the graph to maintain clarity of message. The range of rest angles in the actuator array is 2.4° and in the mirror array it is 3.8° , however the range of vertical displacements in the mirror array is approximately $100\ \mu\text{m}$ compared to less than $30\ \mu\text{m}$ in the actuator array.

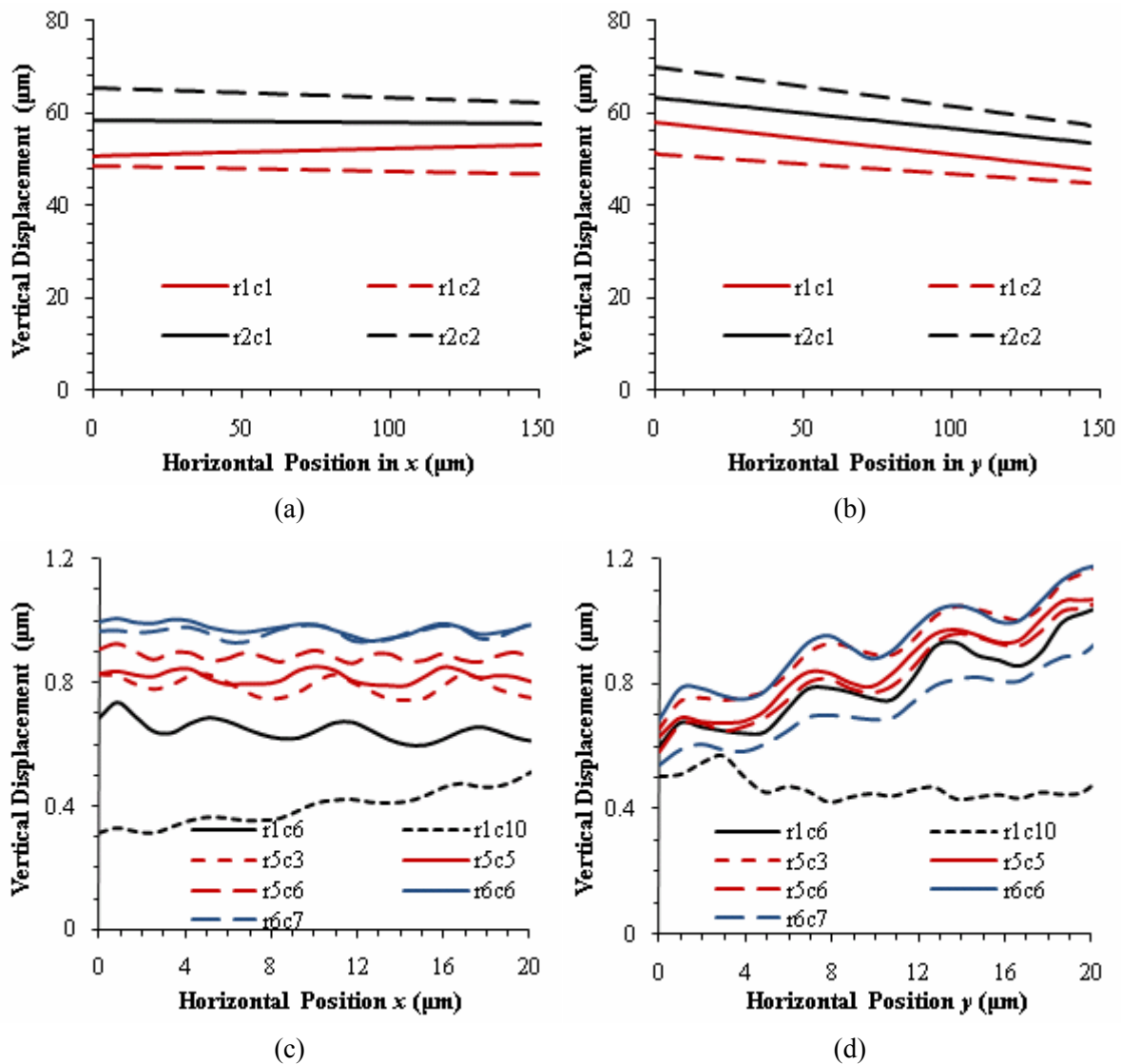
FIGURE 6.28 Coplanarity of (a) the 3×3 SOI-CMOS-MEMS mirror array and (b) the 3×3 LAIK actuator array shown in Figure 6.23 referenced to the center element (row 2, column 2) of each array.



The lack of coplanarity is an artifact of the release etch processes caused by the etch heating effect described in Chapter 5. The larger difference in coplanarity of array elements with and without bonded mirrors is a combination of the back and frontside release etch processes and the much higher temperature seen by mirror devices during frontside release etch. The TiW barrier metal of the inner actuator etches at a faster rate than the TiW barrier metal of the outer actuator after the actuator is released because the inner actuator is hotter. TiW loss reduces $(EI)_{\text{eff},y}$ of the inner actuator beams compared to the outer actuator beams, allowing them to bend more, thus destroying the common-mode residual stress rejection property of the folded electrothermal actuator structure leading to a unidirectional bias angle. Thermally accelerated TiW etching amplifies the effect of natural variation in release etch time between array elements which can be higher than 30 s. The SOI-CMOS-MEMS mirrors can reach temperatures above $300\ ^\circ\text{C}$ after frontside release, while the actuators alone stay below $50\ ^\circ\text{C}$.

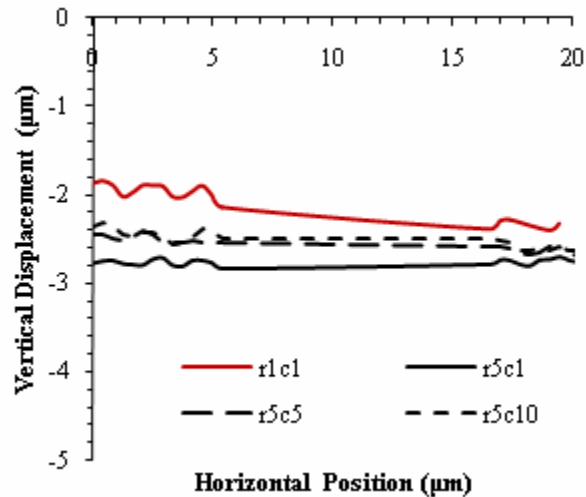
The coplanarity of the pedestals of the 3-D actuators of Figure 6.23 is shown in Figure 6.29. There is a non-zero rest angle on each pedestal of the 3C500 actuators about the x - and y -directions with a range of 2.3° and 2.2° , respectively. The rest angles about the x -axis (Figure 6.29 (b)) are consistent with the inner actuator beams of the set having a reduced ρ_c . The rest angles about the y -axis (Figure 6.29 (a)) do not have a consistent direction, but are smaller in magnitude than those about the x -axis, an effect which may be representative of variation in processes other than the release etch.

FIGURE 6.29 Coplanarity of the 2×2 3C500 actuator array in (a) the x -direction and (b) the y -direction and a representative sample of the 10×10 3C100 actuator array in (c) the x -direction and (d) the y -direction.



The coplanarity of the pedestals of a representative sample of 1A100 actuators is shown in Figure 6.30. The negative height offset of the pedestals occurs because the reference level is a higher level of metal in the stack. The range of rest angles is from -1.3° to 0.3° measured on 13 out of 100 pedestals across the array. The variation likely represents both TiW attack and variations from other process steps.

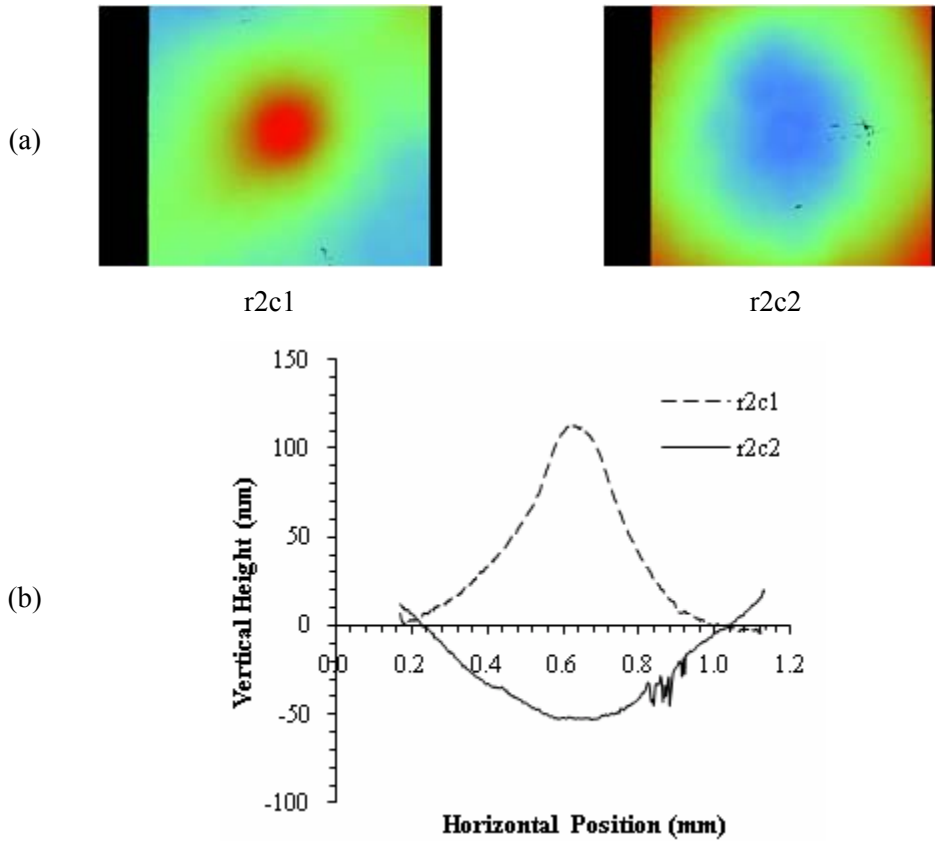
FIGURE 6.30 Coplanarity of representative elements of the 10×10 1A100 actuator array.



6.7.5 Mirror Radius of Curvature and Smoothness

The radius of curvature of a mirror element determines the divergence, or convergence of a light beam reflected from it. The smoothness of the mirror is critical to the amount of optical signal loss due to dispersion. Both of these parameters are measured using a WYKO NT3300. Two representative images of the surface profile of SOI-CMOS-MEMS mirrors are given in Figure 6.31 (a) and the vertical height of each is plotted in Figure 6.31 (a). The mirror radius of curvature is determined by fitting a circle to the height data. For the SOI-CMOS-MEMS mirror array the radius of curvature is measured from -60 mm to -140 mm for mirrors with a profile like r2c1 and from 1.9 m to 4.0 m for mirrors with a profile like r2c2. The reason for the two surface profiles is not understood and requires further investigation. The smoothness of the surface, quantified using average roughness Ra , is output directly by the WYKO NT3300 and ranges from 8 nm to 62 nm across the mirror array.

FIGURE 6.31 (a) Representative examples of the surface profile of mirror elements taken using a WYKO NT3300. (b) Surface height variation over the surface of the two mirrors shown in (a).

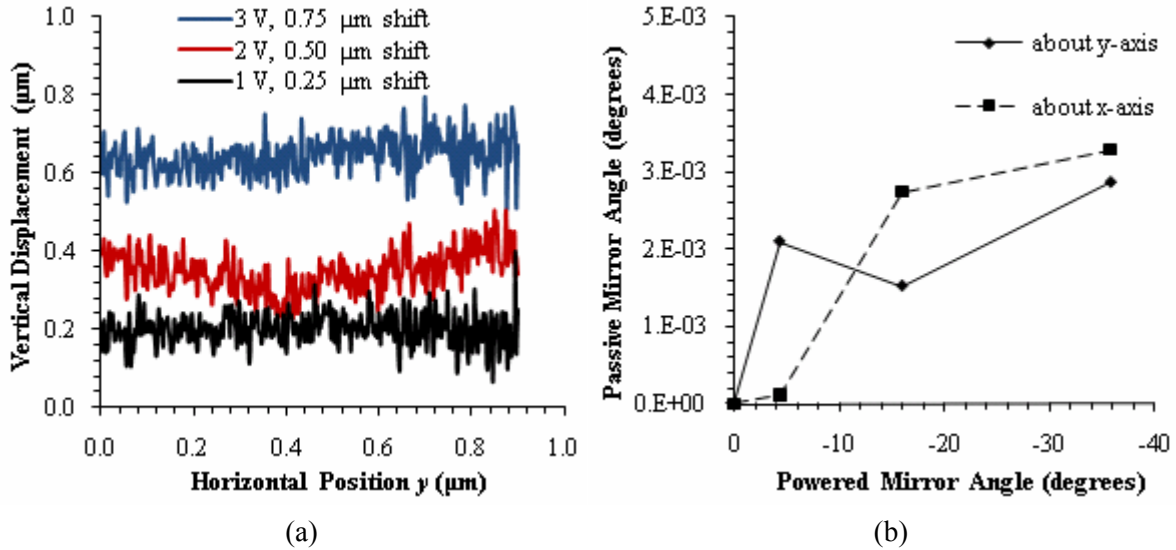


6.7.6 Thermal Cross-talk

Heat spreads. As such, the power dissipated in one mirror can be expected to affect another. Although the folded electrothermal actuator structure for 1-D mirrors is designed to reject common-mode temperature variation, the cross-array gradients in temperature caused by heating individual mirrors is still expected to perturb the rest position of adjacent mirrors. The effect of the perturbation is called “thermal cross-talk” and is measured using a WYKO NT3300 by sweeping the voltage on the central element (r2c2) of a SOI-CMOS-MEMS mirror array and measuring the passive angular displacement of the adjacent mirrors about the x - and y -axes referenced to each mirror element rest angle (see Figure 6.32 (a)). For clarity, the surface profiles at each voltage are shifted from each other by a small amount indicated in the legend. The measured displacements are plotted against the displacement of the powered mirror to extract the angular degree/degree cross-talk shown in Figure 6.32 (b).

Across the array, the maximum thermal cross-talk is measured to be 100 ppm. In making the measurements, it appears the curvature of the mirror changes but this component cannot be quantified at this time and requires further investigation.

FIGURE 6.32 Thermal cross-talk in a SOI-CMOS-MEMS micromirror array. (a) Surface variation of unpowered mirror under the influence of heat dissipated in a powered mirror. (b) Passive mirror angular displacement vs. powered mirror angular displacement.



The effect of scaling on thermal cross-talk has not been investigated, but a few speculations are warranted as a guide to the thoughts of any researcher who may consider this problem in future. Thermal cross-talk due to solid conduction will likely increase as the Si of the anchor decreases in thickness and the spatial separation of the actuator elements decreases. It is shown in Chapter 2 how the power density increases with decreasing scale and this will drive up thermal cross-talk, even as actuator power sensitivity is decreasing. At smaller scales, the post height would be smaller, further increasing the possibility of mirror curvature variation as a component in cross-talk.

6.7.7 Dynamic Response

The dynamic responses of SOI-CMOS-MEMS mirrors and 1-D electrothermal actuators are measured using a Microvision system and are shown in Figure 6.33. The Microvision system processes

stroboscopic image data to extract the motion of a MEMS structure and requires well defined edges, unambiguous features and high contrast to identify and track moving structures.

FIGURE 6.33 Frequency response of (a) 1A1K actuators, (b) 1E1K actuators, (c) SOI-CMOS-MEMS mirrors and (d) 1A100 actuators.

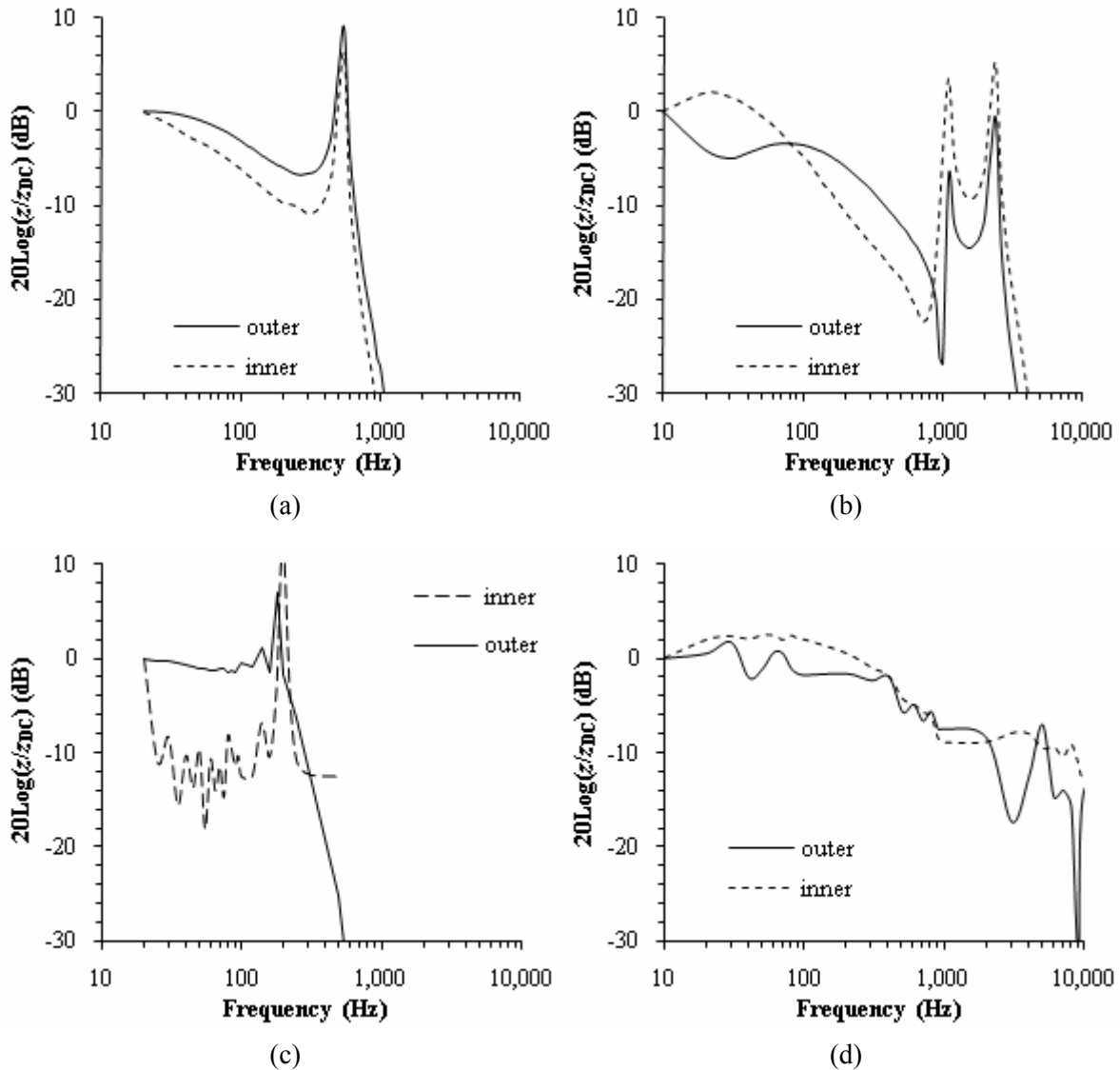


Figure 6.33 (a) and (c) shows the frequency response for 1A1K and 1E1K actuators, respectively, without mirrors. These curves are smooth and the mechanical resonant peaks are well-defined. Voltages are applied that produce low frequency displacements of $\sim 1 \mu\text{m}$, which provide a good signal-to-noise ratio for the measurement (the noise for Microvision measurements on these structures is on the order of 10 nm). However, in the case of SOI-CMOS-MEMS mirrors bonded to 1A1K actuators, the

Microvision has difficulty in processing the data reliably because edge translation is strongly coupled to angular rotation that results in changes in the intensity of the image (i.e. translation is convoluted with image intensity variation). Also, with the addition of the mirror and post mass, the Q of the system increases so voltages must be used that are low enough to ensure the structure doesn't move out of the Microvision ROI at resonance. These voltages produce noisy low frequency displacements of ~ 50 nm. The frequency response of SOI-CMOS-MEMS mirrors is shown in Figure 6.33 (c) and illustrates the noise and instability inherent in the measurement. For example, there is a dip in the response of the outer actuator in Figure 6.33 (c) at 160 Hz - 180 Hz just before the peak at 200 Hz. Analysis of the raw image data shows that the displacement for these frequencies is similar, and possibly larger, in magnitude than at 200 Hz, but the variation in intensity of the image of the mirror disrupts the Microvision image processing.

The first mechanical mode frequency for SOI-CMOS-MEMS mirrors bonded to 1A1K actuators is 200 Hz. The thermal cut-off frequency can't be reliably extracted from the data because of the noise in the measurement so it is necessary to infer $f_{c,th}$ from the frequency responses of the actuators alone. The thermal cut-off of the 1A1K actuator (Figure 6.33 (a)) is 45 Hz for the inner leg and for the outer leg it is 95 Hz. This is consistent with the difference in the thermal isolation of the two actuator legs. The response for both actuators decreases at approximately -10 dB/decade, an effect explained by Messner et al. [128] as being caused by the distributed capacitance of long electrothermal actuator beams with discrete heaters.

The response of the outer leg of the 1E1K actuator has a different form than that of the 1A1K actuator because only half of the outer leg is connected to the anchor, while the other half is connected to the pedestal. The rise in response of the outer actuator has not been analyzed to a degree sufficient to explain its shape and requires further investigation. The net effect, is that the inner leg is faster at 75 Hz while the $f_{c,th}$ of the outer actuator is 20 Hz. No resonance peaks are observed for the 1E100 actuators, but the relative speeds and forms of the responses of the actuator legs is similar to the 1E1K

design, indicating similar dynamics are at work. Due to the small absolute displacements of the 1E00 actuators the responses are noisy and the accuracy of $f_{c,th}$ is questionable, however, both legs have $f_{c,th} = 430$ Hz. The increase in speed is consistent with the scaling behavior predicted in Section 2.4.4.

6.8 Characterization Summary

This chapter characterizes three types of parameters: material properties (ex. Young's modulus) and technology dimensions (ex. layer thicknesses) that feed into analytic models of device behavior, test structure characteristics that represent the compounded effects of material properties and technology dimensions (ex. self-assembly) and device behavior that represents the variations in the other types of parameters coupled with particular design choices (ex. power sensitivity). The trends in the behavior of test structures and fabricated devices are consistent with the models developed in Chapter 2 (ex. the power sensitivity of an actuator depends strongly on its payload). To fully close this loop, additional work is needed to independently extract CTE and thermal conductivities of the respective materials.

The variation in the measured parameters, even considering small sample sizes (min. 3 samples) is large, up to 50% (see trend of vertical radius of curvature in Figure 6.12) and are significantly different from nominal values. This highlights the need to baseline these parameters and monitor them on a run-to-run basis to enable proper understanding of device behavior variation and its sources.

6.8.1 Process Variation and Device Variation

One goal of this research is to use the measured variation in the parameters populating the analytic models of device behavior to predict the expected variation in device behavior. This is important to prevent a designer from making an error of the first kind, or calling a false alarm [120], in which the design is assumed to be deviant when in fact the observed deviation in device performance is due to normal process variations. To make a simple estimate, the individual parameters must be statistically

independent, otherwise accurate knowledge of the covariance is required. This not the case for the layer thicknesses as the total stack thickness is kept within some range of a target value and if one layer increases in thickness the other layers must decrease. However, parameters such as CD bias, m3 Al loss, Young's modulus, CTE, thermal conductivity and residual stress may be statistically independent.

For this work, the variation in m1 and m1Si ILD thickness, Young's modulus, CTE, thermal conductivity and TiW attack are significant in determining the power sensitivity of SOI-CMOS-MEMS mirrors, but a method of measuring TiW attack has not been developed and extracting CTE and thermal conductivity has not been employed, so these parameters have not been tracked. The variation in coplanarity of mirror elements is a function of TiW attack that varies on an element-to-element basis. At this time, the power sensitivity is the only tracked parameter that can be used to predict some of the variation in SOI-CMOS-MEMS mirror performance. Based on a 3σ control scheme and the measured run-to-run variance in thermal sensitivity γ from Figure 6.14 (d) the power sensitivity under normal variation of SOI-CMOS-MEMS mirrors bonded to 1A1K actuators can range from $1.6 \text{ deg}\cdot\text{mW}^{-1}$ to $2.3 \text{ deg}\cdot\text{mW}^{-1}$ for the inner actuator and $-0.8 \text{ deg}\cdot\text{mW}^{-1}$ to $-1.1 \text{ deg}\cdot\text{mW}^{-1}$ for the outer actuator.

7

SOI-CMOS-MEMS: Impact and Outlook

“It’s not the mountain we conquer, but ourselves.”

- Edmund Hillary

“I have climbed my mountain, but I must still live my life.”

-Tenzing Norgay

7.1 A Summing Up

SOI-CMOS-MEMS and the analytic description of folded electrothermal actuators with discrete heaters is the main contribution of the work described in this dissertation. Other contributions to the research community have been made in etch process modeling and the understanding of etch artifacts like TiW barrier metal attack during release etch.

SOI-CMOS-MEMS is a fabrication technology with the demonstrated capability of large range of actuator motion ($\pm 45^\circ$) with high fill factor (90%) for mm-scale devices. The power consumption of the fabricated electrothermal mirrors is less than 50 mW for FSD, which is better than the power consumption reported for mirrors actuated by electrothermal and other methods [29][34]. SOI-CMOS-MEMS in its present form cannot be scaled to dimensions 500 μm and lower because of fluidic effects that cause undesirable spreading of bonding adhesive and post breakage during BOX removal in post

fabrication. A mask revision is the first step in solving the problem of uncontrolled adhesive spread and vapor phase HF etching is available to eliminate post breakage.

The folded electrothermal actuator topologies investigated in this work are described analytically and the models are shown to be consistent with characterization data for mirrors and actuators at various scales. The performance advantage of bimorphs with discrete heaters over multimorphs beams with distributed heaters is drawn out of the theoretical analysis and backed up with direct experimental validation on test structures. Detailed measurements of foundry CMOS layer thicknesses explain much of the variation observed in self-assembly displacements and device response. Characterization of material properties like Young's modulus provide a means to explain some of the variation observed from foundry run to foundry run. Measurements made on test structures validate the electrothermal actuator response dependence on stack composition, heater placement, payload dimensions and beam dimensions predicted by the analytical models.

In developing SOI-CMOS-MEMS it became necessary to generate models for the application of ARDEM for the control of etch depth and etch uniformity. The model is analytically tractable and, stripped of its spatial and pattern-based variation components, can be used by researchers to easily estimate etch depth based on the characteristic dimension of a feature, provided their process has been shown to adhere to Rangelow's criteria for the validity of the Coburn and Winter's ARDE model.

A significant contribution to the basic understanding of device variation caused by MEMS processing is made in the investigation of etch heating during release etch. It is shown how isotropic Si etching by F is the main source of temperature increases for this Si etch process and chamber. The dependence on structure dimensions is captured in a power balance model of etch heating that can be applied to any etch process whose plasma parameters are known. The proportion of exothermic reaction heat absorbed by released MEMS structures from the etching of Si by F is quantified for possibly the first time, which represents a fundamental scientific contribution.

7.2 Conclusions

The complete elimination of TiW barrier metal attack during plasma release etch is essential to reduce variation in SOI-CMOS-MEMS arrayed devices and make the technology a viable alternative for microsystems designers. The release etch strategies adopted to overcome catastrophic electrical failure due to W via attack are sufficient to produce working micromirror devices, but are insufficient to the task of eliminating TiW barrier metal attack that drives within array coplanarity variation. Without this, the complexity of implementing SOI-CMOS-MEMS micromirror devices in optical systems increases due to the need to characterize every chip for array coplanarity deviations and power sensitivity variations and to implement a control scheme to compensate for these effects.

Control over layer thicknesses must be given to the designer if SLM-scale micromirror devices are to be realized in CMOS-MEMS or SOI-CMOS-MEMS. As the device scale reduces and the array pitch decreases, it is shown analytically and demonstrated experimentally that the power sensitivity, i.e. the angular rotation per mW power input, rapidly decreases due to its linear dependence on actuator length and the limitations on the sustainable temperature gradients imposed by the CMOS material system. It is shown that the only way to recover this adverse scaling relationship in the context of CMOS is to decrease the thickness of the metal, oxide and poly layers in a multimorph distributed heater actuator. The other alternative takes the designer away from CMOS into a custom process with an optimized material system.

Power density increases exponentially with decreasing device pitch because more power is needed to achieve the maximum temperatures that generate the full-scale device deflections. This is a function of the decrease in thermal isolation between the legs of the folded electrothermal actuator topology and between the heaters and the thermal grounds with decreasing pitch. Mechanical latching is unavoidable if continuous operation must be provided or micromirror positions must be held indefinitely. However, if scan range is a critical specification, electrothermal actuation is superior for pitches greater than approximately 200 μm .

7.3 Future Directions

A great deal has been learned in this work about the issues of integrating microscale components with CMOS-MEMS that have use for the wafer manufacturer and the single-chip researcher. Etch depth control has been improved through the use of ARDEM and etch ballasting and the understanding of the mechanisms of device heating during plasma release etch mean that forbidding regions of the process space are no longer inhabited by dragons. With ARDEM models in hand, it is feasible for MEMS manufacturers to compensate for process-chamber-based spatial etch depth variation by varying ARDEM patterns across a wafer. The algorithms to generate complex geometries with equivalent etch rates must be developed to realize this kind of goal, but may be no more difficult to implement than optical pattern correction algorithms. The converse is also feasible, to work backwards from a desired multi-level depth profile to the single ARDEM mask that would produce it. The goal in such a case could be to tailor Si breakthrough times to particular structures or to compensate for unavoidable ARDE effects due to the frontside design. This appears to be an algorithm development project that would proceed hand-in-hand with process research and characterization.

The observations made during post etch development indicate there is also a need for modeling of ARDP and lateral ARDE effects. Neither topic has been widely investigated in the literature but both are necessary to understand the issues of design-based Si release etch variation. Effective modeling of lateral ARDE could provide other useful etch techniques for the production of honeycomb structures that could be used to enhance thermal convection and conduction through air. The problem will likely require revisitation of Clausing's theoretical development of the vacuum conductance correction factor for analytic development of its angular dependence.

The strongly worded conclusion in Section 7.2 about the elimination of TiW barrier metal attack presages the call for the investigation of an independent sidewall passivation process following frontside oxide etch but preceding any bonding or release etch process. It was proposed to investigate such a process as part of this dissertation but the immediate need was eliminated by the "success" of alter-

nate release etch process strategies indicated by the conclusions of the IR etch heating investigation. However, the avoidance of the development of a sidewall passivation process proved to be a mistake as TiW attack appears to be the dominant cause of coplanarity loss in micromirror arrays. The issue does not affect only large angle micromirror arrays in SOI-CMOS-MEMS but is observed by Iyer [47], Lackdawala [126] and Zhu [66] in other fabrication technologies. The sidewall spacer approach of the semiconductor industry is still a promising candidate that could be implemented using PECVD oxide deposition or atomic layer deposition. Passivation adhesion and integrity through release etch must be considered in such an investigation.

The issues with post etch, adhesive application and bonding can be overcome with small modifications to mask designs. Once the other issues hindering device scaling to SLM dimensions are overcome, these process steps should be revisited to demonstrate SOI-CMOS-MEMS mirror arrays for these applications.

Independent measurement of CTE and thermal conductivity and their tracking across fabrication technologies and from foundry run to foundry run should be done to enable accurate predictions of device behavior and its variation using the models in Chapter 2.

Finally, other payloads should be investigated for SOI-CMOS-MEMS and/or an Alternate-material-CMOS-MEMS fabrication technology. The technology is ready for mm-scale devices to be integrated with CMOS-MEMS and could be readily enhanced by developing techniques to electrically interconnect payloads such as hard-disk drive read/write heads to CMOS-MEMS actuators.

Appendix A - SOI-CMOS-MEMS Process Flow



A.1 CMOS

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	CMOS	Formation of devices in CMOS technology	CMOS chip with passivation openings to bond pads.	CMOS foundry		Foundry processing	JAZZ Semiconductor - 3 month manufacturing and shipment lead time from tape-out.
0110	Inspect	Inspect CMOS die and bin according to quality	Bins of varying quality die for use as test die and device die	Olympus MX80 microscope	CMOS die		
0120	Measure	Measure CMOS chip thickness	Characterize the thickness of the returned CMOS chips to enable appropriate choice of tile thickness	micrometer	CMOS die		Measure a minimum of 5 chips to get a range from across the wafer.

A.2 CMOS-MEMS

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1000	Clean	Clean CMOS die and Si tiles	Particulates and organics removed from both surfaces of the CMOS	wet bench ultrasonic bath beaker petri dish N ₂ gun	acetone IPA N ₂	Ultrasonic Time - 10 min	Put 2 die/tiles per beaker and fill beaker with acetone ~ half way. Fill the ultrasonic bath with water until it reaches the level of the acetone in the beaker. Use small petri dish filled with IPA to rinse off acetone. Use N ₂ gun to dry the die and tiles.
1010	Deposit	Deposit Al on backside of CMOS die	100 nm of Al	Perkin Elmer 8L	Al	Pressure - 5 mT Power - 130 W DC Time - 1 min Heat Ex. Temp - 14 °C	Ar is used as the bleed gas. The flow of the Ar is adjusted to achieve the desired pressure. This layer acts as the mask for the final CMOS-MEMS actuator release etch. Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
1020	Tile	Tile CMOS die with Si	1 - 4 CMOS die surrounded by tiles of appropriate thickness to ensure uniform coat of resist	wet bench	Kapton tape Si tiles		CMOS will be mounted face down, so backside of CMOS die and backside of tile should face up. Kapton tape holds the tiled arrangement together for transport.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1030	Coat	Coat 3" glass carrier wafer with resist	A uniform ~4 μ m layer of resist to act as an adhesion layer for the CMOS die and Si tiles	Solitec photoresist spinner	3" round glass wafer AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 1800 rpm	Do not allow solvent to fully evaporate before placing the CMOS die and Si tiles on the carrier. Spin rate can be adjusted to increase or reduce solvent loss. However, too thick a resist layer can make it very difficult to achieve planarity across all CMOS die.
1040	Mount	Mount CMOS die and Si tiles on glass wafer	Uniform height of CMOS and silicon tile surface with ~5 μ m gap between die and tiles to ensure good resist coat	hotplate		Temp - 90 °C Time - as required	Mount tiled die on the glass wafer and rearrange them to reduce the gaps between die and tiles to ~5 μ m. Use the hotplate to soften the resist during the rearrangement. The gap between the CMOS die prevents buckling during backside etch.
1050	Clean	Clean surface of die and tiles	Clean CMOS backside surface in preparation for resist coat	cotton swab	acetone		Blot excess acetone from the swab before cleaning the die, otherwise the excess acetone will dissolve the resist between the die and lead to bubbling during the bake operation.
1060	Inspect	Inspect the die and tiles for defects	Clean and planar die and tiles with gaps minimized and no serious chips or cracks in tiles	Olympus MX80 microscope			Planarity over the surface of the die and tiles affects resist uniformity.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1070	Coat	HMDS coat	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense enough HMDS to coat the die and the tiles. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
1080	Coat	Resist coat	~1 μm resist with uniform die surface coverage	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a puddle that coats both the die and tiles.
1090	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
1100	Expose	Expose "no grating" backside pattern	Exposed resist	Heidelberg DWL66	mask as required by design	Write-head - 10 mm Filter - 31% Intensity - as required by equipment state Defocus - 2047	Perform DWL backside alignment calibration prior to chip alignment. Align to inner corner of bottom left-hand mirror (ie column 1, row 1).
1110	Develop	Develop exposed resist	Clean backside no-grating mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish 3" wafer holder DI gun N ₂ gun	AZ Developer DI water N ₂	Temp - 20 °C Time - ~2.0 min + 0.5 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1120	Etch	Backside Al wet etch	Patterned Al	acid bench petri dish 3" wafer holder DI gun N ₂ gun	Al etchant DI water N ₂	Temp - 20 °C Time - ~2.5 min + 0.5 min overetch	Visually endpoint the etch. Look for non-uniformity in the etching of the Al and endpoint when the last Al is gone. Al etchrate ~0.6 nm/s. Quench the etch in a petri dish of water before final rinse and dry.
1130	Inspect	Inspect the die for complete Al etch	Clean "no-grating" mask pattern transferred to Al and no residual Al in the open areas	Olympus MX80 microscope			
1140	Demount	Remove chips from glass carrier wafer	Intact individuated die with backside "no-grating" pattern	hotplate		Temp - 90 °C Time - as needed	Heat glass wafer on hotplate and apply light shearing force to the short edge of the tiles away from the die.
1150	Strip	Clean resist from front and back surface of die	Clean surface of die in preparation for backside "grating" litho	petri dish N ₂ gun	acetone IPA N ₂		Soak briefly in acetone in petri dish before transferring to petri dish with IPA to rinse off acetone.
1160	Tile	Tile CMOS die with Si	1 - 4 CMOS die surrounded by tiles of appropriate thickness to ensure uniform coat of resist	wet bench	Kapton tape Si tiles		Re-use the tiles from the first, Al-masking step. CMOS will be mounted face down, so backside of CMOS die and backside of tile should be face up. Kapton tape holds the tiled arrangement together for transport.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1170	Coat	Coat 3" glass carrier wafer with resist	Form a uniform ~4 μ m layer of resist to act as an adhesion layer for the CMOS die and Si tiles	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 1800 rpm	Do not allow solvent to fully evaporate before placing the CMOS die and Si tiles on the carrier. Spin rate can be adjusted to increase or reduce solvent loss. However, too thick a resist layer can make it very difficult to achieve planarity across all CMOS die.
1180	Mount	Mount CMOS die and Si tiles on glass wafer	Uniform height of CMOS and silicon tile surface with ~5 μ m gap between die and tiles to ensure good resist coat	hotplate	3" round glass wafer	Temp - 90 °C Time - as needed	Mount tiled die on the glass wafer and rearrange them to reduce the gaps between die and tiles to ~5 μ m . Use the hotplate to soften the resist during the rearrangement. The gap between the CMOS die prevents buckling during back-side etch.
1190	Clean	Clean surface of die and tiles	Clean CMOS backside surface in preparation for resist coat	cotton swab	acetone		Blot excess acetone from the swab before cleaning the die, otherwise the excess acetone will dissolve the resist between the die and lead to bubbling during the bake operation.
1200	Inspect	Inspect the die and tiles for defects	Clean and planar die and tiles with gaps minimized and no serious chips or cracks in tiles	Olympus MX80 microscope			Planarity over the surface of the die and tiles affects resist uniformity.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1210	Coat	HMDS coat	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Two HMDS coats are applied to the die with the same spin conditions. Dispense enough HMDS to coat the die and the tiles. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
1220	Coat	Resist coat	~4.5 um of resist with uniform die surface coverage	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 2000 rpm	Two coats are applied to the die with the same spin conditions. Dispense a puddle that coats both the die and tiles. Apply the second coat immediately after the first spin is completed.
1230	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
1240	Expose	Expose "grating" backside pattern	Exposed resist	Heidelberg DWL66	mask as required by design	Write-head - 10 mm Filter - 31% Intensity - as required by equipment state Defocus - 2047	Perform DWL backside alignment calibration prior to chip alignment using "bsalign". Align to inner corner of bottom left-hand mirror (ie column 1, row 1).
1250	Develop	Develop exposed resist	Clean backside grating mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish 3" wafer holder DI gun N ₂ gun	AZ developer DI water N ₂	Temp - 20 °C Time - ~5.0 min + 0.5 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry. Gentle dry needed to protect fine grating pattern.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1260	Inspect	Inspect the die for complete development	Clean backside mask pattern transferred to resist, no bridging of features and good edge definition	Olympus MX80 microscope			
1270	Bake	Hardbake resist	Stabilize and harden resist in preparation for the silicon etch process	Blue M Stabiltherm gravity oven		Temp - 90 °C Time - 30 min	
1280	Mount	Mount glass wafer on 4" backside etch carrier wafer	Good adhesive and thermal contact between carrier wafer and glass wafer		150 °C Revalpha Nitto Denko heat release tape 4" Si sub with resist		Use a 3" diameter circle of tape to mount the glass wafer. Ensure there is adequate room at the edge of the 4" carrier for the STS clamp fingers to avoid the tape surface, otherwise handling errors can occur in the STS due to sticking.
1290	Etch	Backside silicon etch	Etch silicon to a depth of 240 μm in the actuator regions without eroding all resist and maintain full thickness of silicon in masked areas	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~105 min polymer rem. - 1 min isotropic - 5 min See Appendix C for detailed Si etch recipe conditions.	
1300	Inspect	Inspect the die for complete silicon etch	Backside grating structure completely removed and ~240 μm etch depth in the actuator region	Olympus MX80 microscope			

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1310	Demount	Remove die from glass carrier wafer	Intact individuated die with backside pattern	hotplate		Temp - 90 ° C Time - as needed	Heat glass wafer and 4" Si sub carrier on hotplate and apply light shearing force to the short edge of the tiles away from the die.
1320	Strip	Clean resist from front and back surface of die	Clean surface of die in preparation for frontside etch	beaker ultrasonic bath petri dish N ₂ gun	acetone IPA N ₂	Ultrasonic Time - 8 min	Put 2 dice per beaker and fill beaker with acetone ~ half way. Fill the ultrasonic bath with water until it reaches the level of the acetone in the beaker.
1330	Etch	Frontside oxide etch	Remove oxide from the surface of the die to expose MEMS structures and silicon surface.	Plas-matherm 790		See Appendix C for oxide etch recipe conditions	
1340	Inspect	Inspect the die for complete oxide etch	Complete oxide etch on all Si surfaces	Olympus MX80 microscope			Narrow gaps between two metal4 structures are the last features to clear of oxide. Check these areas closely. If further etching is required, do it in 15 min steps.
1350	Store	Store CMOS-MEMS die for further processing	Secure low humidity storage	dry box		Temp - 20° C	

A.3 SOI Mirror-Post

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2000	Clean	Clean SOI wafer	Surface free of organics and particulates	wet bench Semitool PSC-101 4" wafer holder N ₂ gun	SOI wafer acetone IPA N ₂	Default SRD recipe	Use a double-sided polished SOI wafer. This flow assumes a 25 μm device layer, 1 μm buried oxide and 500 μm handle layer is used. Spin/rinse/dry following acetone/IPA rinse. **For very thin SOI wafers the Semitool can't be used. Hold the wafer like a CD while rinsing and drying. Avoid "Tacoma Narrows" effect while drying.
2010	Deposit	Deposit Al on post/handle side	100 nm of Al	Perkin Elmer 8L	Al	Pressure - 5 mT Power - 130 W Heat Ex. Temp - 14 °C Time - 1 min	Ar is used as the bleed gas. The flow of the Ar is adjusted to achieve the desired pressure. Al is deposited on the post/handle side first to protect the quality of the mirror surface. Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
2020	Clean	Clean SOI wafer	Remove any particulates that may have contaminated the mirror/device side while the post/handle side was being coated with Al	wet bench Semitool PSC-101 4" wafer holder N ₂ gun	acetone IPA N ₂	Default SRD recipe	Spin/rinse/dry following acetone/IPA rinse.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2030	Deposit	Deposit Al on mirror/device side	100 nm of Al	Perkin Elmer 8L	Al	Pressure - 5 mT Power - 130 W Heat Ex. Temp - 14 °C Time - 1 min	Ar is used as the bleed gas. The flow of the Ar is adjusted to achieve the desired pressure. Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
2040	Coat	HMDS coat mirror/device side	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense enough HMDS to coat the wafer. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
2050	Coat	Imaging resist coat mirror/device side	Resist thickness ~1 μm with uniform wafer surface coverage	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" diameter puddle.
2060	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
2070	Coat	Protective resist coat post/handle side	Resist thickness ~1 μm with uniform wafer surface coverage	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" diameter puddle.
2080	Bake	Resist solvent removal	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 5 min	Prop the mirror/device side of the wafer so that the bulk of the surface is not contacting anything. This will reduce mirror defects and scratches.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2090	Expose	Expose mirror/ device side	Exposed resist	Süss MA56	mask as required by design	Time - 1.8 s	Use "First Mask" setting as no alignment is required. Center the stage before loading the wafer.
2100	Develop	Develop exposed resist	Clean mirror mask pattern transferred to resist, no bridg- ing of features and good edge defini- tion	wet bench petri dish 4" wafer holder DI gun N ₂ gun	AZ devel- oper DI water N ₂	Temp - 20 °C Time - ~0.8 min + 0.2 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry.
2110	Inspect	Inspect the devel- oped pattern	Clean mirror mask pattern transferred to resist, no bridg- ing of features and good edge defini- tion	Olympus MX80 microscope			
2120	Etch	Mirror Al wet etch	Patterned Al	acid bench petri dish 4" wafer holder DI gun N ₂ gun	Al etchant DI water N ₂	Temp - 20 °C Time - ~2.5 min + 0.5 min overetch	Visually endpoint the etch. Look for non-uniformity in the etching of the Al and endpoint when the last Al is gone. Al etchrate ~0.6 nm/s. Quench the etch in a petri dish of water before final rinse and dry.
2130	Inspect	Inspect the etched pattern	Clean mirror mask pattern transferred to Al and no resid- ual Al in the open areas	Olympus MX80 microscope			
2140	Strip	Clean resist from front and back surface of wafer	Clean surface of die in preparation for post/handle side patterning	4" wafer holder N ₂ gun	acetone IPA N ₂		

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2150	Coat	Protective resist coat mirror/device side	Resist thickness ~1 μm with uniform wafer surface coverage	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" diameter puddle.
2160	Bake	Resist solvent removal	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 5 min	
2170	Coat	HMDS coat post/handle side	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense enough HMDS to coat the wafer. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
2180	Coat	Imaging resist coat post/handle side	Resist thickness ~1 μm with uniform wafer surface coverage	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" diameter puddle.
2190	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
2200	Expose	Expose post/handle side	Exposed resist	Süss MA6	mask as required by design	Mode - Vac Time - 50 s	
2210	Develop	Develop exposed resist	Clean post mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish DI gun N ₂ gun	AZ Developer DI water N ₂	Temp - 20 °C Time - ~0.8 min + 0.2 min overdevelop	Quench the develop process in a petrie dish of DI water prior to DI gun rinse and N2 dry. Gentle dry needed to protect fine grating pattern.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2220	Inspect	Inspect the developed pattern	Clean post mask pattern transferred to resist, no bridging of features and good edge definition	Olympus MX80 microscope			
2230	Etch	Post Al wet etch	Patterned Al	acid bench petri dish 4" wafer holder DI gun N ₂ gun	Al etchant DI water N ₂	Temp - 20 °C Time - ~2.5 min + 0.5 min overdevelop	Visually endpoint the etch. Look for non-uniformity in the etching of the Al and endpoint when the last Al is gone. Al etchrate ~0.6 nm/s. Quench the etch in a petri dish of water before final rinse and dry.
2240	Inspect	Inspect the etched pattern	Clean post mask pattern transferred to Al and no residual Al in the open areas	Olympus MX80 microscope			
2250	Mount	Mount wafer on dicing frame	Dicing tape laminated on backside of wafer with no bubbles	hotplate laminator dicing frame	dicing tape		
2260	Scribe	Scribe mirror/device side	Scribe lanes in the mirror side that extend ~15 um deeper than the buried oxide	Kulicke and Soffa dicing saw		Chuck-up Height - 0.565 mm Dicing saw conditions. See Appendix C for detailed conditions.	Use a chuck up height of 550 μm. **Chuck up height must be adjusted for wafers of different handle, device and buried oxide thickness.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2270	Dice	Dice wafer into individual die	Straight, clean dicing street dividing the wafer into sections 3 dice wide by 6 dice long	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	
2280	Demount	Demount individual die	Intact, individual mirror-post die				Remove the sections from the dicing tape. Be careful not to bend the sections because they will break along the scribe lines. Instead, peel the dicing tape slowly from the back of the sections while holding the section still.
2290	Strip	Clean resist from front and back surface of the sections	Clean surface of sections in preparation for etching	petri dish ultrasonic bath N ₂ gun	acetone IPA N ₂		Ultrasonic the sections in a beaker filled with acetone. Any resist residue on the mirror/device side will lead to a failure of the heat release tape to properly release after etching.
2300	Store	Store diced sections for later use	Secured sections with minimal risk of pattern damage	wafer carrier			Put a circular paper filter below and above the sections to prevent them moving excessively.
2310	Mount	Mount die on a carrier wafer	Post die section uniformly adhered to the carrier using heat release tape with good thermal contact between the die and the carrier		post etch carrier wafer 150° C heat release tape		Cut a 2" x 2" section of heat release tape and laminate it to the carrier wafer. Place the section on the tape and apply slight pressure to the edge of the section normal to the corner so there is both a downward and sideways force component.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2320	Tile	Tile silicon bal-last around the die	Post die section surrounded along its perimeter by 1 cm of Si		1 mm thick x 5 mm x 10 mm Si tiles		Place the Si tiles as close to the edge of the post die section as possible.
2330	Etch	Post/handle side silicon etch	Intact posts with vertical sidewalls on the posts and the perimeter wall of each chip and no buried oxide	STS-ASE	SF ₆ C ₄ F ₈ O ₂	anisotropic - ~420 min polymer rem. - 1 min isotropic - 1 min polymer rem. -2 min See Appendix C for detailed Si etch recipe conditions.	The final polymer removal step is necessary to expose the buried oxide so it can be etched by the buffered HF.
2340	Inspect	Inspect the etched section	Intact posts with vertical sidewalls on the posts and the perimeter wall of each chip and no buried oxide break-through	Olympus MX80 microscope			Look for underetched silicon in the open areas, and any signs of misshapen sidewalls on the posts. It may be necessary to sacrifice some die for the sake of the others and a yield less than 18 die should be expected.
2350	Demount	Demount singulated die from carrier	Individual die	hot plate		Temp - 150 °C Time < 1 min	Observe the release of the heat release tape very closely to see which edge pops up first on each die. Gently push the die along the opposite edge from any edge still adhering to the tape.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2360	Etch	Buried oxide HF etch	Complete buried oxide removal	acid bench teflon bowls teflon tweezers (sharp tip) 1.7 mL dropper personal protective equipment DI gun N ₂ gun	Buffered HF DI water IPA N ₂	Temp - 20 °C Time - 10 min + 1 min overetch	Use the dropper to dispense an amount of HF into the cavity formed by the post die perimeter wall so that the meniscus is level with the wall. Do a quench in a separate teflon bowl and a final rinse in another teflon bowl. Completion of the process will be obvious as the Si surface will dewet.
2370	Sort	Identify good die for device bonding	Bin the singulated die into bins for later use.	Olympus MX80 microscope			
2380	Store	Store singulated die for later use	Secured die with minimal risk of post damage.	Die carrier			

A.4 Flip-chip Bonding

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3000	Charge	Fill dip tray with epoxy	~40 μm thick layer of epoxy in the reservoir of a dip tray	1 mL syringe 26 gauge hypodermic needle mirror-post dip tray	Epo-Tek 377	Temp - 20 $^{\circ}\text{C}$	Dispense a single drop of epoxy into the well of the dip tray. Use the needle to spread the epoxy evenly across the well so it contacts but does not overflow the perimeter boundary wall of the reservoir.
3010	Coat	Dip the ends of the posts into epoxy	Uniform ~40 μm of epoxy on the ends of the posts	M9-A bonder tool mirror-post diffuser plate		Force - 200 g Temp - 20 $^{\circ}\text{C}$ Time - 10 s	The M9-A is operated manually for the dipping process because the automated program turns off the vacuum at the end of bonding process leaving the mirror-post die on the dip tray. The mirror-post die remains on the upper chuck after dipping until the bonding operation.
3020	Diebond	Flip-chip bond the CMOS-MEMS and mirror-post die	Intact and bonded SOI-CMOS-MEMS die	M9-A bonder tool mirror-post diffuser plate CMOS diffuser plate		Force - 200 g Temp - 150 $^{\circ}\text{C}$ Time - 15 min	CMOS on lower chuck, mirror-post on the upper chuck. The M9-A is operated manually for the bonding process but could be automated. The force is allowed to float as the temperature increases. The force at 150 $^{\circ}\text{C}$ is ~1500 g. The vacuum diffuser plate also releases with the bonded die and care must be taken in lifting the diffuser off of the bonded die.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3030	Bake	Finish the epoxy cure	Fully cured epoxy	Blue M Sta-biltherm gravity oven		Temp - 150 °C Time - 60 min	The cure schedule published by the manufacturer is 5 min at 150 °C, however cure time increases as epoxy volume decreases. The correct cure schedule has not been characterized but the cure schedule used here has proved sufficient.
3040	Mount	Mount the die on a carrier wafer	Uniformly adhered die mirror side down on the carrier wafer		release etch carrier wafer 150 °C heat release tape		The die needs to be pressed down onto the heat release tape, but care must be taken not to generate a shearing force that could break the flip-chip bond.
3050	Etch	CMOS-MEMS release etch	Fully released, electrically and mechanically intact CMOS-MEMS actuator	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~20 min polymer rem. - 1 min isotropic - 1 min See Appendix C for detailed Si etch recipe conditions.	Visually endpoint the etch process by watching for the motion of the mirrors as they release.
3060	Inspect	Inspect for fully released CMOS-MEMS actuators	Fully released, electrically and mechanically intact CMOS-MEMS actuator	Olympus MX80 microscope			

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3070	Demount	Remove die from carrier wafer	Intact SOI-CMOS-MEMS die	hotplate		Temp - 90 °C Time - <1 min	The die will pop up off the heat release tape when the tape releases. Watch closely to identify if any side continues to adhere to the tape. Push gently on a corner of the mirror-post die that is opposite the side which is still adhering. Generate a shearing force to break any residual adhesion before attempting to pick the die up. Pick the fully released die up on the CMOS-MEMS edge away from the mirror-post die.
3080	Mount	Mount the die on a carrier wafer	SOI-CMOS-MEMS die uniformly adhered to the carrier wafer CMOS side down using heat release tape with good thermal contact between the die and the carrier		release etch carrier wafer 150 °C heat release tape		The die needs to be pressed down onto the heat release tape. Press at the edges of the CMOS but take care not to contact the mirror-post die or the bonds will break.
3090	Etch	Mirror release etch	Fully released, electrically and mechanically intact SOI-CMOS-MEMS devices	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~10 min See Appendix C for detailed Si etch recipe conditions.	

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3100	Inspect	Inspect for fully released SOI-CMOS-MEMS devices	Fully released, electrically and mechanically intact SOI-CMOS-MEMS devices	Olympus MX80 microscope			
3110	Demount	Remove die from carrier wafer	Intact SOI-CMOS-MEMS die	hotplate		Temp - 90 °C Time - <1 min	The die will pop up off the heat release tape when the tape releases. Watch closely to identify if any side continues to adhere to the tape. Push gently on a corner of the CMOS-MEMS die that is opposite the side which is still adhering. Generate a shearing force to break any residual adhesion before attempting to pick the die up. Pick the fully released die up on the CMOS-MEMS edge away from the mirror-post die.
3120	Store	Store SOI-CMOS-MEMS die for packaging	Secure low humidity storage	dry box		Temp - 20 °C	

A.5 Packaging

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
4000	Mount	Mount die on package	Die level and adhered to package		40 pin DIP package silver paste		Use the minimum amount that will provide adhesion. The risk with too much paste is that the actuator will be fouled by the paste or the range of motion will be decreased.
4010	Cure	Set and harden silver paste	Hardened silver paste	dry box		Temp - 20 °C Time - minimum 1 hour	
4020	Bond	Bond gold wire to pads and DIP traces	Gold wire leads attached from DIP traces to die	West Bond 4500E wire-bonder		Boeing bonding conditions	Bond pads should not be shorted and wire loops should not protrude above the plane of the package surface. Use manual mode of wirebonder. Use a heater to raise the temperature of the package and device to 70 °C.
4030	Test	Test electrical functionality of mirrors in the array	Ensure electrical contact, actuation and range of motion	probe station micromanipulators WYKO NT3300 Microvision	<7 μm radius probe needles		
4040	Cap	Mount lid to package	Wirebonded die secured and protected beneath package lid		DIP lid tape		
4050	Store	Store for further testing or shipment	Intact die fully characterized or in customer's hands				

Appendix B - Auxiliary Process Flows



B.1 Epoxy Dip Tray

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Coat	HMDS coat	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	500 μm thick 100 mm Si wafer HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense enough HMDS to coat the die and the tiles. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
0110	Coat	Resist coat	~ 2 μm resist with uniform die surface coverage	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" puddle.
0120	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 $^{\circ}\text{C}$ Time - 30 min	
0130	Expose	Expose "dip-tray" mask	Exposed resist	Süss MA56	mask as required by design	Time - 2.5 s	Use "First Mask" setting as no alignment is required. Center the stage before loading the wafer.
0140	Develop	Develop exposed resist	Clean diptray mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish 100 mm wafer holder DI gun N ₂ gun	AZ developer DI water N ₂	Temp - 20 $^{\circ}\text{C}$ Time - ~ 0.8 min + 0.2 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0150	Etch	Silicon etch	Etch silicon to a depth of 40 μm in wall regions	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~10 min polymer rem. - 1 min isotropic - 5 min See Appendix C for detailed Si etch recipe conditions.	
0160	Strip	Clean resist from front of wafer	Clean surface of wafer	100 mm wafer holder N ₂ gun	acetone IPA N ₂		Rinse with acetone followed by IPA. Do not allow acetone to dry on the surface of the wafer
0170	Mount	Mount wafer on dicing frame	Dicing tape laminated on backside of wafer with no bubbles	hotplate laminator dicing frame	dicing tape		
0180	Dice	Dice wafer into sections	Straight, clean dicing street dividing the wafer into individual diptrays	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	
0190	Demount	Demount individual diptrays	Intact, individual diptrays				Remove the sections from the dicing tape. Peel the dicing tape slowly from the back of the sections while holding the section still.
0200	Clean	Clean diptrays	Particulates and organics removed from diptray surfaces	wet bench ultrasonic bath beaker petri dish N ₂ gun	acetone IPA N ₂	Ultrasonic Time - 10 min	Put 2 diptrays per beaker and fill beaker with acetone ~ half way. Fill the ultrasonic bath with water until it reaches the level of the acetone in the beaker. Use small petri dish filled with IPA to rinse off acetone. Use N ₂ gun to dry the die and tiles.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0210	Deposit	Deposit Al on diptray	100 nm of Al	Perkin Elmer 8L	Al	Pressure - 5 mT Power - 130 W Heat Ex. Temp - 14 °C Time - 1 min	Al coat is needed to enable the epoxy to wet the diptray, otherwise the epoxy sits in a drop in the dip tray. Ar is used as the bleed gas. The flow of the Ar is adjusted to achieve the desired pressure. Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
0220	Store	Store diptray for later use	Secure low humidity storage	dry box		Temp - 20° C	

B.2 Flip-chip Vacuum Diffuser

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Coat	HMDS coat	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	220 μm thick double-sided polished 100 mm Si wafer HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	**For very thin wafers the Semi-tool can't be used. Hold the wafer like a CD while rinsing and drying. Avoid "Tacoma Narrows" effect while drying. Dispense enough HMDS to coat the die and the tiles. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
0110	Coat	Resist coat	~ 2 μm resist with uniform die surface coverage	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense a 1" puddle.
0120	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 $^{\circ}\text{C}$ Time - 30 min	
0130	Expose	Expose "diffuser backside" mask	Exposed resist	Süss MA56	mask as required by design	Time - 2.5 s	Use "First Mask" setting as no alignment is required. Center the stage before loading the wafer. The backside pattern has a series of channels.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0140	Develop	Develop exposed resist	Clean diffuser backside mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish 100 mm wafer holder DI gun N ₂ gun	AZ devel- oper DI water N ₂	Temp - 20 °C Time - ~0.8 min + 0.2 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry.
0150	Mount	Mount wafer on carrier wafer	Device wafer securely mounted on a 100 mm carrier		150 °C heat release tape 100 mm Si wafer		Cut a 100 mm circle of heat release tape no larger than the carrier wafer. Laminate the carrier wafer then press the device wafer onto it.
0160	Etch	Silicon etch	Etch silicon to a depth of 50 μm in wall regions	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~25 min See Appendix C for detailed Si etch recipe conditions.	
0170	Strip	Clean resist from front of wafer	Clean surface of wafer	100 mm wafer holder N ₂ gun	acetone IPA N ₂		Rinse with acetone followed by IPA. Do not allow acetone to dry on the surface of the wafer.
0180	Coat	HMDS coat	Monolayer of adhesion promoter to improve resist adhesion and pattern integrity	Solitec photoresist spinner	220 μm thick double-sided polished 100 mm Si wafer HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Dispense enough HMDS to coat the die and the tiles. Allow the HMDS to puddle for ~ 5 s before commencing the spin. Do a second HMDS coat right after the first.
0190	Coat	Resist coat	~4 μm resist with uniform die surface coverage	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 2000 rpm	Dispense a 1" puddle.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0200	Bake	Pre-exposure resist cure	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
0210	Expose	Expose “diffuser frontside” mask	Exposed resist	Süss MA6	mask as required by design	Time - 120 s	The frontside pattern has an array of holes.
0220	Develop	Develop exposed resist	Clean diffuser backside mask pattern transferred to resist, no bridging of features and good edge definition	wet bench petri dish 100 mm wafer holder DI gun N ₂ gun	AZ developer DI water N ₂	Temp - 20 °C Time - ~1.0 min + 0.2 min overdevelop	Quench the develop process in a petri dish of DI water prior to DI gun rinse and N ₂ dry.
0230	Mount	Mount wafer on carrier wafer	Device wafer securely mounted on a 100 mm carrier		150 °C heat release tape 100 mm Si wafer		Cut a 100 mm circle of heat release tape no larger than the carrier wafer. Laminate the carrier wafer then press the device wafer onto it.
0240	Etch	Silicon etch	Etch silicon to a depth of 50 µm in wall regions	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - ~90 min See Appendix C for detailed Si etch recipe conditions.	
0250	Inspect	Inspect the etched pattern	Si etched through the wafer	Olympus MX80 microscope			The frontside holes must be etched through to the backside channels. Etch in 5 min increments using anisotropic conditions until holes are etched through.
0260	Demount	Demount wafer from carrier	Intact, demounted etched wafer	hotplate		Temp - 150 °C Time ~ 30 s	Watch the wafer during heating. It will pop up slightly when the heat release tape releases.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0270	Etch	Etch polymer from surface	All polymer removed from surface so resist can be wet stripped	IPC barrel etcher	O ₂	Time - 10 min Power - 200 W Pressure - 1 T	
0280	Strip	Clean resist from front of wafer	Clean surface of wafer	100 mm wafer holder N ₂ gun	acetone IPA N ₂		Rinse with acetone followed by IPA. Do not allow acetone to dry on the surface of the wafer.
0290	Inspect	Inspect the etched pattern	No organic residue remaining in holes	Olympus MX80 microscope			
0300	Mount	Mount wafer on dicing frame	Dicing tape laminated on backside of wafer with no bubbles	hotplate laminator dicing frame	dicing tape		
0310	Dice	Dice wafer into sections	Straight, clean dicing street dividing the wafer into individual diffusers	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	
0320	Demount	Demount individual diffusers	Intact, individual diffusers				Remove the sections from the dicing tape. Peel the dicing tape slowly from the back of the diffusers while holding them still. Pull at a low angle to avoid breakage.
0330	Store	Store diffusers for later use	Safe and secure diffusers ready for use	dry box		Temp - 20° C	

B.3 Flip-chip Adhesive

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Measure	Dispense epoxy part A	Known mass of epoxy part A in petri dish	petri dish electronic scales with 0.01 g precision	Epo-Tek 377 part A	Temp - 20° C	This mass represents a predetermined proportion of the final solution. Check the manufacturer's spec sheet.
0110	Measure	Dispense epoxy part B	Known mass of epoxy part B in petri dish	petri dish electronic scales with 0.01 g precision	Epo-Tek 377 part A	Temp - 20° C	This mass represents a predetermined proportion of the final solution. Check the manufacturer's spec sheet. Dispense part B directly into the same petri dish to which part A was dispensed. This mass represents 50% of the final solution.
0120	Mix	Mix epoxy parts A and B	Homogeneous mixture of epoxy part A and part B	glass stirring rod	Epo-Tek 377	Temp - 20° C	Visually inspect for homogeneity. The part A is clear and the part B is a light yellow color so judge uniformity by the color of the solution.
0130	Charge	Charge syringe with epoxy solution	Bubble free epoxy in 1 mL syringe	1 mL syringe 26 gauge hypodermic needle	Epo-Tek 377	Temp - 20° C	Remove bubbles from the solution before dispensing to dip tray.

B.4 Backside Lithography Tiles

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Mount	Mount Si wafer on dicing frame	100 mm Si sub-mounted on dicing frame using tape	hotplate laminator dicing frame	~280 μ m thick 100 mm Si wafer dicing tape	Temp - 50 °C	Silicon substrate thickness chosen to match CMOS die thickness within 5 μ m to ensure planarity of resist coat during backside patterning.
0110	Dice	Dice Si sub into tiles	Straight, clean dicing street between 5 mm x 10 mm tiles	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	Leave the dried, diced wafer on the dicing tape, but cut the tape to a size that it can be stored in clamshell until tiles are needed.
0120	Store	Store die for later use		clam shell			
0130	Demount	Remove tiles from the tape	No chipping or cracking of tiles during removal				Remove tiles from tape by hand. Stretch the tape from the backside of the singulated die by pressing into it so the fragile edges of the tiles spread apart during demounting. Edge and corner integrity is necessary for planar resist coat and survival during etch.
0140	Clean	Clean tiles before use	Clean singulated tiles with smooth, sharp edges and no Si residues	beaker ultrasonic bath	acetone IPA		Ultrasonic in acetone to remove adhesive and silicon debris.

B.5 Etch Ballast Tiles

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Mount	Mount Si wafer on dicing frame	100 mm Si sub-mounted on dicing frame using tape	hotplate laminator dicing frame	1 mm thick 100 mm Si wafer dicing tape	Temp - 50 °C	The great thickness difference between the ballast tiles and the die they surround is to accommodate ARDE which results in a much faster tile etch rate than observed on the die.
0110	Dice	Dice Si sub into tiles	Straight, clean dicing street between 5 mm x 10 mm tiles	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	Leave the dried, diced wafer on the dicing tape, but cut the tape to a size that it can be stored in clamshell until tiles are needed.
0120	Store	Store die for later use		clam shell			
0130	Demount	Remove tiles from the tape	No chipping or cracking of tiles during removal				Remove tiles from tape by hand. Stretch the tape from the back-side of the singulated die by pressing into it so the fragile edges of the tiles spread apart during demounting. Edge and corner integrity is necessary for planar resist coat and survival during etch.
0140	Clean	Clean tiles before use	Clean singulated tiles with smooth, sharp edges and no Si residues	beaker ultrasonic bath	acetone IPA		Ultrasonic in acetone to remove adhesive and silicon debris.

B.6 Backside Etch Carrier Wafer

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Coat	Coat wafer with resist	Uniform, bubble free coat of resist	Solitec photoresist spinner	100 mm Si wafer AZ4620	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	
0110	Bake	Remove solvent from resist	Solvent free resist film	hotplate		Temp - 90 °C Time - 30 min	Do not use the convection oven as the permanent adhesive side of the heat release tape will not adhere to the resulting surface for the duration of the backside etch process.
0120	Bake	Hardbake resist	Hardened, etch resistant resist film	Blue M Stabiltherm gravity oven		Temp - 120 °C Time - 60 min	A longer bake does not cause a problem. The carrier wafer should be left in the oven until immediately before the glass wafer with the CMOS die is to be mounted. Etch the CMOS immediately after mounting as the adhesion between the heat release tape and carrier wafer deteriorates over time.
0130	Cut	Cut heat release tape to size	3" diameter circle of heat release tape	scissors	150 °C heat release tape		Heat release side facing up.
0140	Laminate	Laminate heat release tape on wafer	Bubble free heat release tape	rod with rounded end			While holding one side of the heat release tape off the surface of the wafer, rub the other side onto the wafer using the rounded end of a pen or other implement.

B.7 Post Etch Carrier Waferr

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Coat	Coat wafer with resist	Uniform, bubble free coat of resist	Solitec photoresist spinner	100 mm Si wafer AZ4620	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 2000 rpm	Do two coats of resist, one immediately after the other.
0110	Bake	Remove solvent from resist	Solvent free resist film	hotplate		Temp - 90 °C Time - 30 min	Do not use the convection oven as the permanent adhesive side of the heat release tape will not adhere to the resulting surface for the duration of the backside etch process.
0120	Bake	Hardbake resist	Hardened, etch resistant resist film	Blue M Stabiltherm gravity oven		Temp - 120 °C Time - 60 min	A longer bake does not cause a problem. The carrier wafer should be left in the oven until immediately before the glass wafer with the CMOS die is to be mounted. Etch the CMOS immediately after mounting as the adhesion between the heat release tape and carrier wafer deteriorates over time.
0130	Cut	Cut heat release tape to size	>2" x 2" square of heat release tape	scissors	150 °C heat release tape		Heat release side facing up.
0140	Laminate	Laminate heat release tape on wafer	Bubble free heat release tape	rod with rounded end			While holding one side of the heat release tape off the surface of the wafer, rub the other side onto the wafer using the rounded end of a pen or other implement.

B.8 Release Etch Carrier Wafer

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
0100	Cut	Cut heat release tape to size	~0.5" by 0.5" square of heat release tape	scissors	120 °C heat release tape		Heat release side facing up.
0110	Laminate	Laminate heat release tape on wafer	Bubble free heat release tape	rod with rounded end	100 mm Si wafer		While holding one side of the heat release tape off the surface of the wafer, rub the other side onto the wafer using the rounded end of a pen or other implement.

B.9 Etch Heating Test Structures

B.9.1 Backside Oxide Removal

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1000	Clean	Clean the wafer prior to resist coat	Clean surface free of micromasking defects or defect that may lead to pinholes in the resist	Semitoool PSC-101	100 mm, 220 μm double-sided polished wafer with 1.5 μm thick oxide DI water	default SRD conditions	Do not use tweezers to hold 220 μm thick wafers during rinsing and drying operations due to the risk of breakage. Use a 100 mm wafer holder.
1010	Coat	Frontside resist coat	Pinhole free resist film on the frontside of the wafer and no resist defects on the backside of the wafer	Solitec photoresist spinner	AZ4210	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	The frontside of the wafer is the side the final etch release mask is patterned on. Remove backside resist defects with cotton swab soaked in acetone, ensuring no streaks left after wiping.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
1020	Bake	Softbake resist	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
1030	Bake	Hardbake resist	Harden resist to increase the resistance to the HF etch	Blue M Stabiltherm gravity oven		Temp - 120 °C Time - 30 min	
1040	Etch	HF backside oxide removal	Oxide removed from the backside of the wafer	wet bench teflon dish teflon tweezers	buffered HF	Temp - 20 °C Time - 16 min	Ensure the backside surface dewets, indicating the oxide is gone.
1050	Strip	Resist strip	Complete removal of all resist and other organic residues	wet bench petri dish teflon tweezers	acetone IPA		Use a wipe soaked in acetone to remove the bulk of the resist ensuring no streaks are left, then use the acetone.

B.9.2 Frontside Patterning

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2000	Bake	Dehydration bake	Drive out all H ₂ O from the oxide layer	Blue M Sta-biltherm gravity oven		Temp - 200 °C Time - 6 hr	
2010	Deposit	Frontside TiW/ Al deposition	600 nm of Al on 100 nm of TiW on oxide	Perkin-Elmer 8L	TiW Al	<u>TiW deposition</u> Pressure - 20 mT Power - 100 W DC Time - 15 min <u>Al deposition</u> Pressure - 5 mT Power - 150 W DC Time - 10 min Heat Ex. Temp - 14 °C	Neither of the process conditions are optimized for any particular film property. The conditions were taken from working processes of other researchers. Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
2020	Deposit	Backside Al deposition	100 nm of Al on Si	Perkin-Elmer 8L	Al	Pressure - 5 mT Power - 130 W DC Time - 1 min Heat Ex. Temp - 14 °C	Perform at least 2 minutes of pre-sputter on each target to condition them. Pumpdown below 5×10^{-7} Torr will take > 60 mins.
2030	Coat	Backside resist coat	~1 μm thick, pin-hole free resist film on the frontside of the wafer and no resist defects on the backside of the wafer	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Resist coat of the backside is done first to prevent the frontside imaging resist from contacting any hard surfaces. The rationale is that it is better to have shallow scratches in the frontside Al, than have a deep scratch in the imaging resist.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2040	Bake	Softbake resist	Minimally hardened resist to prevent scratches penetrating to the Al layer during frontside coat	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 5 min	
2050	Coat	Frontside HMDS coat	Uniform hydrophobic surface for optimal resist adhesion	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Allow the HMDS puddle to cover the entire wafer surface and sit for a couple of seconds prior to spinning. Do a second HMDS coat right after the first.
2060	Coat	Frontside resist coat	~1 μm thick, pinhole free resist film on the frontside of the wafer and no resist defects on the backside of the wafer	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	
2070	Bake	Softbake resist	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 °C Time - 30 min	
2080	Expose	Expose resist	Fully exposed resist	Karl Suss MA56	thermal_isolation_mask	Time - 1.8 s	The time results in overexposure of the resist but the feature bias is small enough to retain the smallest features so further optimization was not done.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
2090	Develop	Develop exposed resist	Fully developed resist with no residues in the open areas	wet bench petri dish teflon tweezers	AZ developer	Time - < 1 min	The pattern should develop within a few seconds and should clear in less than 30 s. Overdevelop for approximately 50% of the time it took to clear. One of the petri dishes should be used for water to quench the develop process. Flow water into the quench dish to fully rinse of the developer. Avoid the wafer edge impacting the wall of the petri dish.
2100	Inspect	Post-develop inspection	Fully developed resist with no residues in the open areas	Olympus MX80 microscope			
2110	Etch	Aluminum etch	Fully etched Al down to TiW layer, with no residues	acid wet bench petri dish teflon tweezers personal protective clothing	Al etchant	Temp - 20 °C Time - 12 min + 0.5 min overetch	Etch until all Al is removed from the open areas and add 30 s overetch. The Al will begin to clear at the edge of the wafer.
2120	Strip	Remove resist	Resist removed from front and back of wafer with no particle or streak residues	solvent bench petri dish teflon tweezers	acetone IPA		

B.9.3 Backside Patterning

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3000	Coat	Frontside resist coat	~1 μm thick, pin-hole free resist film on the frontside of the wafer and no resist defects on the backside of the wafer	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Resist coat of the backside is done first to prevent the frontside imaging resist from contacting any hard surfaces. The rationale is that it is better to have shallow scratches in the frontside Al, than have a deep scratch in the imaging resist.
3010	Bake	Softbake resist	Minimally hardened resist to prevent scratches penetrating to the Al layer during frontside coat.	Despatch Protocol-Plus convection oven		Temp - 90 $^{\circ}\text{C}$ Time - 5 min	
3020	Coat	Backside HMDS coat	Uniform hydrophobic surface for optimal resist adhesion	Solitec photoresist spinner	HMDS	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	Allow the HMDS puddle to cover the entire wafer surface and sit for a couple of seconds prior to spinning. Do a second HMDS coat right after the first.
3030	Coat	Backside resist coat	~1 μm thick, pin-hole free resist film on the frontside of the wafer and no resist defects on the backside of the wafer	Solitec photoresist spinner	AZ4110	Spread Time - 6 s Spread Rate - 600 rpm Spin Time - 30 s Spin Rate - 4000 rpm	
3040	Bake	Softbake resist	Removal of excess solvent and resist stabilization	Despatch Protocol-Plus convection oven		Temp - 90 $^{\circ}\text{C}$ Time - 30 min	

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3050	Expose	Expose resist	Fully exposed resist	Karl Suss MA6	ARDEM_b ackside_ma sk	Time - 50 s	The time results in overexposure of the resist but the feature bias is small enough to retain the smallest features so further optimization was not done.
3060	Develop	Develop exposed resist	Fully developed resist with no residues in the open areas	wet bench petri dish teflon tweezers	AZ developer	Time - < 1 min	The pattern should develop within a few seconds and should clear in less than 30 s. Overdevelop for approximately 50% of the time it took to clear. One of the petri dishes should be used for water to quench the develop process. Flow water into the quench dish to fully rinse of the developer. Avoid the wafer edge impacting the wall of the petri dish.
3070	Inspect	Post-develop inspection	Fully developed resist with no residues in the open areas	Olympus MX80 microscope			
3080	Etch	Aluminum etch	Fully etched Al down to TiW layer, with no residues	acid wet bench petri dish teflon tweezers personal protective clothing	Al etchant	Temp - 20 °C Time - ~ 12 min	Etch until all Al is removed from the open areas and add 30 s overetch. The Al will begin to clear at the edge of the wafer.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
3090	Inspect	Post-etch inspection	Fully etched Al with no residues in the open areas	Olympus microscope			
3100	Strip	Remove resist	Resist removed from front and back of wafer with no particle or streak residues	wet bench petri dish teflon tweezers	acetone IPA		

B.9.4 Singulation

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
4000	Mount	Mount wafer in dicing frame	Wafer mounted on dicing frame using dicing tape, with no bubbles between the dicing tape and the wafer	laminator Al dicing frame	dicing tape	Temp - 50 °C	The backside of the wafer is placed facing upwards on the dicing tape laminator. In that case, the frontside of the wafer is exposed to the dicing blade. The choice was made on the basis of metal delamination seen at the edge of the dicing streets on one wafer on the side contacting the dicing tape. It is more important to protect the frontside pattern.
4010	Dice	Dice the wafer into individual chips	38 chips	Kulicke and Soffa dicing saw		Chuck-up Height - 0.075 mm Dicing saw conditions. See Appendix C for detailed conditions.	Alignment and cut guides at the edges of the array of chips.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
4020	Demount	Remove die from the dicing tape	Single die	delrin tipped tweezers			
4030	Clean	Post dicing clean	Clean die with no dicing tape or Si residues	ultrasonic bath glass beaker petri dish	acetone IPA	Time - 6 min	Ultrasonic single chips in acetone to remove debris and tape residue.

B.9.5 Test Preparation

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
5000	Mount	Mount single die on carrier	Single die mounted on carrier wafer with backside of die facing up		150 °C heat release tape resist coated carrier		Laminate the permanent adhesive side of the heat release tape onto the carrier wafer in the center of the wafer. Drop the die onto the heat release side of the tape and press down the edges to achieve a good thermal contact and adhesive bond.
5010	Etch	Backside Si etch	80 μm to 20 μm thick Si plate under the test structure areas	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - as required for desired Si thickness polymer rem. - 1 min isotropic - 5 min See Appendix C for detailed Si etch recipe conditions.	

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
5020	Measure	Etch depth measurement	Known backside etch depth	Olympus BHMJL microscope			Use the graduations on the focus knob to identify the height difference between the wafer backside surface and the Si surface in the etch pit. Ensure all the sacrificial pattern walls have been etched away.
5030	Demount	Demount die from carrier	Single intact die	hot plate		Temp - 150 °C Time - < 1 min	Heat until the heat release tape transitions to a uniform white color. Check the adhesion of the die before trying to pick it up. If there is residual adhesion, use a scalpel blade to gently pry up one corner.
5040	Etch	Frontside TiW/ SiO ₂ etch	Exposed frontside Si surface	Plas-matherm 790	CHF ₃ CF ₄ O ₂	See Appendix C for detailed oxide etch recipe conditions.	
5050	Inspect	Post-etch inspection	Fully etched SiO ₂ with Si exposed in open areas	Olympus BHMJL microscope			If pattern is globally underetched, re-etch in 10 minute increments until all Si is exposed.
5060	Measure	Measure etch mask stack	Known Al and TiW thickness	Veeco profi-leometer			The thermal oxide thickness is 1.5 μm. The Al and TiW stack thickness is ~0.8 μm.

Op. No.	Op. Type	Operation Description	Process Goal	Equipment	Materials	Conditions	Comments
5070	Measure	Measure suspension beam width	Known suspension beam width	Olympus MX80 microscope			Capture image using MagnaFire-SP and process image using Image Pro-Plus.
5080	Etch	Frontside release etch	Released MEMS heating test structures	STS-ASE	SF ₆ O ₂ C ₄ F ₈	anisotropic - as required to break-through the Si plate polymer rem. - 1 min isotropic - as required See Appendix C for detailed Si etch recipe conditions.	Etch the silicon substrate to a depth of 30 μm to 100 μm and then laterally etch for 10um to release the suspended disc structures.

Appendix C - Process Recipes

C.1 Perkin-Elmer 8L Al Deposition Conditions

Parameter	Value	Units
Base Pressure	$< 5 \times 10^{-7}$	Torr
Ar Flow	~ 17	scm
DC Power	150	W
Pressure	5	mTorr
Coolant Temperature	9	°C
Electrode Separation	56	mm
Time	As Required	min

C.2 STS DRIE Silicon Etch Conditions

Step Name	Standard Anisotropic		Polymer Removal	Standard Isotropic	
Step Type	Passivate	Etch	Etch	Etch	
Parameter	Value	Value	Value	Value	Units
ASE Switching	Selected		Not Sel'd	Not Sel'd	
Cycles	as required		N/A	N/A	
Process Time	as required		00:02:00	00:06:00	h:m:s
Cycle	1st	2nd	N/A	N/A	
Cycle Time	8	12	N/A	N/A	s
APC Mode	Manual		Auto	Auto	
APC Setting	58	58	N/A	N/A	%
Pressure	N/A	N/A	50	50	mTorr
C ₄ F ₈	85	0	0	0	sccm
SF ₆	0	130		130	sccm
O ₂	0	13	80	0	sccm
RF Coil	600	600	600	600	W
RF Platen	0	12	12	12	W
Matching	Auto	Auto	Auto	Auto	
DC Bias, V _b	N/A	120	135	150	V
RF Frequency	13.56				MHz
Platen Temperature	20				°C
Lid Temperature	45				°C
He Cooling	6				Torr

C.3 Plasmatherm Oxide Etch Conditions

Step Name	Pre-O ₂ Clean	Oxide Etch	Post-O ₂ clean	
Parameter	Value	Value	Value	Units
Pump	Turbo	Turbo	Turbo	
Terminate by	Var Time	Var Time	Var Time	
Default Time	20	300	10	min.
Pressure	50	100	200	mT
CHF3	0	22.5	0	sccm
O ₂	50	16	80	sccm
Power	100	100	100	W

C.4 Kulicke and Soffa Dicing Saw Conditions

Step Name	General	
Parameter	Value	Units
Units	mm	
Cutting Type	Dice	
Ref Point	Yes	
Alignment	Manual	
Process Flow	Dual	
Substrate Shape	Circ	
X,Y Offsets	0	
Quality Diameter	95	%
Thickness	0.65	mm
Auto Height Rate	25	cuts
Spindle Speed	25	krpm

Step Name	Block 1	Block 2	
Parameter	Value	Value	Units
Chuck-up Height	as required	as required	mm
Angle	0	90	deg
Cut Length	120	120	mm
Index	var	var	mm
Cut Count	var	var	
Overcut	10	10	mm
Z Speed	6	6	mms ⁻¹
X Entry Speed	6	6	mms ⁻¹
X Cutting Speed	6	6	mms ⁻¹

C.5 West Bond 4500E Wirebonder Conditions

Bond Recipe	Bond 1	Bond 2	
Parameter	Value	Value	Units
U/S Power	250	200	
U/S Time	350	250	ms
Force	HIGH	HIGH	
Depth	2	3	z steps
Inhibit Auto	ON	ON	
Speed	5	5	
Delay	25	25	ms

High force = 32 g

Critical bond = 1

Machine Setup		
Parameter	Value	Units
Clamp Home	130	steps
Wire Pull	34	steps
Wire Tail	19	steps
Dual Force	ON	
Restart Height Elevation	1400	steps
Lift Before Pull	OFF	
U/S Power During Feed	0	
U/S Power During Feed	0	
U/S Diagnostic Test	ON	

Appendix D - Scripts and Code

D.1 Surface F Concentration Simulation for Microloading Analysis

Comsol Multiphysics® (3.5a with Matlab®) is used to simulate the variation in F concentration in a region of space above a resist coated Si wafer with an exposed circle of Si of varying diameter at its center. The concentration is extracted along the surface of the wafer from the center to the edge. The model m-file was built in Matlab® R2008a.

```
fileclear fem

% COMSOL version
clear vrsn
vrsn.name = 'COMSOL 3.5';
vrsn.ext = 'a';
vrsn.major = 0;
vrsn.build = 603;
vrsn.rcs = '$Name: $';
vrsn.date = '$Date: 2008/12/03 17:02:19 $';
fem.version = vrsn;

% Constants
fem.const = {'De','80.2', ...
             'EA','5.6e-21', ...
             'D','0.5', ...
             'cF','5.5e-5', ...
             'kB','1.38e-23', ...
             'Te','300'};

% Descriptions
clear descr
descr.const= {'D','diffusion coefficient','EA','activation energy','De',...
             'etching flux constant','Te','etching temperature','kB',...
             'Boltzmann constant','cF','bulk concentration'};
fem.descr = descr;
```

```
% Parameters defining structure
R = 60e-3; % radius of the Si wafer plus an extended region
ts = 50e-3; % thickness of the stagnation zone above the wafer surface
% radius of central circle of exposed Si
r = [1e-6, 50e-6, 0.1e-3, 1e-3, 5e-3, 10e-3, 20e-3];

[mr,nr] = size(r);
rho = [0,linspace(1e-6,9e-6,18),linspace(1e-5,9e-5,18),linspace(1e-4,9e-4,18)...
    linspace(1e-3,9e-3,36),linspace(1e-2,6e-2,48)];
[mrho,nrho]=size(rho);
z = zeros(1,nrho);
p = [rho;z];

cout = zeros(nrho,nr);

for ir = 1:nr

    % Geometry
    g1=rect2(R,ts,'base','corner','pos',{'0','0'},'rot','0');
    g2=curve2([0,r(ir)],[0,0]);

    % Analyzed geometry
    clear c s
    c.objs={g2};
    c.name={'B1'};
    c.tags={'g2'};

    s.objs={g1};
    s.name={'R1'};
    s.tags={'g1'};

    fem.draw=struct('c',c,'s',s);
    fem.geom=geomcsg(fem);

    % Initialize mesh
    fem.mesh=meshinit(fem,'hauto',2);

    % Application mode 1
    clear appl
    appl.mode.class = 'FICnvDiff';
    appl.mode.type = 'axi';
    appl.dim = {'c2'};
    appl.name = 'cd2';
    appl.assignsuffix = '_cd2';
    clear prop
    prop.analysis='static';
    clear weakconstr
    weakconstr.value = 'off';
    weakconstr.dim = {'lm2'};
    prop.weakconstr = weakconstr;
    appl.prop = prop;
    clear bnd
```

```
bnd.c0 = {0,0,0,'cF'};  
bnd.name = {'no_etching','axi_sym','etching','source'};  
bnd.N = {0,0,'-De*c2*Te^0.5*exp(-EA/kB/Te)',0};  
bnd.type = {'N0','ax','N','C'};  
bnd.ind = [2,3,4,1,1];  
appl.bnd = bnd;  
clear equ  
equ.D = 'D';  
equ.ind = [1];  
appl.equ = equ;  
fem.appl{1} = appl;  
fem.sdim = {'r','z'};  
fem.frame = {'ref'};  
fem.border = 1;  
fem.outform = 'general';  
clear units;  
units.basesystem = 'SI';  
fem.units = units;  
  
% ODE Settings  
clear ode  
clear units;  
units.basesystem = 'SI';  
ode.units = units;  
fem.ode=ode;  
  
% Multiphysics  
fem=multiphysics(fem);  
  
% Extend mesh  
fem.xmesh=meshextend(fem);  
  
% Solve problem  
fem.sol=femstatic(fem, ...  
    'solcomp',{c2}, ...  
    'outcomp',{c2}, ...  
    'blocksize','auto');  
  
cstep = postinterp(fem,'c2',p);  
cout(:,ir) = cstep';  
end  
  
% Save current fem structure for restart purposes  
fem0=fem;
```

D.2 Etch Heating ROI Temperature Extraction

The following code, written in PERL (v5.6.1), is used to extract and compile thermometric data from text files produced by the ExaminIR Max software provided by FLIR. The software enables the user to define multiple ROI's in the IR camera field of view for which predefined statistical routines (average, maximum, minimum, median, etc.) are executed on the pixel level thermometric data for multiple preset temperature ranges. The code is written for a specific file name convention that comprises a numeric chip identifier, process recipe and the geometry of the test structure being monitored (ex. 1_2_hotiso2_5_25_0.txt refers to chip 1, version 2, isotropic process version 2, suspension width 5 μm , suspension length 25 μm and temperature preset range 0, which is 20 C to 90 C).

```
#!/usr/bin/perl

# Modules
use strict;

# scalar
my ($i, $j, $jrec, $jw, $jl, $jr, $jp, $jref, $o, $chip_ct, $frame, $line, $rev, $outref, $s, $file, $w, $l,
    $result, $Tavg, $Tavgsum, $Trefavgsum, $Trefavg, $Tref);

# arrays
my (@e, @recipe, @width, @length, @radius, @preset, @ref, @data, @output, @fdump, @procout);

# initialize variables
print "Enter chip count\n"; # the user is requested to enter the number of test die
$chip_ct = <STDIN>;
chomp($chip_ct);

print "Enter chip revision\n"; # the user is requested to enter the revision of the test die
$rev = <STDIN>;
chomp($rev);

@recipe = ("hotiso1", "hotiso2", "hotiso3", "aniso", "stdaniso", "polymer_removal"); # process list
@width = (5, 10, 20); # test structure suspension width list
@length = (25, 250, 500); # test structure suspension length list
@radius = (50, 250, 500, 750); # test structure suspended disc radius list
@preset = (0, 1, 2); # IR camera temperature presets list

# Create a chip-level file chip_num+rev+recipe that contains all the extracted ROI data for each frame,
# for every test structure, preset and structure or reference ROI. The reason for the complexity of the
# code that performs a very simple task is that the camera acquisition board drops frames randomly
# and is not consistent across the presets. So each file must be opened and its data aligned with the
# the first file opened, which is taken as the frame baseline.
```

```

for ($j = 1; $j <= $chip_ct; $j++) {
  OUTPUT: foreach $jrec (@recipe) {
    @output = [];
    @procout = [];
    $file=1;
    $w=0;
    $l=0;
    @e=[];
    $Tavg=undef;
    $Trefavg=undef;

    foreach $jw (@width) {
      foreach $jl (@length) {
        foreach $jp (@preset) {
          if (-e ".$j-$rev\_ $jrec/$j-$rev\_ $jrec\_ $jw\_ $jl\_ $jp.txt") {
            open (INPUT, ".$j-$rev\_ $jrec/$j-$rev\_ $jrec\_ $jw\_ $jl\_ $jp.txt");
            $frame=0;
            $s=0;
            @fdump=[];

            LINE: while (<INPUT>) {
              chomp;
              @data = split /\t/;
              if ($file==1) {
                $output[$frame][0] = "$data[0]t";
                unless ($frame < 2) {
                  if ($data[0] == $output[$frame-1][0]) {
                    $output[$frame][0] = undef;
                    next LINE;
                  }
                }
              } else {
                $fdump[$frame][0] = $data[0];
                unless ($frame < 2) {
                  if ($data[0] == $fdump[$frame-1][0]) {
                    next LINE;
                  }
                }
              }
            }

            STRUCTURE: for ($s = 0; $s <= 3; $s++) {
              $i=2*(1+$s);
              # $o=1+6*$s+2*$jp+24*$l+72*$w;
              $o=1+6*$s+2*$jp+24*$l;
              $output[$frame][$o] = $data[$i];
              $output[$frame][$o+1] = $data[$i+1];
            }
            $frame++;
          }
        }
      }
    }
    close (INPUT);
    $file++;
  }
}

```

```

        } else {
            unlink "./$j-$rev\_$_jrec.rd";
            next OUTPUT;
        }
    }
    $l++;
}
$w++;
}
splice (@output, -10);
$frame=0;

```

The final output file is compiled. The absolute temperature of the suspended disc and the # temperature of the suspended disc with respect to the anchor is needed.

```

while (defined($output[$frame])) {
    $procout[$frame][0] = $output[$frame][0];
    if ($frame == 0) {
        for ($s = 0; $s <= 35; $s++) {
            $i=1+6*$s;
            $o=1+2*$s;
            $procout[$frame][$o] = "T, $output[$frame][$i]\t";
            $procout[$frame][$o+1] = "deltaT, $output[$frame][$i]\t";
        }
        $procout[$frame][73]= "Trefavg\t";
    }
    } elsif ($frame == 1) {
        $Tavgsum=0;
        $Trefavgsum=0;
        for ($s = 0; $s <= 35; $s++) {
            $Tavgsum=$Tavgsum+$output[$frame][1+6*$s];
            $Trefavgsum=$Trefavgsum+$output[$frame][2+6*$s];
        }
        $Tavg=$Tavgsum/36;
        print "Tavg\= $Tavg\n";
        $Trefavg=$Trefavgsum/36;
        $procout[$frame][73]="$Trefavg\t";
        for ($s = 0; $s <= 35; $s++) {
            $i=1+6*$s;
            $o=1+2*$s;
            $e[$s]=$output[$frame][$i]-$Tavg;
            $result = $output[$frame][$i]-$e[$s];
            $procout[$frame][$o] = "$result\t";
            $result = $result-$Trefavg;
            $procout[$frame][$o+1] = "$result\t";
        }
    }
    } else {
        $Trefavgsum=0;
        for ($s = 0; $s <= 35; $s++) {
            $Trefavgsum=$Trefavgsum+$output[$frame][2+6*$s];
        }
    }
}

```

```

$Trefavg=$Trefavgsum/36;
$procout[$frame][73]= "$Trefavg\t";

for ($s = 0; $s <= 35; $s++) {
    $i=1+6*$s;
    $o=1+2*$s;
    if ($output[$frame][$i] < 85) {
        $result = $output[$frame][$i]-$e[$s];
        $procout[$frame][$o] = "$result\t";
        $result = $result-$Trefavg;
        $procout[$frame][$o+1] = "$result\t";

    } elseif ($output[$frame][$i] < 150) {
        $result = $output[$frame][$i+2]-$e[$s];
        $procout[$frame][$o] = "$result\t";
        $result = $result-$Trefavg;
        $procout[$frame][$o+1] = "$result\t";

    } else {
        $result = $output[$frame][$i+4]-$e[$s];
        $procout[$frame][$o] = "$result\t";
        $result = $result-$Trefavg;
        $procout[$frame][$o+1] = "$result\t";
    }
}
}
$frame++;
}
open (RAW_DATA, ">./$j-$rev\_jrec.rd") || die "Unable to open $j-$rev\_jrec.rd";
foreach $outref (@procout) {
    print RAW_DATA ("@$outref\n");
}
close (RAW_DATA);
}
}

```

D.3 F Concentration Simulation for Suspended Disc

Comsol Multiphysics[®] (3.5a with Matlab[®]) is used to simulate the F concentration around the suspended disc for the etch heating study. The model m-file was built in Matlab[®] R2008a and iterates over the suspended disc geometry and across the temperature range observed in the experiment. The output of the simulation is the concentration along the sidewall and underside of the suspended disc structure. The extracted F concentration at the bottom of the sidewall, called the “corner concentra-

tion” is used as the input to the Mathematica® 6 notebook in Appendix D.3 for the generation of an analytic fitting function.

```

fclear fem

% COMSOL version
clear vrsn
vrsn.name = 'COMSOL 3.5';
vrsn.ext = 'a';
vrsn.major = 0;
vrsn.build = 603;
vrsn.rcs = '$Name: $';
vrsn.date = '$Date: 2008/12/03 17:02:19 $';
fem.version = vrsn;

% Constants
fem.const = {'EA','1.1e-20', ...
    'kB','1.38e-23', ...
    'CF','1.1e-4', ...
    'De','160.4', ...
    'D','0.3'};

% Parameters defining structure
tw = 220e-6;
t = [25e-6, 40e-6, 80e-6, 120e-6, 160e-6];
r = [25e-6, 75e-6, 100e-6, 250e-6, 500e-6, 750e-6];
l = [25e-6, 50e-6, 75e-6, 100e-6, 175e-6, 250e-6, 500e-6];
Temp = [300:25:450];
Plot_Temp = Temp;
Corner_conc = [];
data_row = [];

% Descriptions
clear descr
descr.const= {'D','Diffusion coefficient','EA','Activation energy','CF','F concentration','De','Etching flux
factor','kB','Boltzmann constant'};
fem.descr = descr;

for ir = 1:6
    for il = 1:7
        for it = 1:5
            data_row = [r(ir), l(il), t(it)];
            % Geometry
            g1=rect2(r(ir)+l(il),tw,'base','corner','pos',{0,'0'},'rot','0');
            g2=rect2(r(ir),t(it),'base','corner','pos',{0,tw-t(it)},'rot','0');
            g3=geomcomp({g1,g2},'ns',{'R1','R2'],'sf','R1-R2','edge','none');

            % Analyzed geometry
            clear s
            s.objs={g3};
            s.name={'CO1'};

```

```

s.tags={'g3'};

fem.draw=struct('s',s);
fem.geom=geomcsg(fem);

% Initialize mesh
fem.mesh=meshinit(fem,'haut0',5);

% Application mode 1
clear appl
appl.mode.class = 'FICnvDiff';
appl.mode.type = 'axi';
appl.dim = {'c2'};
appl.sdim = {'x','z','y'};
appl.name = 'cd2';
appl.sshape = 2;
appl.assignsuffix = '_cd2';
clear prop
prop.analysis='static';
clear weakconstr
weakconstr.value = 'off';
weakconstr.dim = {'lm2'};
prop.weakconstr = weakconstr;
appl.prop = prop;
clear bnd
bnd.c0 = {0,0,0,'CF'};
bnd.name = {'insulation','axi_sym','etching','source'};
bnd.N = {0,0,-De*c2*Te^0.5*exp(-EA/kB/Te),0};
bnd.type = {'N0','ax','N','C'};
bnd.ind = [2,1,3,3,4,3];
appl.bnd = bnd;
clear equ
equ.D = 'D';
equ.ind = [1];
appl.equ = equ;
fem.appl{1} = appl;
fem.frame = {'ref'};
fem.border = 1;
fem.outform = 'general';
clear units;
units.basesystem = 'SI';
fem.units = units;

% ODE Settings
clear ode
clear units;
units.basesystem = 'SI';
ode.units = units;
fem.ode=ode;

% Multiphysics
fem=multiphysics(fem);

```

```
% Extend mesh
fem.xmesh=meshextend(fem);

% Solve problem
fem.sol=femstatic(fem, ...
    'solcomp',{'c2'}, ...
    'outcomp',{'c2'}, ...
    'blocksize','auto', ...
    'pname','Te', ...
    'plist',Temp, ...
    'oldcomp',{});

% Save current fem structure for restart purposes
fem0=fem;

% Integrate
for iT = 1:7
    data_row(4) = Temp(iT);
    data_row(5) = postint(fem,'c2', ...
        'unit','mol/m^3', ...
        'recover','off', ...
        'dl',3, ...
        'edim',0, ...
        'solnum',iT);
    Corner_conc = [Corner_conc; data_row];
end
end
end
end
```

D.4 Suspended Disc Corner F Concentration Fitting

The m-file in Appendix D.2 is used to simulate the Fconcentration at the bottom of the sidewall of the disc so an analytic function can be fit to the data. The Mathematica[®]6 FindFit function is used as the LSR fitting tool. The fitted model's goodness-of-fit is determined by the R^2 correlation coefficient and its validity is assessed using a quantile-quantile plot. Text lines, executable lines and output lines in Mathematica[®]6 are identified through formatting that is not used here. Text lines are delineated by the "*" symbol, input line blocks by a line of "~" symbols and output lines by the "#" symbol. To reconstitute the code in Mathematica[®]6, paste the each line and block of lines individually and change "Format" to the appropriate "Style".

* Program for extracting the fitting parameters for the function relating corner F concentration in a
* suspended disc test structure to the geometric parameters and temperature.

* Data Import

```
~~~~~  
SetDirectory["C:\\Documents and Settings\\gilgunn\\Desktop\\PhD\\Publications\\JMM\\Etch Heating  
  Paper\\Diffusion Model\\"];  
data = Import["corner_conc_raw_data_for_fit.txt", "Table"];  
Needs["StatisticalPlots"];  
~~~~~
```

* Model Fitting

* The suspended disc structure has a thickness t and radius r. It is suspended by four fixed-fixed
* beams of length l, which define an annulus of the same width. As the structure heats to a
* temperature T, the etch rate increases and the rate of F consumption increases, hence the
* concentration of F decreases. The F must diffuse through the gap, along the exposed Silicon to
* reach the underside of the disc. The F concentration at this corner is needed to compute the F
* concentration under the disc.

* This model contains four terms: 1. a linear term in thickness t, 2. a linear term in temperature T, 3. a
* Dushman conductance term relating to the aspect ratio of the structure and 4. a microloading term
* relating to the ratio of the exposed Si area to the total plan area of the structure.

* Extracting the fitting parameters for the model

```
~~~~~  
CFb = 1.1 x 10^-4; (*bulk F concentration*)  
model = CFb*(1 - a1*t*T)/(1 + a2*t/l)/(1 + a3*(r/(l + r))^2);  
fit = FindFit[data, model, {{a1, 10}, {a2, 10}, {a3, 10}}, {r, l, t, T}];  
~~~~~
```

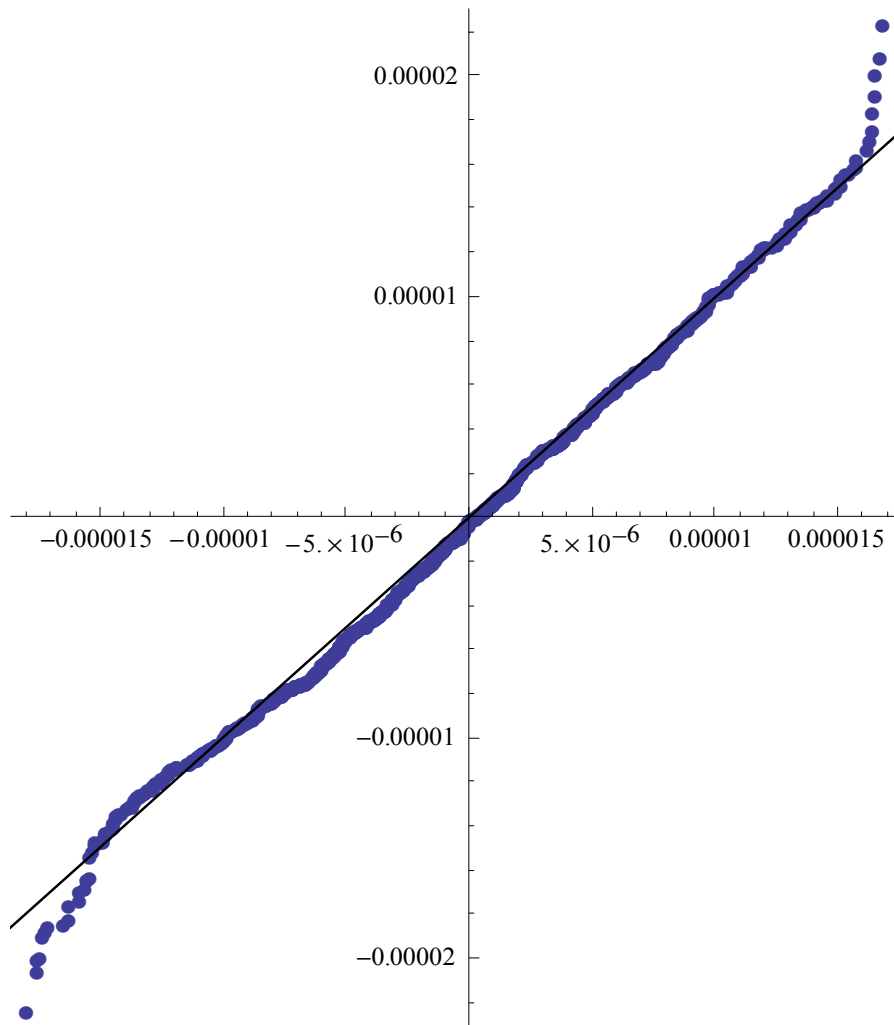
* The output of the FindFit function is not an exact value, but an approximation so the numeric portion
* of the result must be separated from the symbols that identify it as an approximation.

```
a1m = a1 /. {fit[[1]]};  
a2m = a2 /. {fit[[2]]};  
a3m = a3 /. {fit[[3]]};
```

~~~~~  
\* A predicted value of F corner concentration is generated for each set of independent variables and  
\* compared to the simulated data from which it is derived. The residuals of the model are calculated  
\* and analyzed using a quantile-quantile plot and correlation coefficient R<sup>2</sup> to determine the validity of  
\* the model.  
~~~~~

```
f[r_, l_, t_, T_] := CFb*(1 - a1m*t*T)/(1 + a2m* t/l)/(1 + a3m*(r/(l + r))^2);  
radius = data[[All, 1]];  
length = data[[All, 2]];  
thickness = data[[All, 3]];  
temp = data[[All, 4]];  
ybar = Mean[data[[All, 5]]];
```

```
~~~~~  
fitteddata = f[radius, length, thickness, temp];  
residual = data[[All, 5]] - fitteddata;  
{n} = Dimensions[residual];  
resbar = Mean[residual];  
resstd = StandardDeviation[residual];  
norm = RandomReal[NormalDistribution[0, resstd], n];  
QuantilePlot[residual, norm]
```



```
~~~~~  
sse = 0; (*sum of squared error*)  
sst = 0; (*sum of squared total error*)  
For [i = 1, i < n + 1, i++,  
    sse = sse + residual[[i]]^2;  
    sst = sst + (data[[i, 5]] - ybar)^2  
]  
Rsquared = 1 - sse/sst (*R2 correlation coefficient*)  
~~~~~  
# 0.89539
```

D.5 Eigenvalues of F Concentration Solution Under Suspended Disc

The relative magnitudes of the eigenvalues of the F concentration under the suspended disc were evaluated to assess the contribution of each in the final solution and determine if a dominant eigenvalue existed that would enable a simplified approximation to the exact solution.

Manual changes are required from the user to make this script work correctly. The list “btry” contains a list of approximate eigenvalues used to initiate the FindRoot function. The user must change the numeric index of btry where shown to select the approximate location to search for the eigenvalue. The output file “beta_output.txt” that is generated by the script must be manipulated from an 18 x 1 table to a 6 x 3 table with all non-numeric characters stripped out and then saved to a file called “beta_input.txt”.

```

clear all;
*needed as user may evaluate this notebook multiple times per session

* Define the parameters and equations
~~~~~
ρ=2330; (*Silicon density in kgm-3*)
μSi=28 x 10-3; (*Silicon molar mass in kgmol-1*)
A=30.11 x 10-6; (*Arrhenius pre-exponential factor in m4K-1/2mol-1s-1*)
EA=7 x 10-21; (*Activation energy in Jparticle-1*)
DF=1.5; (*diffusivity of F in a mixture of F and SiF4 in m2s-1*)
kB=1.38 x 10-23; (*Boltzmann constant in JK-1*)
tw=220 x 10-6; (*Si wafer thickness in m*)
tSi={25 x 10-6, 40 x 10-6, 80 x 10-6}; (*Si thickness under suspended disc*)
T={300,325,350,375,400,425}; (*Temperature values in K*)
btry= {425,1000,2000,4000,8000,12000,20000,40000,60000,80000,100000,120000}; (*Approximate
      root locations for the transcendental equation*)
~~~~~

* Functions for the generalized transport parameter h and the
* transcendental equation for Subscript[β, m].
~~~~~
H[T_]:=4*(ρ A)/(μSi *DF)*T0.5*Exp[-EA/(kB*T)];
h=H[T];
f[βm_]:=βm *Tan[βm *(tw-tSi[[j]])]-h[[i]];
K[β_]:= (Sin[2*β*(tw-tSi[[j]])]/(β2+h[[i]]2))/(β*((tw-tSi[[j]])/(β2+h[[i]]2))+h[[i]]);
~~~~~

* Loop over h and tSi to get a matrix of roots of f[β_] that are
* printed to a file and read back in to calculate a matrix of values for K.
~~~~~
SetDirectory["C:\\Documents and Settings\\gilgunn\\Desktop\\PhD\\

```

```

Publications\JMM\Etch Heating Paper\"];
roots = {};
{mh} = Dimensions[h];
{nt} = Dimensions[tSi];
For[j = 1, j < nt + 1, j++,
  For[i = 1, i < mh + 1, i++,
    AppendTo[roots, FindRoot[f[β], {β, btry[[1]]}];
    (* the user must change the numeric index of btry to select the approximate location to search for
    an eigenvalue*)
  ]
]
roots
Export["beta_output.txt", roots, "Table"];

```

```

# roots = {{β -> 330.555}, {β -> 359.85}, {β -> 387.542},
  {β -> 413.744}, {β -> 438.569}, {β -> 462.126},
  {β -> 344.071}, {β -> 374.567}, {β -> 403.396},
  {β -> 430.674}, {β -> 456.52}, {β -> 481.046},
  {β -> 390.195}, {β -> 424.791}, {β -> 457.497},
  {β -> 488.448}, {β -> 517.775}, {β -> 545.606}}

```

```

betain = Import["beta_input.txt", "Table"]
(* the output of this command line is displayed to allow the user to verify the dimensions of the input file
were correct*)
{mi, ni} = Dimensions[betain];
Kays = {};
For[j = 1, j < ni + 1, j++,
  For[i = 1, i < mi + 1, i++,
    AppendTo[Kays, K[betain[[i,j]]]]
  ]
]
Export["K_output.txt", Kays, "Table"];
Kays

```

```

# betain = {{330.555, 344.071, 390.195}, {359.85, 374.567, 424.791},
  {387.542, 403.396, 457.497}, {413.744, 430.674, 488.448},
  {438.569, 456.52, 517.775}, {462.126, 481.046, 545.606}}

```

```

# kays = {0.998614, 0.998358, 0.998095, 0.997828, 0.99756, 0.99729,
  0.998721, 0.998484, 0.998241, 0.997995, 0.997747, 0.997498,
  0.999005, 0.998821, 0.998632, 0.99844, 0.998247, 0.998054}

```

D.6 Suspended Disc Temperature Modeling

The Mathematica[®]6 FindRoot function is used to predict the suspended disc temperature for each combination of geometric parameters and process condition for a range of values of α . The R^2 correlation coefficient is calculated for each value of α using the entire experimental dataset and the value of α that produces the best fit based on R^2 is determined. A quantile-quantile plot is generated to assess the validity of the model using the optimal value of α .

The etch model incorporates an eigenfunction solution for the F concentration under the suspended disc. The eigenvalues are dependent on the generalized mass transport parameter he representing the F consumption that occurs during etching, which is dependent on the temperature. FindFit is used iteratively to predict the suspended disc temperature in this case. A convergence tolerance is used to control the accuracy of the model prediction.

Text lines, executable lines and output lines in Mathematica[®]6 are identified through formatting that is not used here. Text lines are delineated by the “*” symbol, input line blocks by a line of “~” symbols and output lines by the “#” symbol. Text strings embedded in input lines are bounded by “(*text*)”. To reconstitute the code in Mathematica[®]6, paste each line and block of lines individually and change “Format” to the appropriate “Style”.

* Data Input

```

~~~~~
SetDirectory["C:\Documents and Settings\gilgunn\Desktop\PhD\
Publications\JMM\Etch Heating Paper\"];
data = Import["raw_temp_data_for_analysis.txt","Table"];
{md,nd}=Dimensions[data];
w=1 x 10-6*data[[All,2]]; (*suspension width in m*)
l=1 x 10-6*data[[All,3]]; (*suspension length in m*)
r=1 x 10-6*data[[All,4]]; (*suspended disc radius in m*)
t=1 x 10-6*data[[All,5]]; (*suspended disc thickness in m*)
tg=220 x 10-6-t; (*thickness of the gap under the suspended disc in m*)
Vb = data[[All,6]]; (*etch bias voltage in V*)
Ta=273+data[[All,7]]; (*anchor temperature in K*)
Tm=273+data[[All,8]]; (*measured temperature of the suspended disc in K*)
(*Tmi = 300;*)
Tmbar=Mean[Tm];
Tmstdev=StandardDeviation[Tm];
zeros=ConstantArray[0,md];

```

Needs["StatisticalPlots`"]

~~~~~  
\* Constants and Variables

\* Physical Constants

~~~~~  
e = 1.602 x 10⁻¹⁹; (*electronic charge in C*)
σ = 5.67 x 10⁻⁸; (*Stefan-Boltzmann constant in Wm⁻²K⁻⁴*)
kB=1.38 x 10⁻²³; (*Boltzmann constant in WK⁻¹*)
ρSi = 2330; (*silicon density in kgm⁻³*)
μSi= 2.809 x 10⁻²; (*silicon molar mass in kgmol⁻¹*)
~~~~~

\* Structure Parameters

~~~~~  
Nb = 4; (*number of suspension beams*)
tb = 2.36 x 10⁻⁶; (*suspension thickness in m*)
κ = 78; (*effective beam thermal conductivity in Wm⁻¹K⁻¹*)
~~~~~

\* Plasma Parameters

~~~~~  
EA = 11 x 10⁻²¹; (*activation energy for Si-F reaction in J*)
AA = 480 x 10⁻⁶; (*Arrhenius's pre-exponential factor in m⁴K^{-0.5}s⁻¹*)
cFb=110 x 10⁻⁶; (*bulk neutral F density in molm⁻³*)
ΔH=1.45 x 10⁶; (*product weighted SiF_x reaction heat in Jmol⁻¹, where x = 3,4*)
Γi=35 x 10⁻⁶; (*ion flux in molm⁻²s⁻¹*)
Te = 1.6; (*electron temperature in eV*)
DF = 0.3; (*F diffusion coefficient in SF₆ in m²s⁻¹*)
K1=π*AA*ρSi/μSi*ΔH;
~~~~~

\* Thermal and Infrared Parameters

~~~~~  
ε = 0.95; (*emissivity*)
T0 = 308; (*surrounding temperature in K*)
~~~~~

\* Modelling Parameters

~~~~~  
Ttol = 0.5; (*convergence tolerance for temperature calculation*)
~~~~~

\* Fitting parameters for a model of the F concentration along the sidewall  
\* of the suspended disc structure. These parameters were obtained using the  
\* notebook "corner\_conc\_fitting.nb".

~~~~~  
a1 = 1.8971058278006814;
a2 = 0.24504917894159833;
a3 = 0.19391469936483213;
~~~~~

\* Solving the Power Balance Equation to Extract  $\alpha$

\* The generalized transport parameter from the diffusion equation solution  
 \* for the F concentration under the suspended disc, based on the measured  
 \* data.

$$hm = 4 * \rho_{Si} / \mu_{Si} * (AA * T_m^{0.5} * \exp[-(EA / (k_B * T_m))]) / DF;$$

\* The transcendental equation that defines the eigenvalues of the diffusion  
 \* equation solution for the F concentration under the suspended disc. The  
 \* initial approximation to the eigenvalues (i.e. roots of  $fm[\beta_m]$ ) is  
 \* made on the basis of the measured data.

$$fm[\beta_m] := \beta_m * \tan[\beta_m * (tg[[ib]])] - hm[[ib]]; \\ f\alpha[\beta_] := \beta * \tan[\beta * (tg[[ib]])] - h\alpha[[ib]]; \\ ~~~~~~$$

\* Parameter  $K0 = g[\beta_, h_]$  arises from the norm of the solution of the  
 \* diffusion equation for the F concentration under the suspended disc.

$$g[\beta_, h_] := (\sin[2 * \beta * (tg[[ib]])] * (\beta^2 + h^2)) / (\beta * \\ ((tg[[ib]]) * (\beta^2 + h^2) + h)); \\ ~~~~~~$$

\* The expanded power balance equation.

$$P[T_] := \pi * e * r[[ib]]^2 * \Gamma * Vb[[ib]] + (\alpha[[ib]] * K1 * \\ cFb * T^{0.5} * \exp[-(EA / (k_B * T))]) * r[[ib]] / ((1 + a2 * t[[ib]] / l[[ib]]) * \\ (1 + a3 * (r[[ib]] / (r[[ib]] + l[[ib]]))^2)) * (K0\alpha[[ib]] * \\ (1 - a1 * t[[ib]] * T) * r[[ib]] * (1 - (\beta\alpha[[ib]] * r[[ib]])^2 / 8 + \\ (\beta\alpha[[ib]] * r[[ib]])^4 / 48 - (\beta\alpha[[ib]] * r[[ib]])^6 / \\ 288) + 2 * t[[ib]] * (1 - a1 * (t[[ib]] * T) / 2)) - 2 * \pi * \epsilon * \sigma * \\ r[[ib]] * (r[[ib]] + t[[ib]]) * (T^4 - T0^4) - (Nb * \kappa * w[[ib]] * tb) / \\ l[[ib]] * (T - Ta[[ib]])); \\ ~~~~~~$$

\* The range of the reaction heat absorption coefficient is compressed to  
 \* home in on the optimal value with increased resolution. This range can be  
 \* adjusted.

$$\alpha = \text{Range}[0.2, 0.3, 0.01]; \\ \{n\alpha\} = \text{Dimensions}[\alpha]; \\ \text{betam} = \text{zeros}; \\ K0m = \text{zeros}; \\ ~~~~~~$$

\* Initialization of the model parameters and the statistical parameters.

```
For[ib = 1, ib <= md, ib++,
  rootbeta = FindRoot[fm[β], {β}, 2000], AccuracyGoal -> 4];
  betam[[ib]] = β /. {rootbeta[[1]]};
  K0m[[ib]] = g[betam[[ib]], hm[[ib]]];
]
```

```

~~~~~
T α = ConstantArray[0, {md, n α };
residual = ConstantArray[0, {md, n α };
resbar = ConstantArray[0, n α];
resstdev = ConstantArray[0, n α];
sse = ConstantArray[0, n α];
sst = ConstantArray[0, n α];
Rsq = ConstantArray[0, n α];
~~~~~

```

\* The main loops in which the temperature for each structure is predicted for each value of  $\alpha$  and the  
\* statistics calculated to determine the goodness of fit to the data. Outer loop for values of  $\alpha$ . Inner  
\* loop for predicted temperatures.

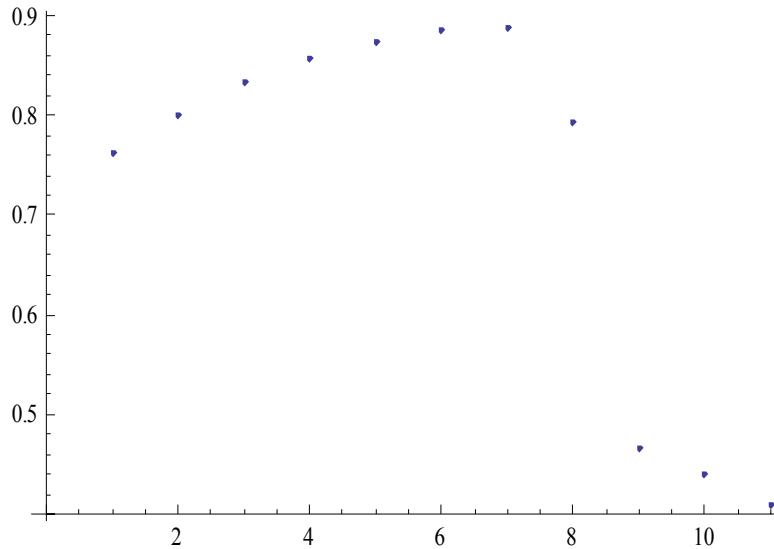
```

~~~~~
For[jb=1,jb<=n α ,,jb++,
 h α =hm;
 beta α =betam;
 K0 α =K0m;
 T α [[All,jb]]=Tm;
 For[ib=1,ib<=md,ib++,
 Titer=0;
 iter=1;
 While[Abs[Titer-T α [[ib,jb]]]>=Ttol,
 (*if the convergence to the root is too slow, take the average of the two values*)
 If[iter==30,
 T α [[ib,jb]]=(T α [[ib,jb]]+Titer)/2;
 Goto[endrow]
];
 Titer=T α [[ib,jb]];
 rootT=FindRoot[P[T],{T,300},AccuracyGoal->4];
 T α [[ib,jb]]=T/.{rootT[[1]]};
 h α [[ib]]=4* ρ Si/ μ Si*(AA*T α [[ib,jb]]^0.5*
 Exp[-(EA/(kB*T α [[ib,jb]])))/DF;
 rootbeta=FindRoot[f α [β],{ β ,2000},
 AccuracyGoal->4];
 beta α [[ib]]= β /.{rootbeta[[1]]};
 K0 α [[ib]]=g[beta α [[ib]],h α [[ib]];
 iter++;
];
 Label[endrow];
];
 residual[[All,jb]]=Tm-T α [[All,jb]];
 resbar[[jb]]=Mean[residual[[All,jb]]];
 resstdev[[jb]]=StandardDeviation[residual[[All,jb]]];
 For [i=1,i<=md,i++,
 sse[[jb]]=sse[[jb]]+residual[[i,jb]]^2;
 sst[[jb]] = sst[[jb]]+(Tm[[i]]-Tmbar)^2;
];
 Rsq[[jb]]=1-sse[[jb]]/sst[[jb]];
]
~~~~~

```

```
# Rsq = {0.76366, 0.801427, 0.832567, 0.857052, 0.874673, 0.885349,  
0.889218, 0.793282, 0.467362, 0.441062, 0.408621}
```

```
ListPlot[Rsqr](*the vertical axis represents Rsqr and is dimensionless*)
```

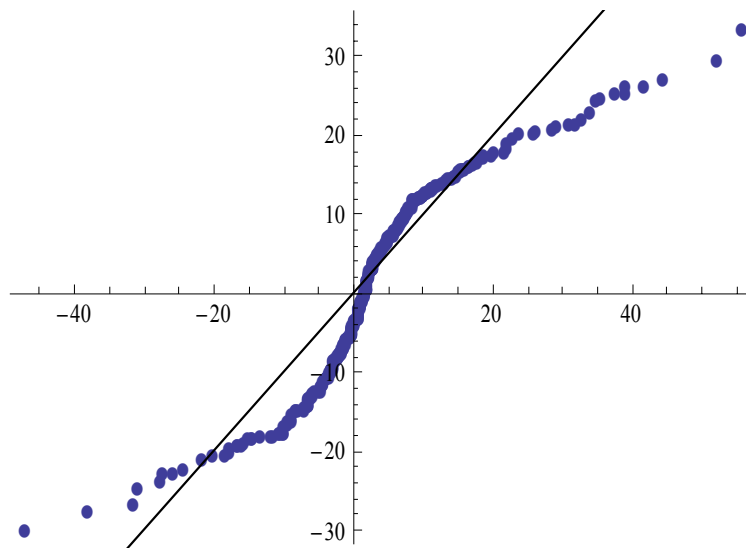


```
* Generate a set of normally distributed data with the same mean and  
* standard deviation as the residuals. The identification of the optimal  
* value for alpha is done manually and the following part of the code  
* has to be modified to apply the correct element of the alpha list.
```

```
norm = RandomReal[NormalDistribution[0, resstdev[[7]]], md];  
output = ConstantArray[0, {md, 3}];  
output[[All, 1]] = Talpha[[All, 7]];  
output[[All, 2]] = residual[[All, 7]];  
output[[All, 3]] = norm;  
Export["final_output.txt", output, "Table"];
```

```
* Reload the output data to make a quantile-quantile plot.
```

```
SetDirectory["C:\\Documents and Settings\\gilgunn\\Desktop\\PhD\\  
Publications\\JMM\\Etch Heating Paper\\"];  
data = Import["final_output.txt", "Table"];  
QuantilePlot[data[[All, 2]], data[[All, 3]]
```



## D.7 Microloading Filter Function

A Comsol Multiphysics<sup>®</sup> model (3.5a with Matlab<sup>®</sup>) was devised to simulate the variation in F concentration at the center of a resist masked Si wafer based on the radius of a circular area of exposed etching Si at the center of the wafer. The axi-symmetric simulation in cylindrical coordinates is looped over the geometry of the structure for a given stagnation zone thickness above the wafer. The output is an array of F concentrations along the surface of the wafer for various central hole radii at linearly spaced points from the center of the wafer to the edge. The analysis of the simulated data is performed offline so no plotting or post-processing commands are built into the script. The user can modify the thickness of the stagnation zone and alter the boundary conditions to simulate different chamber type conditions.

---

```

fileclear fem

% COMSOL version
clear vrsn
vrsn.name = 'COMSOL 3.5';
vrsn.ext = 'a';
vrsn.major = 0;
vrsn.build = 603;
vrsn.rcs = '$Name: $';
vrsn.date = '$Date: 2008/12/03 17:02:19 $';

```

---

```

fem.version = vrsn;

% Constants
fem.const = {'De','80.2', ...
            'EA','5.6e-21', ...
            'D','0.5', ...
            'cF','5.5e-5', ...
            'kB','1.38e-23', ...
            'Te','300'};

% Descriptions
clear descr
descr.const= {'D','diffusion coefficient','EA','activation energy','De',...
            'etching flux constant','Te','etching temperature','kB',...
            'Boltzmann constant','cF','bulk concentration'};
fem.descr = descr;

% Parameters defining structure
R = 60e-3; % radius of the Si wafer plus an extended region
ts = 50e-3; % thickness of the stagnation zone above the wafer surface
% radius of central circle of exposed Si
r = [1e-6, 50e-6, 0.1e-3, 1e-3, 5e-3, 10e-3, 20e-3];

[mr,nr] = size(r);
rho = [0,linspace(1e-6,9e-6,18),linspace(1e-5,9e-5,18),linspace(1e-4,9e-4,18)...
        linspace(1e-3,9e-3,36),linspace(1e-2,6e-2,48)];
[mrho,nrho]=size(rho);
z = zeros(1,nrho);
p = [rho;z];

cout = zeros(nrho,nr);

for ir = 1:nr

    % Geometry
    g1=rect2(R,ts,'base','corner','pos',{'0','0'},'rot','0');
    g2=curve2([0,r(ir)],[0,0]);

    % Analyzed geometry
    clear c s
    c.objs={g2};
    c.name={'B1'};
    c.tags={'g2'};

    s.objs={g1};
    s.name={'R1'};
    s.tags={'g1'};

    fem.draw=struct('c',c,'s',s);
    fem.geom=geomcsg(fem);

    % Initialize mesh

```

```

fem.mesh=meshinit(fem,'hauto',2);

% Application mode 1
clear appl
appl.mode.class = 'FICnvDiff';
appl.mode.type = 'axi';
appl.dim = {'c2'};
appl.name = 'cd2';
appl.assignsuffix = '_cd2';
clear prop
prop.analysis='static';
clear weakconstr
weakconstr.value = 'off';
weakconstr.dim = {'lm2'};
prop.weakconstr = weakconstr;
appl.prop = prop;
clear bnd
bnd.c0 = {0,0,0,'cF'};
bnd.name = {'no_etching','axi_sym','etching','source'};
bnd.N = {0,0,'-De*c2*Te^0.5*exp(-EA/kB/Te)',0};
bnd.type = {'N0','ax','N','C'};
bnd.ind = [2,3,4,1,1];
appl.bnd = bnd;
clear equ
equ.D = 'D';
equ.ind = [1];
appl.equ = equ;
fem.app{1} = appl;
fem.sdim = {'r','z'};
fem.frame = {'ref'};
fem.border = 1;
fem.outform = 'general';
clear units;
units.basesystem = 'SI';
fem.units = units;

% ODE Settings
clear ode
clear units;
units.basesystem = 'SI';
ode.units = units;
fem.ode=ode;

% Multiphysics
fem=multiphysics(fem);

% Extend mesh
fem.xmesh=meshextend(fem);

% Solve problem
fem.sol=femstatic(fem, ...
    'solcomp',{'c2'}, ...

```

```
'outcomp',{c2}, ...  
'blocksize','auto');  
  
cstep = postinterp(fem,'c2',p);  
cout(:,ir) = cstep';  
end  
  
% Save current fem structure for restart purposes  
fem0=fem;
```

---

## D.8 Reaction Probability Via Dushman

This Matlab<sup>®</sup> m-file uses the Dushman conductance correction factor in the Coburn and Winters ARDE model to calculate etch depths for cylinders and rectangular trenches at various points in time using an analytic expression. The predictions are statistically compared to empirical depths to identify the value of reaction probability that produces the best fit to the entire data set. The trenches and cylinders are assumed to be isolated so only self-loading of each structure is considered.

The spatial and macroloading components of the etch rate variation are determined based on empirical correlations. The microloading of each structure is calculated based on analytic formulae specific to the structure. The surface etch rate value is the product of these three terms.

---

```
clear all  
  
% Anisotropic process parameters  
ta = 60; % anisotropic process time in minutes  
te = 12; % anisotropic process etch step time in seconds  
tp = 8; % anisotropic process passivation step time in seconds  
Nc = 60*60/(te+tp)-1; % number of anisotropic etch cycles  
% "-1" because first cycle doesn't etch  
e = 6.5; % number of seconds per cycle during which Si is etching  
T = Nc*e; % total amount of time that Si is etching  
% iteration time step for depth calculations, etch rate is assumed constant during this period  
tstep = 0.5;  
Sstep = 0.01; % reaction probability resolution  
S = (0.15:Sstep:0.25); % reaction probabilities  
[null,imax] = size(S);  
imax = ceil(T/tstep);  
  
% Microloading parameters  
a = 1.4; % microloading scaling factor per meter
```



```

% Trench structure parameters
Tm = 2.5e-6; % resist mask thickness in meters
% characteristic cylinder dimension, diameter in meters
dc = [12.1,22.1,42.1,82.1,102.1,202.1,402.1,642.1,962.1,1282.1,2002.1]/1e6;
rc = [20,10,10,20,0,20,20,20,20,10,10]*1e-3; % radial location of cylinders
[mc,nc] = size(dc); % number of cylinder structures
% trench width in meters
wt = [6.7,11.7,21.7,41.7,51.7,101.7,201.7,321.7,481.7,641.7,1001.7]/1e6;
% radial location of trenches
rt = [20,10,10,20,0,20,20,20,20,10,10]*1e-3;
ltow = 10; % trench length to width aspect ratio
lt = ltow*wt;
dt = 2*lt.*wt./(lt+wt); % characteristic trench dimension
[mt,nt] = size(dt); % number of trench structures

% Load raw data from file and parse
data = load('raw_depth_data_cyl_trench.txt');
[md,nd] = size(data);
tm = data(3:md,1); % Si etch times
Dmeas = data(3:md,2:nc+nt+1)*1e-6; % measured depth data

% Statistical variables
SSE = zeros(1,ismax); % sum of the squared model error
Rsquared = zeros(1,ismax); % correlation coefficient for model fit

Doc = zeros(size(dc)); % cylinder etch depth assuming no ARDE
Dot = zeros(size(dt)); % trench etch depth assuming no ARDE

Mpc = 0.05; % cylinder macroloading
Mpt = 0.052; % trench macroloading

% Calculate the surface etchrate at the geometric center of each trench incorporating microloading,
% macroloading and spatial variation
ERc = 37*Mpc^2-104*Mpc+140; % cylinder etch rate at the center of the wafer
ERt = 37*Mpt^2-104*Mpt+140; % trench etch rate at the center of the wafer

% spatial variation in etch rate for each structure
ERsc = ERc*((3400*Mpc+1340)*rc.^3-60*rc.^2+rc+1); % cylinder
ERst = ERt*((3400*Mpt+1340)*rt.^3-60*rt.^2+rt+1); % trench

% Calculate the microloading for each structure
upc = pi*a*dc; %cylinder
upt = 2*a*dt*(log(sqrt(0.5*(1+(ltow^2+1)^-0.5))+sqrt(0.5*(1-(ltow^2+1)^-0.5)))-
log(sqrt(0.5*(1+(ltow^2+1)^-0.5))-sqrt(0.5*(1-(ltow^2+1)^-0.5))))+...
ltow*(log(sqrt(0.5*(1+(ltow^2+1)^-0.5)))-log(sqrt(0.5*(1-(ltow^2+1)^-0.5)))); % trench
%upt = 8*a*dt is the simplified version for the fixed l:w

% the surface etch rate at the geometric center of each structure
ER0c = (1-upc).*ERsc*1e-9; % cylinder
ER0t = (1-upt).*ERst*1e-9; % trench

```

```

% Compute the etch depth for each structure for each reaction probability S
for is = 1:ismax

    Dc = zeros(size(dc)); % Initialize depth for each cylinder
    Dt = zeros(size(dt)); % same for the trench

    for i = 1:md-2
        % calculate cylinder depth
        tempc = 4*dc/3/S(is)+Tm;
        Dc(i,:)=sqrt(8*dc.*ER0c*tm(i)/3/S(is)+tempc.^2)-tempc;
        % calculate trench depth
        tempt = 4*dt/3/S(is)+Tm;
        Dt(i,:)=sqrt(8*dt.*ER0t*tm(i)/3/S(is)+tempt.^2)-tempt;
        % calculate reference depths that assume no ARDE
        Doc(i,:) = ER0c*tm(i); % cylinder
        Dot(i,:) = ER0c*tm(i); % trench
    end

    Dref = [Doc,Dot];
    D = [Dc,Dt];

    % Calculate the sum of squared errors and the R-squared value for this value of S.
    Nmeas = Dmeas./Dref; % normalize measured data to open field depth
    Npred = D./Dref; % normalize predicted depth to open field depth

    Nmeasbar = mean(Nmeas);
    Nmeasbar = mean(Nmeasbar);
    Nmeasstd = std(Nmeas);

    res_sq = (Nmeas - Npred).^2; % calculate squared residuals
    sse = sum(res_sq);
    SSE(1,is) = sum(sse); % sum of the squared errors

    err_sq = (Nmeas - Nmeasbar).^2; % calculate squared error
    sst = sum(err_sq);
    sst = sum(sst); % sum of squared total error

    Rsquared(is) = 1- SSE(is)/sst;
end

plot(S,SSE)

Sopt = 0;

% Determine best fit S value
for is = 2:ismax
    if SSE(is) < SSE(is-1)
        Sopt = S(is);
        Rsqopt = Rsquared(is);
    end
end
end
% This is the end of the first part of the code

```

```
% Use the optimal value of S to calculate the Dushman-based prediction of etch depth for output
Dc = zeros(size(dc)); % Tm is initial depth for each cylinder
Dt = zeros(size(dt)); % same for the trench
Sopt = 0.22;
for i = 1:md-2
    % calculate cylinder depth
    tempc = 4*dc/3/Sopt+Tm;
    Dc(i+1,:)=sqrt(8*dc.*ER0c*tm(i)/3/Sopt+tempc.^2)-tempc;
    % calculate trench depth
    tempt = 4*dt/3/Sopt+Tm;
    Dt(i+1,:)=sqrt(8*dt.*ER0t*tm(i)/3/Sopt+tempt.^2)-tempt;
end
Output = [[0;tm],Dc,Dt]; % compile a table of depth vs time for each structure
```

---

## D.9 Reaction Probability Via Clausing

This file uses the Clausing conductance correction factor in the Coburn and Winters ARDE model to calculate etch depths for cylinders and rectangular trenches at various points in time. The predictions are statistically compared to empirical depths to identify the value of reaction probability  $S$  that produces the best fit to the entire data set. The trenches and cylinders are assumed to be isolated so only self-loading of each structure is considered.

The spatial and macroloading components of the etch rate variation are determined based on empirical correlations. The microloading of each structure is calculated based on analytic formulae specific to the structure. The surface etch rate value is the product of these three terms.

The Clausing vacuum conductance correction factor  $K$  is determined for each feature size and mask thickness and used to initialize the etch rate  $ER(T_{\text{mask}}/d)$  for a given value of reaction probability  $S$ . The sidewalls of the structure are assumed to be vertical throughout the etch process. The etch rate is assumed constant over a small time step  $t_{\text{step}}$  and used to determine a depth step  $dD$  which is added to the current depth  $D$  (i.e.  $D[n] = D[n-1] + dD$ ). After each depth step, the Clausing conductance factor is re-evaluated and used to determine the etch rate at the new depth  $ER(D[n]/d)$ . When etch depths have

been predicted at all times and for all structures, the residuals of the model are calculated. These steps are looped over a range of S to find that value which leads to the minimum residual.

---

clear all

% Anisotropic process parameters

ta = 60; % anisotropic process time in minutes

te = 12; % anisotropic process etch step time in seconds

tp = 8; % anisotropic process passivation step time in seconds

Nc = 60\*60/(te+tp)-1; % number of anisotropic etch cycles

% "-1" because first cycle doesn't etch

e = 6.5; % number of seconds per cycle during which Si is etching

T = Nc\*e; % total amount of time that Si is etching

% iteration time step for depth calculations, etch rate is assumed constant during this period

tstep = 0.5;

time = zeros(1); % etch time in algorithm

Sstep = 0.01; % reaction probability resolution

S = (0.15:Sstep:0.25); % reaction probabilities

[null,ismax] = size(S);

imax = ceil(T/tstep);

% Microloading parameters

a = 1.4; % microloading scaling factor per meter

% Trench structure parameters

Tm = 2.5e-6; % resist mask thickness in meters

% characteristic dimension, cylinder diameter in meters

dc = [12.1,22.1,42.1,82.1,102.1,202.1,402.1,642.1,962.1,1282.1,2002.1]/1e6;

rc = [20,10,10,20,0,20,20,20,20,10,10]\*1e-3; % radial location of cylinders

[mc,nc] = size(dc); % number of cylinder structures

% trench width in meters

wt = [6.7,11.7,21.7,41.7,51.7,101.7,201.7,321.7,481.7,641.7,1001.7]/1e6;

% radial location of trenches

rt = [20,10,10,20,0,20,20,20,20,10,10]\*1e-3;

ltow = 10; % trench length to width aspect ratio

[mt,nt] = size(wt); % number of trench structures

Kclog = zeros(imax,nc); % for troubleshooting the code

%Ktlog = zeros(imax,nt); % for troubleshooting the code

% Load raw data from file and parse

data = load('raw\_depth\_data\_cyl\_trench.txt');

[md,nd] = size(data);

tm = data(2:md,1);

Dmeas = data(3:md,2:nc+nt+1)\*1e-6;

% Statistical variables

SSE = zeros(1,ismax); % sum of the squared model error

Rsquared = zeros(1,ismax); % correlation coefficient for model fit

% normalized depths in cylinder and trench at which Clausing alpha factor is calculated

---

```

xsc = zeros(1,nc);
xst = zeros(1,nt);

Doc = zeros(size(dc)); % cylinder etch depth assuming no ARDE
Dot = zeros(size(wt)); % trench etch depth assuming no ARDE

Mpc = 0.05; % cylinder macroloading
Mpt = 0.052; % trench macroloading

% Calculate the surface etchrate at the geometric center of each trench
% incorporating microloading, macroloading and spatial variation
ERc = 37*Mpc^2-104*Mpc+140; % cylinder etch rate at the center of the wafer
ERt = 37*Mpt^2-104*Mpt+140; % trench etch rate at the center of the wafer

% spatial variation in etch rate for each structure
ERsc = ERc*((3400*Mpc+1340)*rc.^3-60*rc.^2+rc+1); % cylinder
ERst = ERt*((3400*Mpt+1340)*rt.^3-60*rt.^2+rt+1); % trench

% Calculate the microloading for each structure
upc = pi*a*dc; %cylinder
upt = 2*a*dt*(log(sqrt(0.5*(1+(ltow^2+1)^-0.5))+sqrt(0.5*(1-(ltow^2+1)^-0.5)))-
log(sqrt(0.5*(1+(ltow^2+1)^-0.5))-sqrt(0.5*(1-(ltow^2+1)^-0.5))))+...
ltow*(log(sqrt(0.5*(1+(ltow^2+1)^-0.5)))-log(sqrt(0.5*(1-(ltow^2+1)^-0.5)))); % trench
%upt = 23.64*a*wt is the simplified version for the fixed l:w

% the surface etch rate at the geometric center of each structure
ER0c = (1-upc).*ERsc*1e-9; % cylinder
ER0t = (1-upt).*ERst*1e-9; % trench

% Compute the etch depth for each structure for each reaction probability S
for is = 1:ismax
    % Initialize the ARDE etch terms
    % normalized depth with which the Clausing alpha factor is calculated
    xsc = (1+3*Tm./dc/sqrt(7)).^-1; % cylinder

    for it = 1:nt % trench
        if wt(it) <= Tm
            xst(it) = (1+2*Tm/wt(it)/log(Tm/wt(it)))^-1;
        else
            xst(it) = 0;
        end
    end
end

Dc = zeros(size(dc))+Tm; % Tm is initial depth for each cylinder
Dt = zeros(size(wt))+Tm; % same for the trench

% Clausing alpha factor
aCc = (xsc.^2-(1-xsc).^2+(1-xsc).*sqrt((1-xsc).^2+(dc./Dc).^2)-...
xsc.*sqrt(xsc.^2+(dc./Dc).^2))./((xsc.^2-(2*xsc-1).*(xsc.^2+...
(dc./Dc).^2))./sqrt(xsc.^2+(dc./Dc).^2)-((1-xsc).^2-(2*(1-xsc)...
-1).*((1-xsc).^2+(dc./Dc).^2))./sqrt((1-xsc).^2+(dc./Dc).^2));

```

```
aCt = (1-2*xst-sqrt((1-xst).^2+(wt./Dt).^2)+sqrt(xst.^2+(wt./Dt).^2))./...
      (2-4*xst-2*sqrt((1-xst).^2+(wt./Dt).^2)+2*sqrt(xst.^2+...
      (wt./Dt).^2)+(1-xst)./sqrt((1-xst).^2+(wt./Dt).^2)-...
      xst./sqrt(xst.^2+(wt./Dt).^2));
```

**% Clausing vacuum conductance correction factor**

```
Kc = 4*(1-2*aCc).*((dc./Dc)/2+((dc./Dc).^2-0.5).*sqrt(1+(dc./Dc).^2)-...
      (dc./Dc).^2)/3+aCc+2*(1-aCc).*((dc./Dc).^2-(dc./Dc).^-1.*...
      sqrt((dc./Dc).^2+1)+0.5);
```

```
Kt = aCt.*(1-wt.*log((Dt+sqrt(Dt.^2+wt.^2))./wt)./Dt)-Dt./wt/2+...
      sqrt(Dt.^2+wt.^2)/2./wt+wt.*log((Dt+sqrt(Dt.^2+wt.^2))./wt)./Dt/2;
```

**% etch rate at the start of the etch process**

```
ERc = ER0c./(1+S(is)*(Kc.^-1-1));
ERt = ER0t./(1+S(is)*(Kt.^-1-1));
```

**% loop for cylinders**

```
for i = 2:imax+1
    time(i,1) = (i-1)*tstep; % time in seconds
    % calculate reference depths that assume no ARDE
    Doc(i,:) = Doc(i-1,:) + ER0c*tstep; % cylinder
    Dot(i,:) = Dot(i-1,:) + ER0t*tstep; % trench

    Dc(i,:) = Dc(i-1,:) + ERc*tstep; % new depth after a time step

    % calculate the etch rate at the new depth
    xsc = (1+3*Dc(i,:)./dc/sqrt(7)).^-1;
    aCc = (xsc.^2-(1-xsc).^2+(1-xsc).*sqrt((1-xsc).^2+...
          (dc./Dc(i,:).^2)-xsc.*sqrt(xsc.^2+(dc./Dc(i,:).^2))./...
          ((xsc.^2-(2*xsc-1)*(xsc.^2+(dc./Dc(i,:).^2))./sqrt(xsc.^2+...
          (dc./Dc(i,:).^2)-((1-xsc).^2-(2*(1-xsc)-1)*((1-xsc).^2+...
          (dc./Dc(i,:).^2))./sqrt((1-xsc).^2+(dc./Dc(i,:).^2)));

    Kc = 4*(1-2*aCc).*((dc./Dc(i,:))/2+((dc./Dc(i,:)).^2-0.5).*...
          sqrt(1+(dc./Dc(i,:).^2)-(dc./Dc(i,:)).^2)/3+aCc+2*(1-aCc).*...
          ((dc./Dc(i,:)).^2-(dc./Dc(i,:)).^-1.*sqrt((dc./Dc(i,:)).^2+...
          1)+0.5);

    ERc = ER0c./(1+S(is)*(Kc.^-1-1));
end
```

**% loop for trenches**

```
for i = 2:imax+1
    Dt(i,:) = Dt(i-1,:) + ERt*tstep; % new depth after a time step
    % calculate the etch rate at the new depth
    for it = 1:nt
        if wt(it) <= Dt(i,it)
            xst(it) = (1+2*Dt(i,it)/wt(it)/log(Dt(i,it)/wt(1,it)))^-1;
        else
            xst(1,it) = 0;
        end
    end
```

```

end
aCt = (1-2*xst-sqrt((1-xst).^2+(wt./Dt(i,:)).^2)+sqrt(xst.^2+...
    (wt./Dt(i,:)).^2))./(2-4*xst-2*sqrt((1-xst).^2+(wt./Dt(i,:)).^...
    2)+2*sqrt(xst.^2+(wt./Dt(i,:)).^2)+(1-xst)./sqrt((1-xst).^2+...
    (wt./Dt(i,:)).^2)-xst./sqrt(xst.^2+(wt./Dt(i,:)).^2));

Kt = aCt.*(1-wt.*log((Dt(i,:)+sqrt(Dt(i,:).^2+wt.^2))./wt)./...
    Dt(i,:)-Dt(i,:)./wt/2+sqrt(Dt(i,:).^2+wt.^2)/2./wt+wt.*...
    log((Dt(i,:)+sqrt(Dt(i,:).^2+wt.^2))./wt)./Dt(i,:)/2);

ERt = ER0t./(1+S(is)*(Kt.^-1-1));
end

Do = [Doc,Dot];
Dc = Dc - Tm; % subtract out the mask thickness to obtain depth in Si
Dt = Dt - Tm;
D = [Dc,Dt];

% Extract the predicted values for the experimental times
for j = 2:md-1
    for i = 2:imax+1
        if time(i) == tm(j)
            Dpred(j-1,:) = D(i-1,:);
            Dref(j-1,:) = Do(i-1,:);
        end
    end
end

% Calculate the sum of squared errors and the R-squared value for this
% value of S.
Nmeas = Dmeas./Dref; % normalize measured data to open field depth
Npred = Dpred./Dref; % normalize predicted depth to open field depth

Nmeasbar = mean(Nmeas);
Nmeasbar = mean(Nmeasbar);
Nmeasstd = std(Nmeas);

res_sq = (Nmeas - Npred).^2; % calculate squared residuals
sse = sum(res_sq);
SSE(1,is) = sum(sse); % sum of the squared errors

err_sq = (Nmeas - Nmeasbar).^2; % calculate squared error
sst = sum(err_sq);
sst = sum(sst); % sum of squared total error

Rsquared(is) = 1- SSE(is)/sst;
end

plot(S,SSE)

Sopt = 0;

```

```

% Determine best fit S value
for is = 2:ismax
    if SSE(is) < SSE(is-1)
        Sopt = S(is);
        Rsqopt = Rsquared(is);
    end
end
% This is the end of the first part of the code

% Use the optimal value of S to calculate the Clausing-based prediction ofetch depth for output
% reinitialize the ARDE etch terms the normalized depth with which the Clausing alpha factor is
% calculated
xsc = (1+3*Tm./dc/sqrt(7)).^-1; % cylinder

for it = 1:nt % trench
    if wt(it) <= Tm
        xst(it) = (1+2*Tm/wt(it)/log(Tm/wt(it)))^-1;
    else
        xst(it) = 0;
    end
end

Dc = zeros(size(dc))+Tm; % Tm is the initial depth for each cylinder
Dt = zeros(size(wt))+Tm; % same for the trench

% Clausing alpha factor
aCc = (xsc.^2-(1-xsc).^2+(1-xsc).*sqrt((1-xsc).^2+(dc./Dc).^2)-xsc.*...
    sqrt(xsc.^2+(dc./Dc).^2))./((xsc.^2-(2*xsc-1).*(xsc.^2+(dc./Dc).^2))./...
    sqrt(xsc.^2+(dc./Dc).^2)-((1-xsc).^2-(2*(1-xsc)-1).*((1-xsc).^2+...
    (dc./Dc).^2))./sqrt((1-xsc).^2+(dc./Dc).^2));

aCt = (1-2*xst-sqrt((1-xst).^2+(wt./Dt).^2)+sqrt(xst.^2+...
    (wt./Dt).^2))./(2-4*xst-2*sqrt((1-xst).^2+(wt./Dt).^2)+...
    2*sqrt(xst.^2+(wt./Dt).^2)+(1-xst)./sqrt((1-xst).^2+...
    (wt./Dt).^2)-xst./sqrt(xst.^2+(wt./Dt).^2));

% Clausing vacuum conductance correction factor
Kc = 4*(1-2*aCc).*((dc./Dc)/2+((dc./Dc).^2-0.5).*sqrt(1+(dc./Dc).^2)-...
    (dc./Dc).^2)/3+aCc+2*(1-aCc).*((dc./Dc).^2-(dc./Dc).^-1.*...
    sqrt((dc./Dc).^2+1)+0.5);

Kt = aCt.*(1-wt.*log((Dt+sqrt(Dt.^2+wt.^2))./wt)./Dt)-Dt./wt/2+...
    sqrt(Dt.^2+wt.^2)/2./wt+wt.*log((Dt+sqrt(Dt.^2+wt.^2))./wt)./Dt/2;

% etch rate at the start of the etch process
ERc = ER0c./(1+Sopt*(Kc.^-1-1));
ERt = ER0t./(1+Sopt*(Kt.^-1-1));

imax = ceil(T/tstep);

% loop for cylinders
for i = 2:imax+1

```



```

Dc(i,:) = Dc(i-1,:) + ERc*tstep; % new depth after a time step
% calculate the etch rate at the new depth
xsc = (1+3*Dc(i,:)/dc/sqrt(7)).^-1;
aCc = (xsc.^2-(1-xsc).^2+(1-xsc).*sqrt((1-xsc).^2+(dc./Dc(i,:)).^2)-...
xsc.*sqrt(xsc.^2+(dc./Dc(i,:)).^2))./((xsc.^2-(2*xsc-1).*(xsc.^2+...
(dc./Dc(i,:)).^2))./sqrt(xsc.^2+(dc./Dc(i,:)).^2)-((1-xsc).^2-...
(2*(1-xsc)-1).*((1-xsc).^2+(dc./Dc(i,:)).^2))./sqrt((1-xsc).^2+...
(dc./Dc(i,:)).^2));

Kc = 4*(1-2*aCc).*(dc./Dc(i,:))./2+((dc./Dc(i,:)).^-2-0.5).*sqrt(1+...
(dc./Dc(i,:)).^2)-(dc./Dc(i,:)).^-2)/3+aCc+2*(1-aCc).*...
((dc./Dc(i,:)).^-2-(dc./Dc(i,:)).^-1.*sqrt((dc./Dc(i,:)).^-2+...
1)+0.5);

ERc = ER0c./(1+Sopt*(Kc.^-1-1));
end

% loop for trenches
for i = 2:imax+1
Dt(i,:) = Dt(i-1,:) + ERt*tstep; % new depth after a time step
% calculate the etch rate at the new depth
for it = 1:nt
if wt(it) <= Dt(i,it)
xst(it) = (1+2*Dc(i,it)/wt(it)/log(Dt(i,it)/wt(1,it)))^-1;
else
xst(1,it) = 0;
end
end
aCt = (1-2*xst-sqrt((1-xst).^2+(wt./Dt(i,:)).^2)+sqrt(xst.^2+...
(wt./Dt(i,:)).^2))./(2-4*xst-2*sqrt((1-xst).^2+(wt./Dt(i,:)).^2)+...
2*sqrt(xst.^2+(wt./Dt(i,:)).^2)+(1-xst)./sqrt((1-xst).^2+...
(wt./Dt(i,:)).^2)-xst./sqrt(xst.^2+(wt./Dt(i,:)).^2));

Kt = aCt.*(1-wt.*log((Dt(i,:)+sqrt(Dt(i,:).^2+wt.^2))./wt)./...
Dt(i,:))-Dt(i,:)./wt/2+sqrt(Dt(i,:).^2+wt.^2)/2./wt+wt.*...
log((Dt(i,:)+sqrt(Dt(i,:).^2+wt.^2))./wt)./Dt(i,:)/2;

ERt = ER0t./(1+Sopt*(Kt.^-1-1));
end

Dc = Dc - Tm; % subtract out the mask thickness to obtain depth in Si
Dt = Dt - Tm;

Output = [time,Dc,Dt]; % compile a table of depth vs time for each structure
%save Clausing_model_output.txt Output - ascii -tab

```

## D.10 Etch Model With Microloading Convolution

This script calculates the surface etchrate  $ER(0)$  at a point  $(x,y)$  on a 20 mm square based on its layout-driven microloading and macroloading and the spatial variation model for the etch chamber. The microloading at the geometric center of a site is determined as the convolution of the layout file and a pattern weighting function.

The Clausing vacuum conductance correction factor  $K$  is determined for the feature sizes and mask thickness and used to initialize the etch rate  $ER(T_m/w)$  for each feature. The etch rate is assumed constant over a small time step  $dT$  and used to determine a depth step  $dD$  which is added to the current depth  $D$  (i.e.  $D[n] = D[n-1] + dD$ ). After each depth step, the Clausing conductance factor is re-evaluated and used to determine the etch rate at the new depth  $ER(D[n]/d)$ .

---

```
% Anisotropic process parameters
ta = 60; % anisotropic process time in minutes
te = 12; % anisotropic process etch step time in seconds
tp = 8; % anisotropic process passivation step time in seconds
Nc = 60*60/(te+tp); % number of anisotropic etch cycles
e = 6.5; % number of seconds of each cycle during which Si is etching
T = fix(Nc*e); % total amount of Si etching time
% iteration time step for depth calculations, etch rate is assumed constant during this period
tstep = 1;
S = 0.22; % Si-F reaction probability
time = zeros(1); % etch time in algorithm

% Spatial filter parameters
a = 14e-6; % filter scaling factor per pixel
p = 10e-6; % pixel size in meters
lfx = 2048; % length of filter in x in pixels
lfy = 2048; % length of filter in y in pixels
pcx = ceil(lfx/2); % center filter pixel in x
pcy = ceil(lfy/2); % center filter pixel in y

% Trench structure parameters
Tm = 2.5e-6; % resist mask thickness in meters
wm = [10,20,50,100,200,480,1000]/1e6; % trench width in microns
% structure widths in pixels, based on widths in microns
wt = wm/p;
w = [wm, wm, wm, wm]; % width of trenches in pixels
ww = 20/p/1e6; % number of unexposed pixels around each trench
[mt,nt] = size(wt); % number of trench structures
step = lfx/(nt+1)/2; % number of pixel steps between trenches
ax_loc = (1:7)*step; % axial pixel location of each trench center from zero
Q = 4; % four quadrants of differing density
```

---

```

upT1 = zeros(1,nt); % microloading parameter for quadrant 1 trenches
upT2 = zeros(1,nt); % microloading parameter for quadrant 2 trenches
upT3 = zeros(1,nt); % microloading parameter for quadrant 3 trenches
upT4 = zeros(1,nt); % microloading parameter for quadrant 4 trenches
% normalized depth in trench at which Clausing alpha factor is calculated
xs = zeros(1,Q*nt);
D = zeros(size(w)); % trench depth

% Generating the spatial filter
W = zeros(lfx,lfy); % initialize the filter
P = zeros(lfx,lfy); % initialize the density pattern
Tr = zeros(lfx,lfy); % initialize the trenches
Pw = ones(lfx,lfy); % initialize the walls around the trenches

for i = 1:lfx
    for j = 1:lfy
        % radial distance of each pixel from center pixel in pixels
        r = sqrt(abs(pcx-i)^2+abs(pcy-j)^2);
        if r ~= 0
            W(i,j) = a/r; % filter value for each pixel
        else
            W(i,j) = a/0.85; % filter value for center pixel
        end
    end
end
end

% Generating the mask structure
% This section of code generates an array of trenches of various widths but with length = 10*width.
% The trenches are areas of exposed Si represented by the value "1". Resist covered Si is
% represented by the value "0". The trenches are evenly spaced along the axis of the pattern
% radiating out from the center. Each trench array lies within a quadrant of varying pattern density.
% The pattern density is varied through the frequency of "0"-valued pixels.

% generate a single array of trenches and a single array of walls
for it = 1:nt
    Tr(fix(pcy-5*wt(it)):fix(pcy+5*wt(it))-1, pcx+fix(ax_loc(it)-...
        wt(it)/2):pcx+fix(ax_loc(it)+wt(it)/2)-1)=1;
    Pw(fix(pcy-(5*wt(it)+ww)):fix(pcy+(5*wt(it)+ww))-1, pcx+fix(ax_loc(it)-...
        (wt(it)/2+ww)):pcx+fix(ax_loc(it)+(wt(it)/2+ww))-1)=0;
end

% Rotate the matrix to generate the trench and wall arrays in the other quadrants
Tr = Tr + rot90(Tr)+rot90(Tr,2)+rot90(Tr,3);
Pw = Pw.*rot90(Pw);
Pw = Pw.*rot90(Pw,2);

% fill the quadrants with varying densities of "1"-valued pixels
% quadrant 1
% density = 33%;
for y = 1026:4:2048
    for x = pcx:-3:2*pcx-y+1
        P(x,y) = 1;
    end
end

```

```
end
  for x = pcx:3:y-1
    P(x,y) = 1;
  end
end
for y = 1027:2:2048
  for x = pcx-1:-3:2*pcx-y+1
    P(x,y) = 1;
  end
  for x = pcx+1:3:y-1
    P(x,y) = 1;
  end
end
for y = 1028:4:2048
  for x = pcx-2:-3:2*pcx-y+1
    P(x,y) = 1;
  end
  for x = pcx+2:3:y-1
    P(x,y) = 1;
  end
end
end
```

```
% quadrant 2
% density = 100%;
for x = 1023:-1:1
  for y = pcy:-1:x+1
    P(x,y) = 1;
  end
  for y = pcy:1:2*pcy-x-1
    P(x,y) = 1;
  end
end
end
```

```
% quadrant 3
% density = 66%;
for y = 1023:-1:1
  for x = pcx:-1:y+1
    P(x,y) = 1;
  end
  for x = pcx:1:2*pcx-y-1
    P(x,y) = 1;
  end
end
end
```

```
for y = 1023:-4:1
  for x = pcx-1:-3:y+1
    P(x,y) = 0;
  end
  for x = pcx+1:3:2*pcx-y-1
    P(x,y) = 0;
  end
end
end
```

```

for y = 1022:-2:1
    for x = pcx-2:-3:y+1
        P(x,y) = 0;
    end
    for x = pcx+2:3:2*pcx-y-1
        P(x,y) = 0;
    end
end
for y = 1021:-4:1
    for x = pcx-3:-3:y+1
        P(x,y) = 0;
    end
    for x = pcx+3:3:2*pcx-y-1
        P(x,y) = 0;
    end
end
end

```

```

P = P.*Pw; % generate the resist walls around the trenches
P = P+Tr; % generate the trenches

```

```

clear Tr;
clear Pw;

```

```

% Calculate macroloading parameter

```

```

sumP = sum(P);
sumP = sum(sumP);
Mp = sumP/pi()/5000^2;

```

```

% Computing the convolution of the binary pattern function with the pattern weighting function kernel.
% This is the inverse Fourier transform of the product of the Fourier transforms of the pattern function
% and the weighting function.

```

```

up = ifft2(fft2(P,4096,4096).*fft2(W,4096,4096));
up = up(1024:3071,1024:3071);
up = up.*P; % convert to Si etch rate map for which ERSi = 0 in resist areas

```

```

clear W;
clear P;

```

```

imshow(log(abs(35*up)))

```

```

% Extract the values of the microloading for each trench
density=[0,0.333,0.667,1]; % pattern densities in each quadrant
[md,nd] = size(density);

```

```

% quadrant 1;
for it = 1:nt
    upT1(it) = up(1024,pcx+ax_loc(it)-1);
end

```

```

% quadrant 2;
for it = 1:nt
    upT2(it) = up(pcy-ax_loc(it)+2,1024);
end

```

```

end

% quadrant 3;
for it = 1:nt
    upT3(it) = up(1024, pcx-ax_loc(it)+2);
end

% quadrant 4;
for it = 1:nt
    upT4(it) = up(pcy+ax_loc(it)-1, 1024);
end

upT = [upT1, upT2, upT3, upT4];
clear upT1 upT2 upT3 upT4; %up

% Calculate the surface etchrate at the geometric center of each trench incorporating microloading,
% macroloading and spatial variation

ERC = 37*Mp^2-104*Mp+140; % the etch rate at the center of the wafer
% spatial variation in etch rate
ERs = ERC*((3400*Mp+1340)*(ax_loc*p).^3-60*(ax_loc*p).^2+(ax_loc*p)+1);
ERs = [ERs, ERs, ERs, ERs];

% the surface etch rate at the geometric center of each trench
ER0 = (1-upT).*ERs;

% Compute the etch depth for each trench
% Initialize the ARDE etch terms
% the normalized depth at which the Clausing alpha factor is calculated
for it = 1:Q*nt
    if w(it) <= Tm
        xs(it) = (1+2*Tm/w(it)/log(Tm/w(it)))^(-1);
    else
        xs(it) = 0;
    end
end
end

D = D+Tm; % the initial depth for each trench is the mask thickness

% Clausing alpha factor
aC = (1-2*xs-sqrt((1-xs).^2+(w./D).^2)+sqrt(xs.^2+(w./D).^2))./...
    (2-4*xs-2*sqrt((1-xs).^2+(w./D).^2)+2*sqrt(xs.^2+...
    (w./D).^2)+(1-xs)./sqrt((1-xs).^2+(w./D).^2)-...
    xs./sqrt(xs.^2+(w./D).^2));

% Clausing vacuum conductance correction factor
K = aC.*(1-w.*log((D+sqrt(D.^2+w.^2))./w)./D)-D./w/2+...
    sqrt(D.^2+w.^2)/2./w+w.*log((D+sqrt(D.^2+w.^2))./w)./D/2;

% etch rate at the start of the etch process
ER = ER0./(1+S*(K.^(-1-1)))*1e-9;

```

```

imax=ceil(T/tstep);

for i = 2:imax+1
    time(i,1) = (i-1)*tstep; % time in seconds
    D(i,:) = D(i-1,:) + ER*tstep; % new depth after a time step
    % calculate the etch rate at the new depth
    for it = 1:Q*nt
        if w(it) <= D(i,it)
            xs(it) = (1+2*D(i,it)/w(it)/log(D(i,it)/w(it)))^-1;
        else
            xs(it) = 0;
        end
    end
    end
    aC = (1-2*xs-sqrt((1-xs).^2+(w./D(i,:)).^2)+sqrt(xs.^2+...
        (w./D(i,:)).^2))./(2-4*xs-2*sqrt((1-xs).^2+(w./D(i,:)).^2)+...
        2*sqrt(xs.^2+(w./D(i,:)).^2)+(1-xs)./sqrt((1-xs).^2+...
        (w./D(i,:)).^2)-xs./sqrt(xs.^2+(w./D(i,:)).^2));

    K = aC.*(1-w.*log((D(i,:)+sqrt(D(i,:).^2+w.^2))./w)./D(i,:))-...
        D(i,:)./w/2+sqrt(D(i,:).^2+w.^2)/2./w+w.*log((D(i,:)+...
        sqrt(D(i,:).^2+w.^2))./w)./D(i,:)/2;

    ER = ER0./(1+S*(K.^-1-1))*1e-9;
end

D = (D - Tm)*1e6; % subtract out the mask thickness to obtain depth in Si
Output = [time,D]; % compile a table of depth versus time for each trench

```

---

---

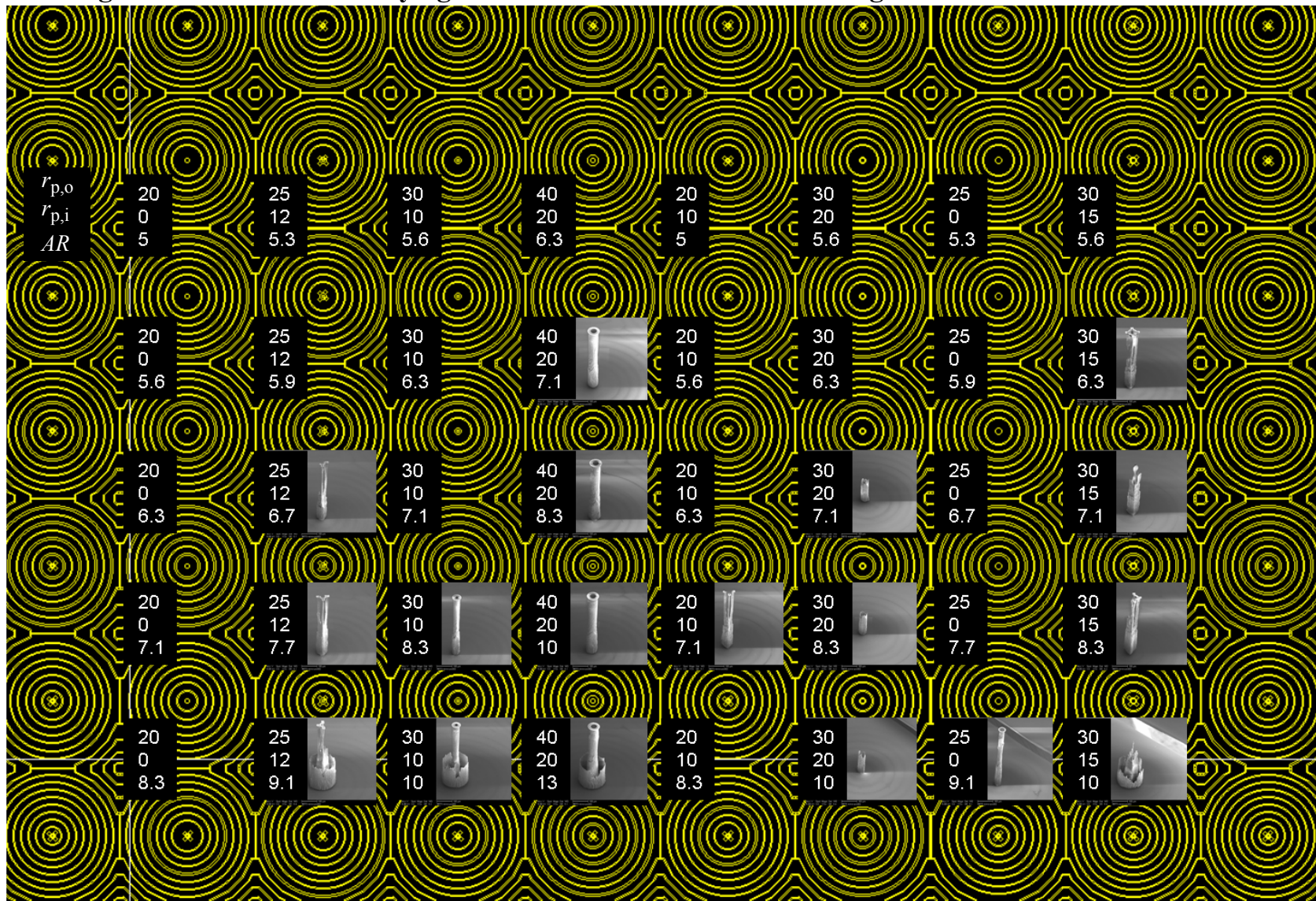
# Appendix E - Post Etch Geometry Study







### E.2 Large Width Posts With Varying Radius of Innermost ARDEM Ring



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