COURSE SYLLABUS

Class:
Mon. & Wed. 12:30 to 2:20, DH 1217

Instructor:
Prof. Andrzej Strojwas
HH 2106; X 8-3530
ajs@ece.cmu.edu
Office hours: Tuesday, 4-6 PM

Course TA’s:

Kartik Murthy
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Office Hours: To be announced

Panchalam Ramanujan
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Course Secretary:
Judy Bandola
HH 2107: X 8-2224
judy@ece.cmu.edu
Office hours: Mon. through Fri. 8:00 AM – 4:30 PM

Course Web Page:
http://www.ece.cmu.edu/~ee525/

Blackboard for on-going discussions
I. PURPOSE

The goal of *Integrated Circuit Design Project* (18-525) is to provide the Electrical and Computer Engineering students with IC design experience. It is an extension of *Analysis and Design of Digital Integrated Circuits* (18-322). **18-525 is aimed at reinforcing the theoretical background and practical skills gained in 18-322.**

The primary stress of the 18-525 class will be on the entire IC design process. Such a process, seen as a sequence of design decisions, must lead to a design, which optimizes a given objective function under a number of constraints. The optimum design must be achieved using a number of variables involving all levels of design abstraction that range from the system architecture choice to the detailed IC layout. Typical design objectives adopted in 18-525 designs will be IC performance (throughput, clock frequency, etc.) and typical constraints will be die size and minimum feature size.

Because of enormous complexity of modern IC’s, actual VLSI design processes must be performed by very large design teams. Efficiency of such teams, as well as quality of the resulting designs, is very strongly dependent on the team members’ communication skills. Such skills are necessary as a key ingredient in any collective design decision-making process. For this reason, the second most important objective of 18-525 is to mimic a large design team environment in which individual designers must: (a) communicate precisely and efficiently his/her ideas and (b) utilize any feedback provided by the “design organization”. This objective will be achieved through in-class presentations given by each student and by stressing the importance of design documentation.

Such an organization is typical for a *fabless company*, which has to design the products given the IC fabrication process capability as provided by the *foundries*. The interface between these two organizations is typically specified in the form of *Layout Design Rules*, *SPICE files* (including worst case conditions) and the available *Standard Cell Libraries*.

II. ORGANIZATION

The students in the class will form **three to four** person design teams. Members of the team will have to collaborate all semester by **evenly** sharing the design and presentation loads. Each team will have to design a single complete IC, produce design documentation and 12 class presentations. Each team will be assigned a Design Manager (one of the TA’s) who will be closely interacting with the team. Each student will send **weekly status report** of what they have accomplished **individually** over the last week via e-mail to the instructor and her/his Design Manager. This report is due before Monday class.

There will be no lectures, exams or formal homeworks. The main workload will be related to the design process itself and class presentations/discussions. Class presentations will be used also as a main mechanism reinforcing correct scheduling of main design milestones, as well as a forum to obtain design advice and the approval of the proposed design strategy.
III. PRESENTATIONS

Project presentations are the key element of the class. Each design team will have to prepare 12 presentations. The goals of class presentations are as follows:

a. Create a discussion forum that enables the design decision-making process for all projects in the class.

b. Provide a feedback and constructive critique for each design team.

c. Assess progress of each design project.

d. Help each team to see both progress and quality of their designs in a broader perspective.

Three or four presentations will be given by each student in front of the class. Each presentation will have to take 15 - 20 minutes with approximately 7 to 8 slides. Dates of all presentations will be decided at the beginning of the semester (second class of the first week of classes).

Each presentation will have to include the following mandatory slides:

1. Title slide with all three-four students names in alphabetical order, title of the project, description of the overall project objective and description of the “design stage objective” discussed in the presentation.

2. The “project status slide” (what was done and what must be done next.)

3. The “assumption slide” listing all the assumptions/constraints used in the decision making process.

4. The “design decision slide” listing all the decisions made since last presentation.

5. The “result slides” illustrating results obtained since last presentation.

Presentations will have to be prepared using Microsoft PowerPoint by the presenter or other group member. We will provide a laptop projection capability. A hardcopy of your presentation may be given to the Course Secretary by 9:30 AM the day of the presentation or may be provided by the presenter. Four paper copies of the presentation must be available before each presentation.
## IV. CLASS SCHEDULE

<table>
<thead>
<tr>
<th>Week</th>
<th>DATE</th>
<th>SUBJECT</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>27 Aug. M</td>
<td><em>Course Objectives and Overview</em></td>
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<tr>
<td>1</td>
<td>29 Aug. W</td>
<td><em>Design Team Formation</em></td>
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<tr>
<td>2</td>
<td>3 Sept. M</td>
<td><em>Labor Day – no class</em></td>
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<td>2</td>
<td>5 Sept. W</td>
<td>Design Ideas Review</td>
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<td>3</td>
<td>12 Sept. W</td>
<td>Design proposals</td>
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<tr>
<td>4</td>
<td>17 Sept. M</td>
<td>Proposed chip architecture (Functional level design)</td>
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<td>4</td>
<td>19 Sept. W</td>
<td><em>Chip architecture refinement discussions</em></td>
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<tr>
<td>5</td>
<td>24 Sept. M</td>
<td>Size estimates/Floorplan</td>
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<tr>
<td>5</td>
<td>26 Sept. W</td>
<td><em>Size estimates/Floorplan Discussions</em></td>
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<tr>
<td>6</td>
<td>1 Oct. M</td>
<td><em>Structural Design &amp; Gate level design discussions</em></td>
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<tr>
<td>6</td>
<td>3 Oct. W</td>
<td><em>Structural Design &amp; Gate level design discussions</em></td>
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<tr>
<td>7</td>
<td>8 Oct. M</td>
<td>Structural design</td>
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<td>7</td>
<td>10 Oct. W</td>
<td>Structural design verification</td>
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<td>8</td>
<td>15 Oct. M</td>
<td>Gate Level Design</td>
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<td>8</td>
<td>17 Oct. W</td>
<td>Gate Level Design Verification</td>
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<td>9</td>
<td>22 Oct. M</td>
<td><em>Component Layout Design</em></td>
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<td>9</td>
<td>24 Oct. W</td>
<td>Component layout &amp; Post-Layout Simulations</td>
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<td>10</td>
<td>29 Oct. M</td>
<td>Functional block layout design</td>
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<td>10</td>
<td>31 Oct. W</td>
<td>Functional block post layout simulation</td>
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<td>11</td>
<td>5 Nov. M</td>
<td>Chip-level layout design</td>
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<td>11</td>
<td>7 Nov. W</td>
<td><em>Chip-level layout design discussion</em></td>
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<tr>
<td>12</td>
<td>12 Nov. M</td>
<td>Design corrections/optimization</td>
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<td>12</td>
<td>14 Nov. W</td>
<td><em>Final design improvements</em></td>
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<tr>
<td>13</td>
<td>19 Nov. M</td>
<td><em>Short presentation preparation</em></td>
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<td>13</td>
<td>21 Nov. W</td>
<td><em>No Class. Thanksgiving Break</em></td>
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<tr>
<td>14</td>
<td>26 Nov. M</td>
<td><em>Short presentation preparation</em></td>
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<tr>
<td>14</td>
<td>28 Nov. W</td>
<td><em>Full final presentation preparation</em></td>
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<tr>
<td>15</td>
<td>3 Dec. M</td>
<td>Full final presentations.</td>
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V. DEADLINES

Final layout design databases are due one day before final project presentation. The design will be accepted if:

a. Final project presentation is successful.

b. LVS & Circuit Simulations are successful.

c. Final documentation is submitted to the course instructor.
VI. GRADING

There will be no homeworks or exams in the class. Final class grade will be given using the following weights:

**Design project**
- Design functionality: 400 p.
- Design quality:
  - (density, performance, etc.): 200 p.
- Individual contribution to the project (based on weekly status Reports): 100 p.

**Communication**
- Average of class presentations:
  - Team grade: 100 p.
  - Presenter: 50 p.
- Quality of final documentation: 100 p.
- Constructive contributions during class discussions: 50 p.
- Invested shares*: 100 p.

There will be an extra credit (up to 100 p.) given for the high-quality and/or highly innovative designs. Additional 50 p. extra credit may be given for a few of the best final project presentations.

Please note that we have an extremely aggressive project schedule. Missing any of the milestones puts the project success in jeopardy. To enforce the timeliness, there will be up to 20 p. penalty for missing any milestone. So if you fall behind, you will have to quickly make up the delay to avoid accumulation of penalties.

Class attendance and active participation are essential to the success of this course. If you cannot make the class, you must notify your Design Manager (TA) who will be keeping track of your attendance record. There will be a penalty of up to 100 points for missing more than 3 classes. On top of the 20 p. for active participation in class discussions, there will be up to 80 p extra credit given to the top 5 students who made the most constructive contribution to the in-class discussions.

* Each student in the class is given “shares” which he or she can invest in any design in the class. This 100 p. credit is given at the end of the class to each student who has chosen a design (who has invested given shares in a design) that is given a full credit for functionality and quality. Three design teams with the largest numbers of accumulated shares will be given 100 p. of extra credit. All shares must be invested before March 26th.
VII. REFERENCE BOOK


VIII. PREREQUISITE

Design of Digital Integrated Circuits (18-322) AND (18-340 or 18-341 or 18-321 or 18-310 or 18-450 or 18-491 or 18-415)