18-360
Intro to Computer-Aided Digital Design
ECE Department

Carnegie Mellon

Course Syllabus Spring 2004

Overview

The design of digital integrated circuits (ICs) has grown in complexity to where computer-aided design tools are required for designers to work in an economically productive manner. This course introduces the techniques of modeling digital systems at various levels of abstraction, and computer-aided design (CAD) algorithms that are applied to these models to support design and analysis tasks. The course covers modeling through the use of a modern hardware description language (Verilog). The language is used to model an IC in the early stages of design using behavioral modeling techniques and in later stages using structural modeling techniques. This is not a "how-to" course on using CAD tools. Rather it is a study of the algorithms used by CAD tools and the design methodologies they promote. The course will cover: modeling of digital systems for debugging, simulation and synthesis using Verilog; test generation — which is used to determine if a manufactured design is correct; event-driven simulation algorithms, and physical design — which is used to map the synthesized logic design onto physical IC area.

This year the course will have added emphasis on modeling for mixed hardware and software systems. We will look at the current languages in use today (e.g., Verilog and C) and understand how these can/cannot be used together to model systems.

Course Staffing

Instructor: Prof. Donald E. Thomas
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Course Admin: Jacqueline Chraska,
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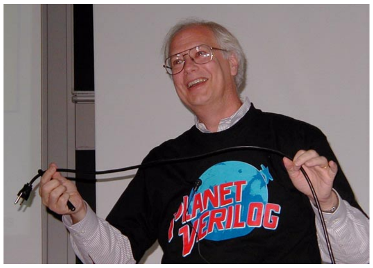

The day Professor Thomas unplugged Wean Hall — *zra*

TAs:		
	James Ma	jdma@ece.cmu.edu
	Peter Milder	pam@andrew.cmu.edu

Office Hours: These will be arranged soon. You can always make an appointment. Call or send e-mail.

Class lecture time and place: TR 10:30 — 11:50, BH-A51, near the produce aisle.

For those with webbed feet

Course assignments will be available on the web. If you don't pick them up in class, print them out or view them directly. See the course home page (http://www.ece.cmu.edu/afs/ece/class/ee360/). A course bboard will also be set up for the class. Check "cmu.ece.class.ee360" for announcements, assignment corrections, hints, and updates on The Young and the Restless (the soap you miss by attending class).

Prereq's

18-240, 15-211. This is a course about computer-aided design algorithms for digital system design. Having 18-240 as a prerequisite insures that everyone in the class will have a basic idea of what it is that we're trying to aid. 15-211 serves as a skill prerequisite. During the course we'll probably hand out an assignment or two that will require 1000 lines of C or Verilog code, involving non-trivial data structures and a fair amount of interaction with other people's code. You need to know more than how to print "hello, world\n"

Textbooks

There really is no one textbook that covers the material for this course at a Junior level — or any other level for that matter. The one book listed below is required although you probably have it from 18-240. One of the topics in the course is hardware modeling and we will use the Verilog language as a means for doing that. I'll have several readings and books on reserve at the library.

The Verilog Hardware Description Language, Fifth Edition, Thomas and Moorby.

Grading

Grading will be based on homeworks, tests (including a final exam), and projects. The *approximate* weightings will be homeworks — 25%, tests — 50%, and projects — 25%. Both projects must be completed or an incomplete (I) grade will be given.

Homeworks

There will be seven or eight homework assignments distributed over the semester. The goal of these will be to give you problems to exercise your knowledge of the lecture material and to prepare you for the tests. We will drop one homework score.

Policy: Homeworks are due at the beginning of class. During the class, solutions will be handed out and we will discuss them at the beginning of class. No late homework. We will drop the lowest homework score for final grading.

Tests

There will be three tests and a final exam.

Projects

Mud wrestling is fun to watch but you don't really understand it until you jump in. The same can be said about CAD. The algorithms and methods that we present in class will (hopefully) be interesting to study. But some of the real engineering problems don't come to life until you try to implement them or apply them in a more-real-life situation. There will be two projects which will involve the coding of an algorithm discussed in class and/or a sizable Verilog description. Details of these will follow. Groups of two are typically encouraged. For at least one of these, you will be expected to make a short presentation to the class on the results of your project. Both projects must be completed to receive a grade in the course; otherwise an incomplete (I) will be given.

General Grading Policies

If we added up your scores incorrectly, tell us immediately. If you think you were misgraded, you have one week from the time the assignment or test is handed back to argue for the grade change. After that, no dice. Implication? We will be totally unsympathetic to someone whining about a grade change on homework 1 on the day after you see your final grade.

There is no extra credit. However, I will take note of people who do an extra spectacular job on a project. It might help you at final grading time.

The gradebook will be available for you to see from the web page. You can get your scores emailed to you. The purpose of making this information available to you is two-fold:

- First, it serves as a check on our database. Did we enter your score correctly? If we didn't, bring your assignment back in and we'll correct our entry.
- Secondly, it gives you an idea of how you're doing with respect to the rest of the class.

We will try to keep the course on a 90-80-70 straight scale. I realize that this assumes that all the questions are calibrated and the grading is perfect. (Well, of course, the grading is always perfect!) So, there will be some curving done. The point is that I'll try to keep the course on a straight scale so that you are competing with the scale, and not with your fellow students.

Mid term grades will be determined by the total points obtained on the assignments graded at that time. Your grade will only be a rough indicator of where you stand. No homeworks will be dropped, no special considerations will be given, etc. Final grades will be determined by the total points after the lowest homework is dropped. At that point, I'll look for special considerations like "you blew one test", "your tests got better over the semester", or "you did a spectacular job on a project". In such cases, if you are close to a grade break, you might get the higher grade.

Cheating

Read the University Policy about Cheating and Plagiarism's lips: — It shall be the policy in this course to discourage cheating as much as possible, rather than to try to trap and punish. On the other hand, in fairness to all concerned, cheating and plagiarism will be treated severely whenever found. Because a large part of the learning experience comes from interaction with your peers, students are encouraged to discuss assignments with each other. The material handed in for grading must, however, be the product of individual effort; anything else constitutes cheating.

Study Groups

…are a good idea. In the real world, engineers design things in teams, bounce ideas off their colleagues, ask others for clarifications, and interact frequently with their peers. A study group can give you a forum to describe your problems, get alternate perspectives on the course material, and probably discover that you are not the only one having trouble with some difficult concept from the course.

But as mentioned above under cheating, there is a difference between talking about course topics with your group and stealing someone else's solution to an assignment. Talk with your group about ideas, methods, approaches, and practice problems; do your own assignments. I've observed that those who do their own assignments are the ones who get the best grades on exams.

A few practical points:

- Protect your work from being copied; it is difficult to determine who copied from whom. Pick up all you printouts from a public printer. Shield your work from others during an exam.
- Homework problems are meant to represent your own work. The course staff recognizes that homeworks are often done in groups, and we recognize that this approach can help you learn. But it only helps you learn if you, individually, do the problem. Hints from others are of great help. Solutions from others leads to cheating.
- Lab projects in this course are the work of an individual or group of two people (see assignment for details). If your partner copies from another group, even without your knowledge, you are a party to cheating. Know what's being handed in.
- When you hand in assignments that ask for Verilog simulations, the Cadence Verilog simulator should be used and your printouts should clearly identify you as the user and your file being executed/printed.

Course Topics

The main topics of the course will be taken from these three categories. However, the professor has been known to add a few topics if interest warrants.

Debugging, Modeling and Simulation. Gate and behavioral modeling, synthesizable models, the internals of a simulator, cycle accurate simulation, hardware acceleration and emulation, hardware/software simulation, Why isn't C++ good enough — who needs Verilog anyway? Any better languages coming along?

Physical Design. Partitioning, placement, and routing. Kernighan & Linn, Min-cut, wirelength models, annealing and force-directed placement, graph theoretical models of routing. Annealing a jar of peanuts.

Test. Fault models, line justification and fault activation, redundant circuits, the D and Podem algorithms, fault simulation.

Tentative assignment due dates:

- Tests (*tentatively* 2/19, 3/18, 4/22)
- Project 1 due mid to late March (we may change that with Spring break so early) — Project 2 due last week of class
- Homeworks due (tentatively): Approx every two weeks