18-360
Intro to Computer-Aided Digital Design
ECE Department

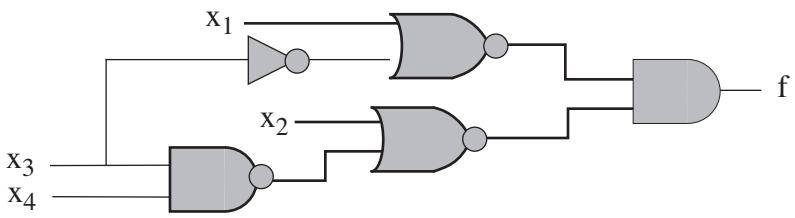
Carnegie Mellon

Out: 2/26/04 Homework 4 Due: 3/4/04

We'll discuss the solutions to these problems at the beginning of class on the due date. Bring your solutions then. Solutions will be handed out, so we can't accept late assignments.

1. Find a test for … 20%

Use the methods shown in the first lecture to find tests for these faults. Redraw the circuit for each of these situations and label it with D notation as well as the values in the circuit that are propagated from the input values selected.

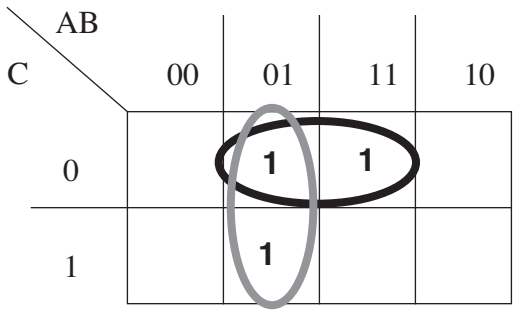


a. x3 SA1 (stem)

b. Now remove the inverter and do x3 SA1 — Hmm, there's a problem! Explain.

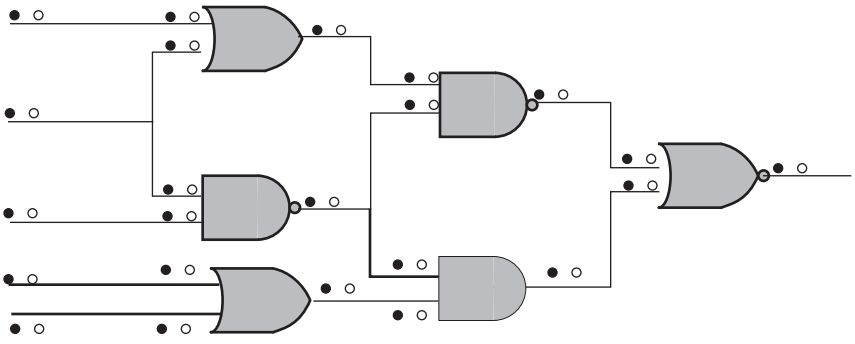
2. Redundant? 15%

So, here's a KMAP for a circuit, much like the one we showed in class. Is this a redundant circuit? If so, what is the redundancy and what part of the circuit is not testable? Explain.



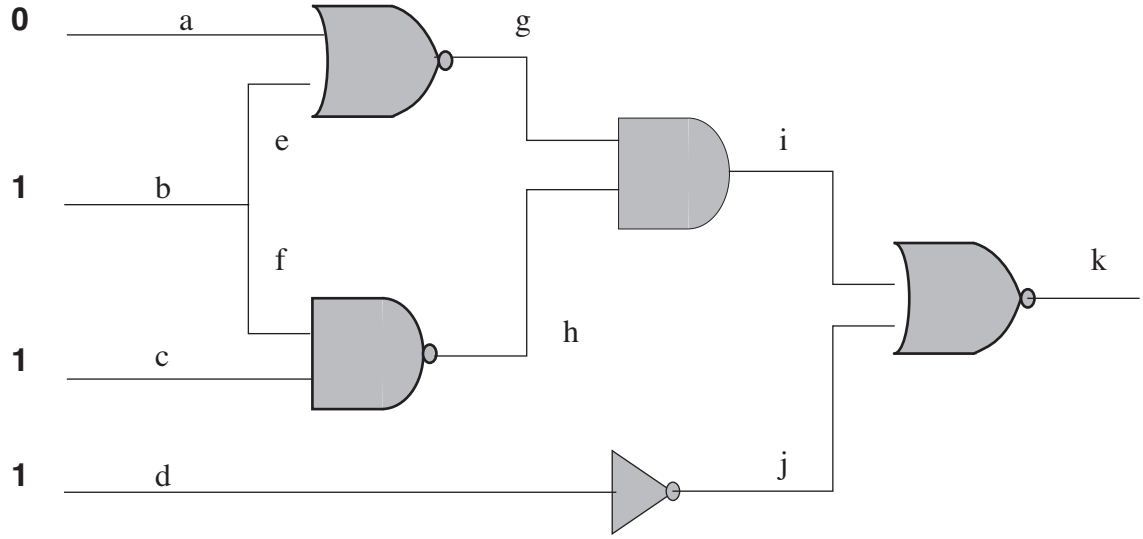
3. From Here to There 15%

The following circuit shows all of the SSFs for each of the gates and branches. Use the methods shown in class to produce the collapsed fault set. Do functional equivalence first, dominance second, and structural equivalence third.



4. Deductive fault simulation 25%

Use deductive fault simulation to determine all of the faults found by the test 0111 in the circuit below. Show the list of visible faults for each node. For each node beyond the inputs, show the equations used to find the list. What faults are finally detected at the output?



5. Find them all 25%

For the circuit in problem 4, come up with a minimal test set to test *all* SSFs in the circuit (figure out problem 3 before doing this one!). The test set does not need to be the absolute minimum, but don't turn in a test set containing 32 vectors either. For the two tests on input a, list the functionally equivalent faults that are found.