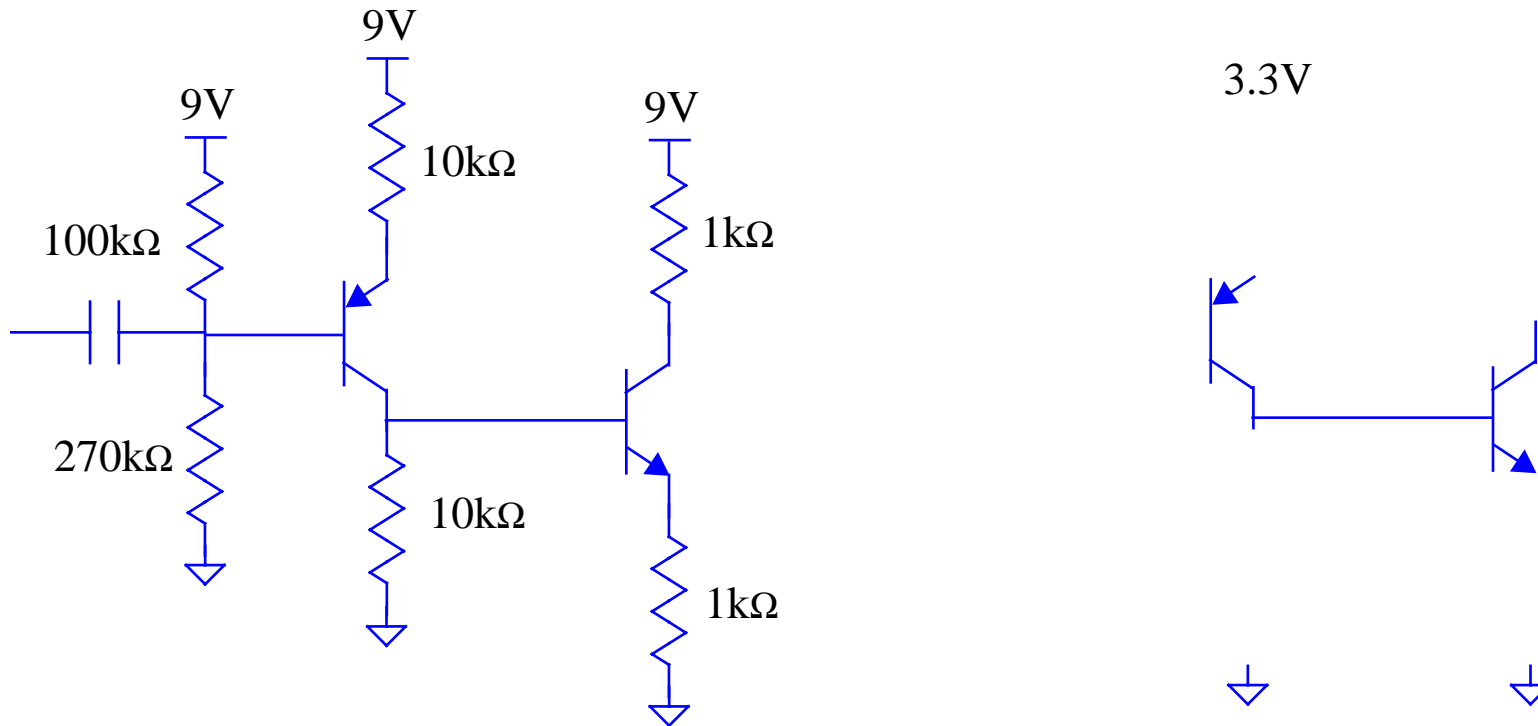


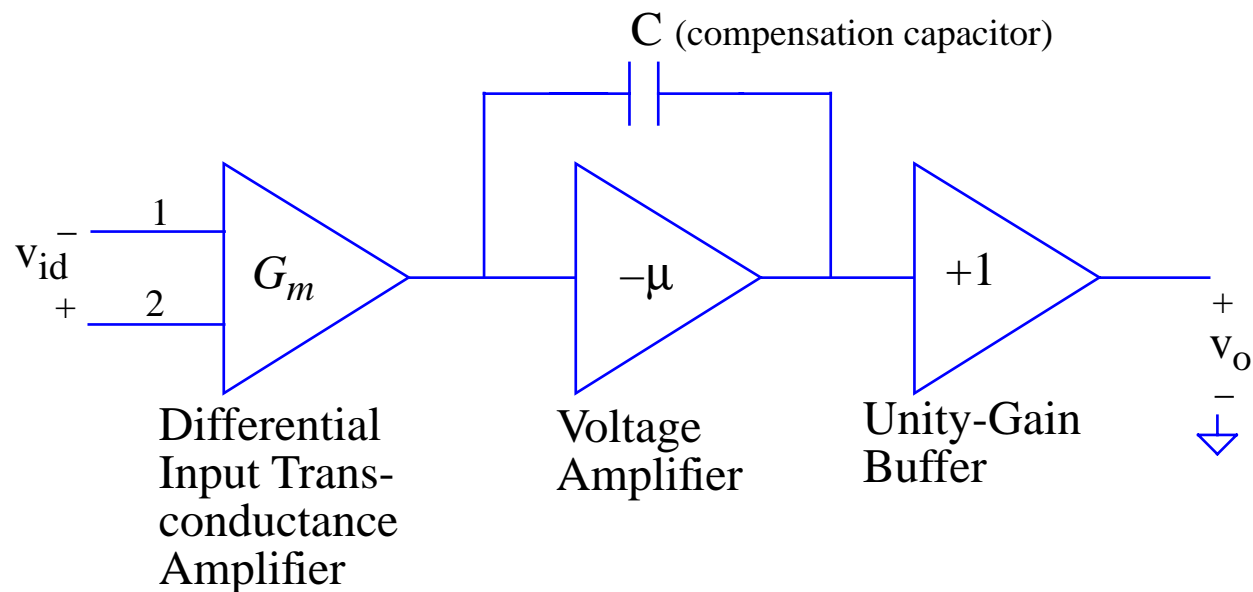
IC implementations

- So far, we talked mostly about discrete circuits...
- In IC:
 - Very rare use of capacitors, inductors practically never (only in some RF circuits)
 - - you typically do not have resistors $>$ several K Ohm,
 - - the larger resistance, the more expensive it is,
 - - a resistor is much more expensive than a bunch of transistors!



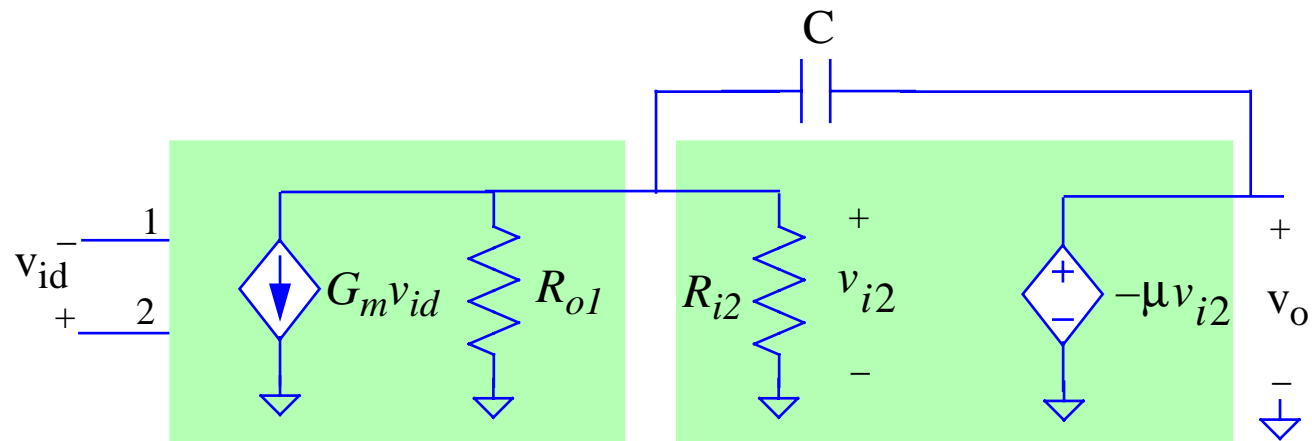
Opamps

- Previously we looked at the **block-level** internal structure of an operational amplifier
- We are now starting to look at the transistor level implementations of these blocks
- What sort of amplifier circuits would you propose for the blocks below based on what you've seen so far?



Opamps

- We macromodeled these blocks in the following way:



- What do the R's represent?

IC implementations

- There is one more thing you have when you design IC:

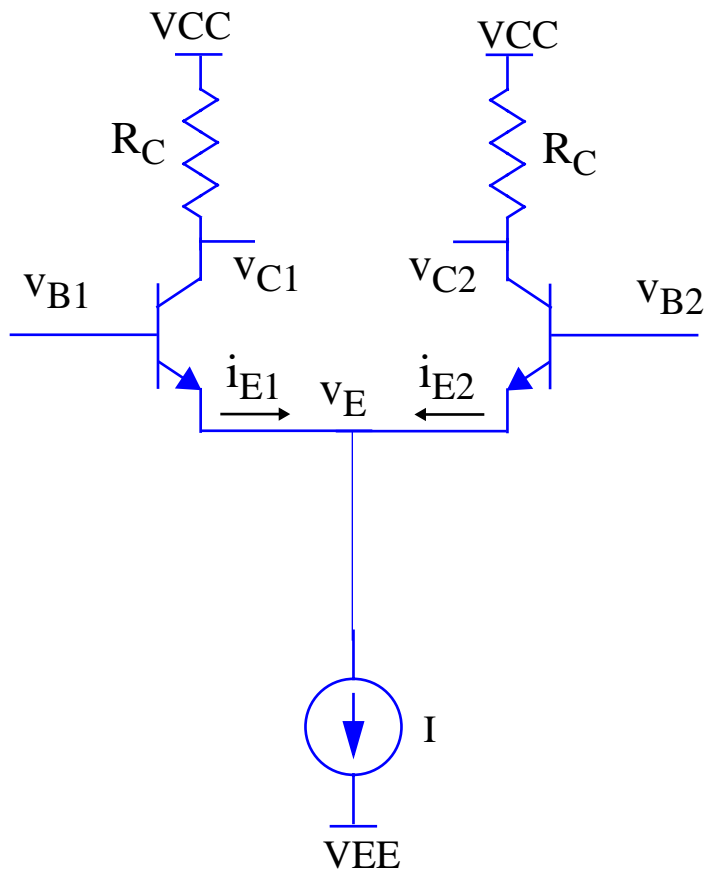
Device Matching

For example:

- electrical parameters of device 0.1 %
 - temperature of operation of many devices can be almost the same.
- This would be to some extent possible, but veeeeeeeeeeeeery expensive in discrete design

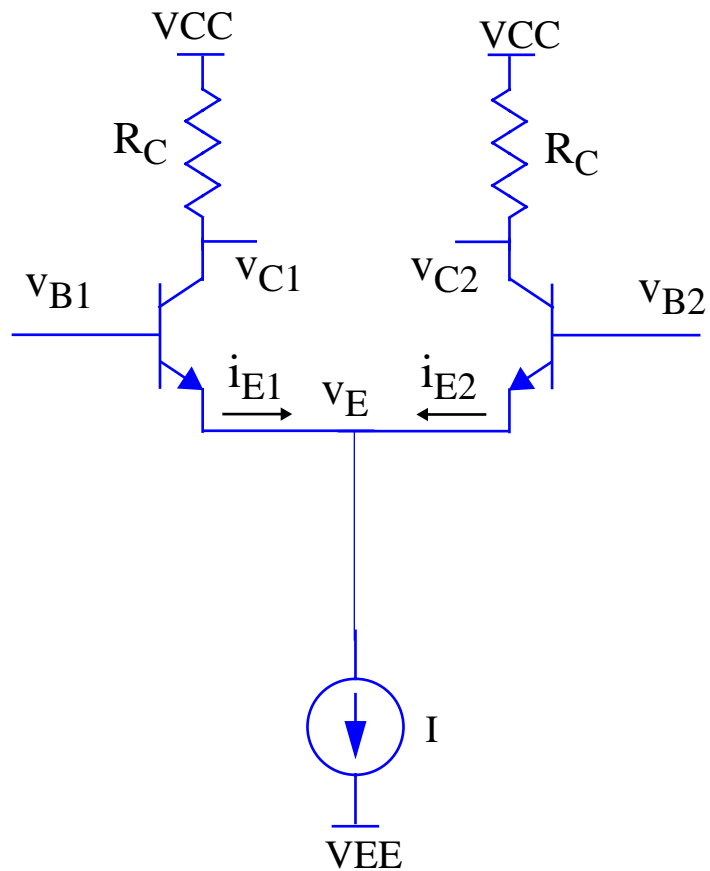
Basic Differential Amplifier

- Emitter voltage becomes whatever value is necessary so that forward active transistor currents sum to current source value, I



Basic Differential Amplifier

- You can express input signal in more convenient terms:



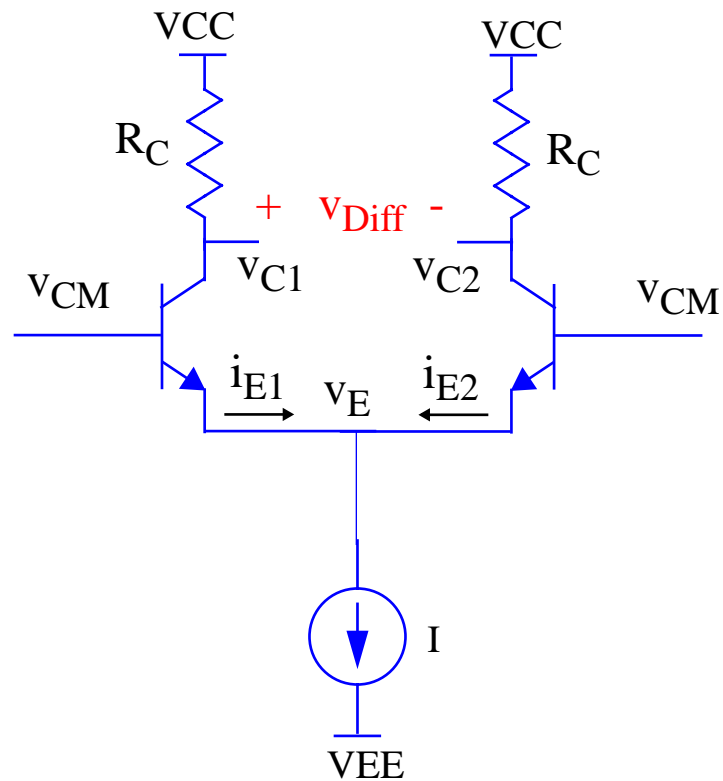
common mode signal:

differential mode signal:

then:

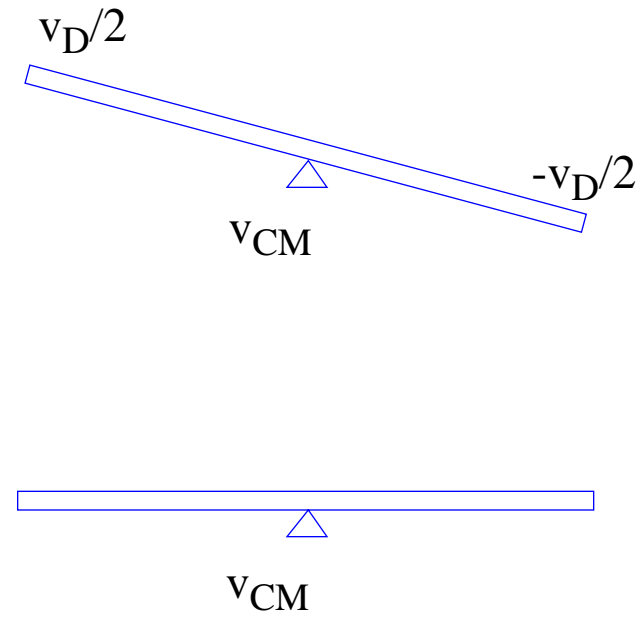
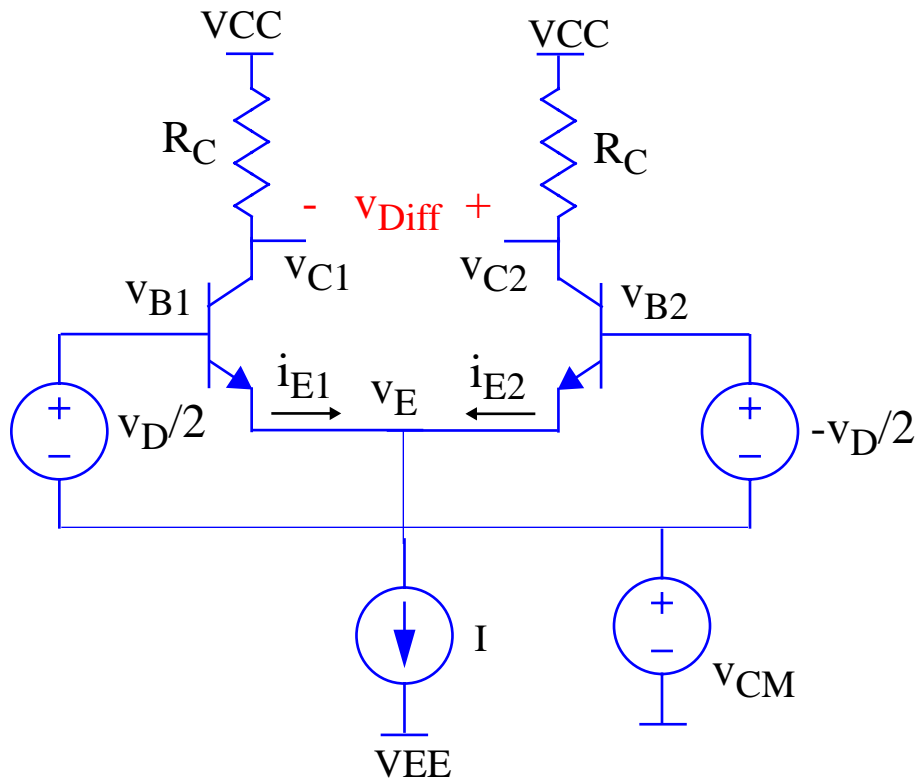
Basic Differential Amplifier

- Differential output rejects **common mode** inputs



Differential Amplifier: Qualitative View (1)

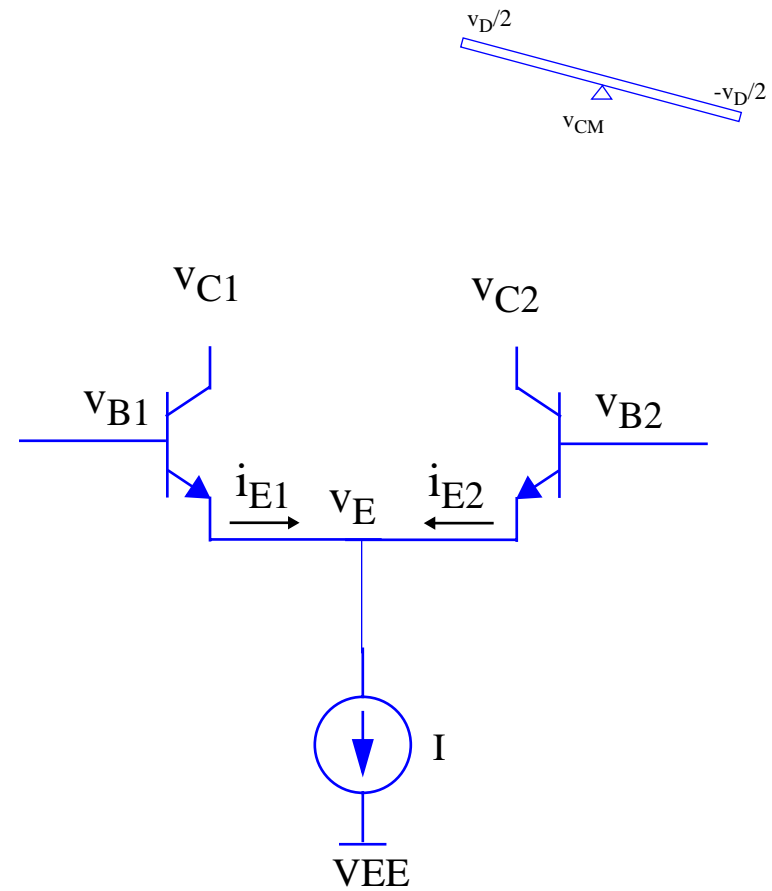
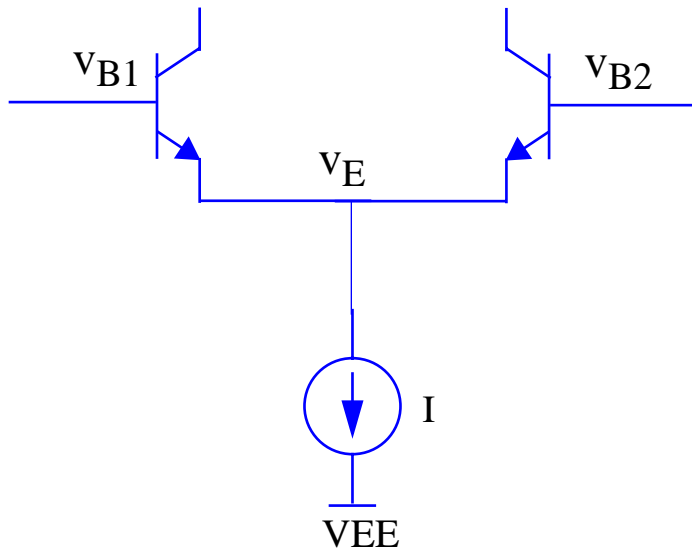
- Think about seesaw...



- Is v_E constant for a given value of v_{CM} and varying v_D ?

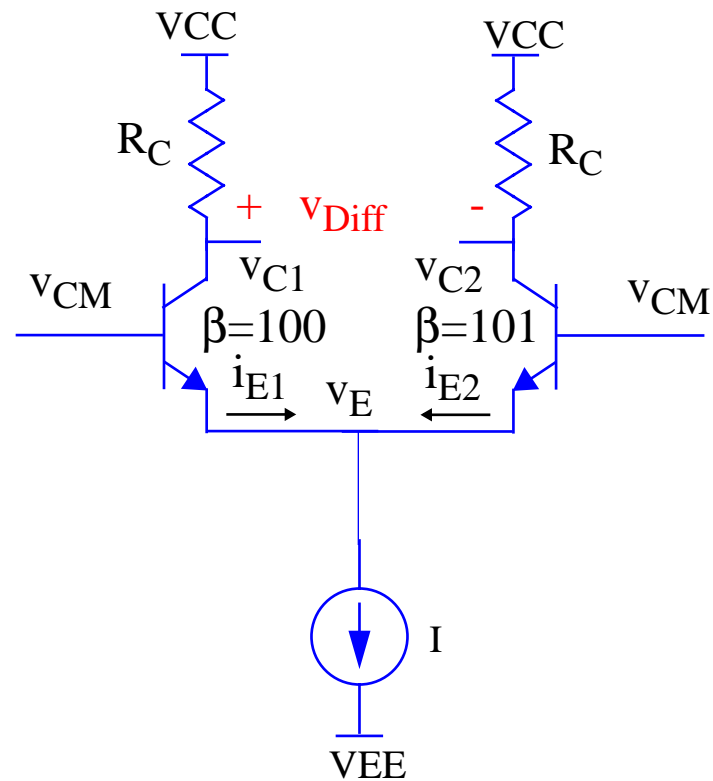
Differential Amplifier: Qualitative View(2)

- Is v_E **constant** for a given value of v_{CM} and varying v_D ?

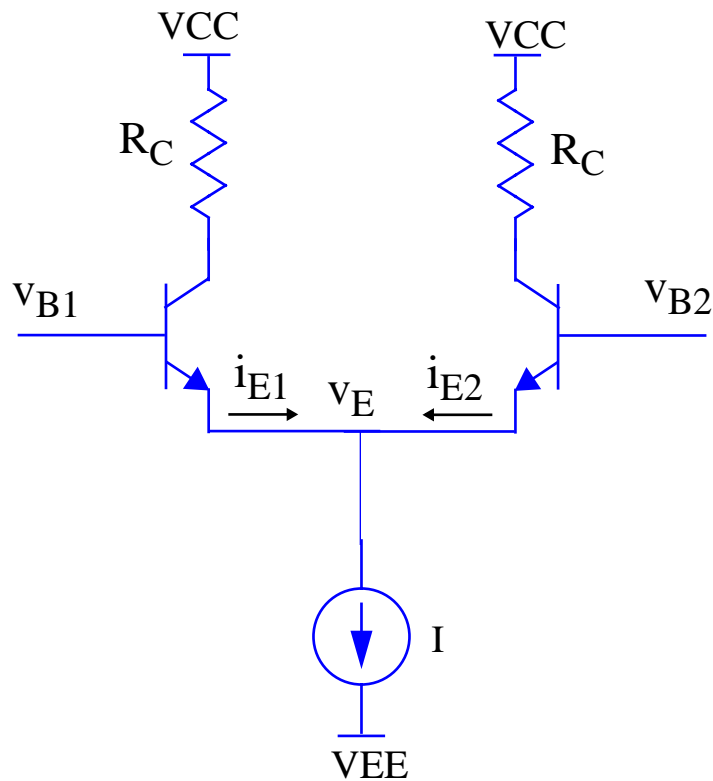


Mismatch of elements

- Differential output rejects **common mode** inputs, but what if T1 and T2 are not identical or “ R_c in not identical to R_c ”?



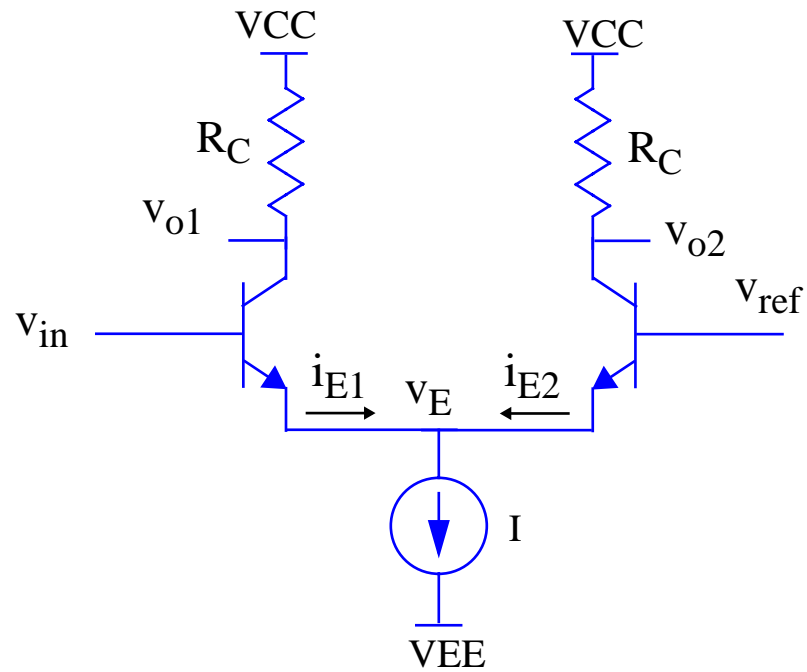
What if we have only single ended output?



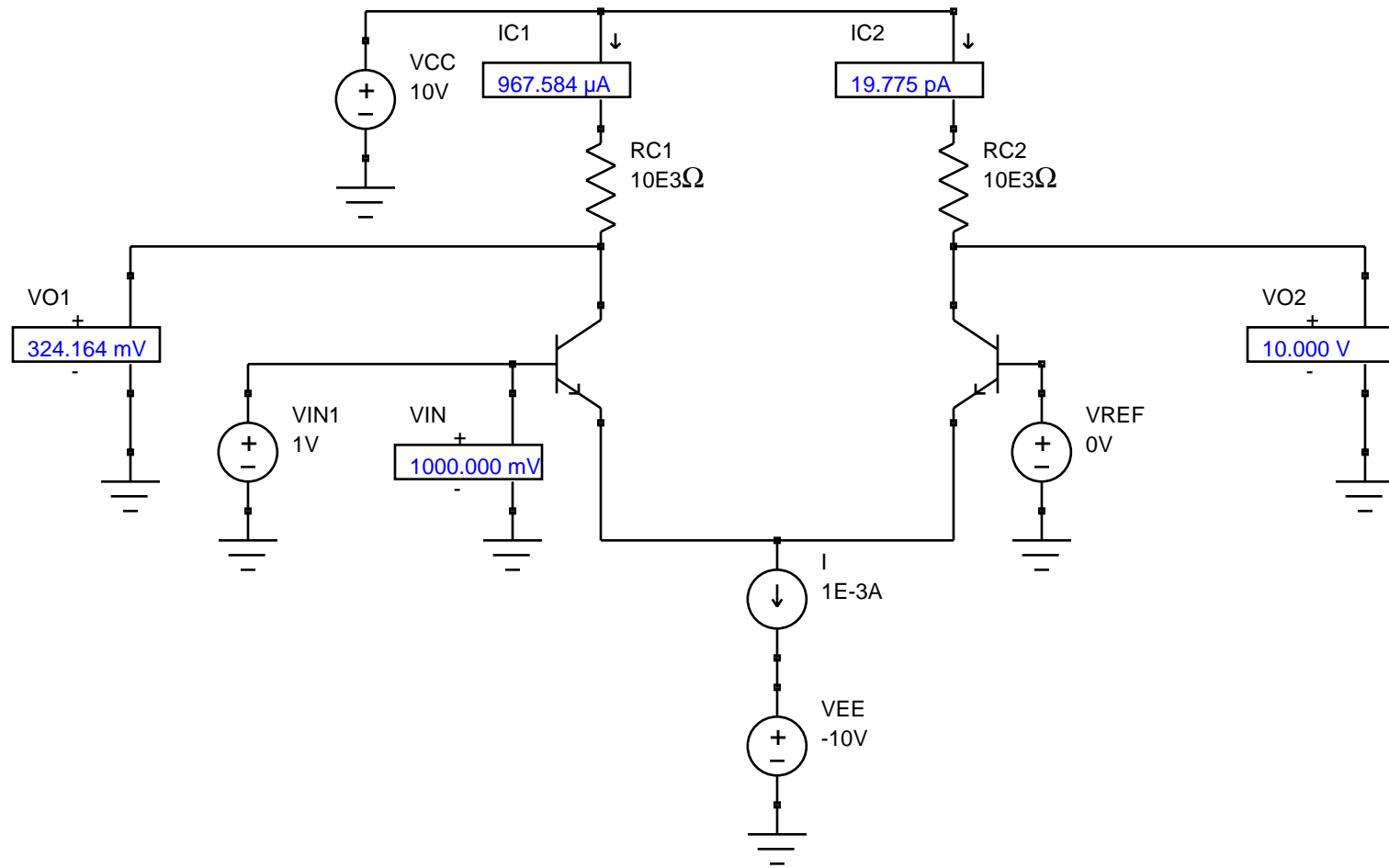
- Using transistors as loads we can do some tricks not to lose gain for asymmetric output - you will see this later.

ECL

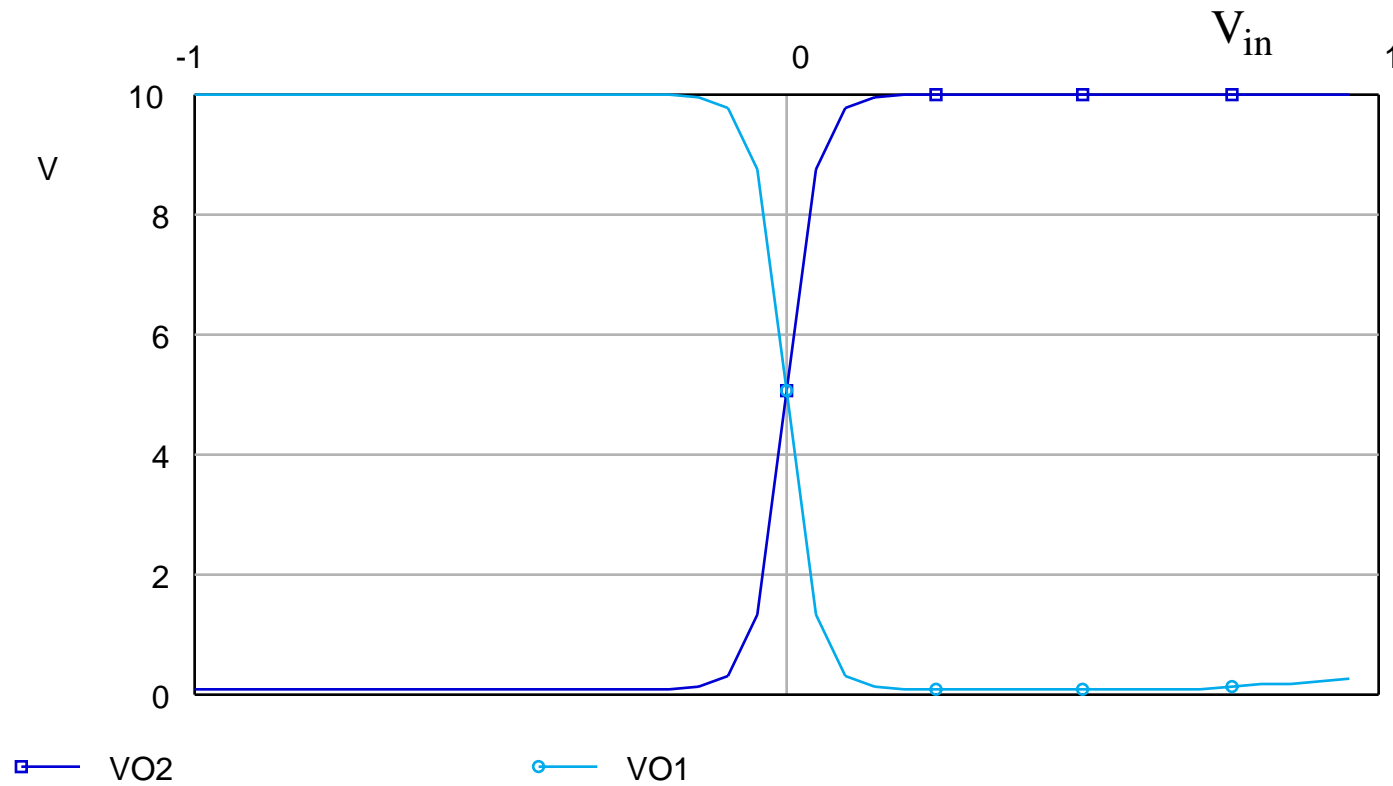
- Basic component of an emitter-coupled logic (ECL) gate



Switch Example

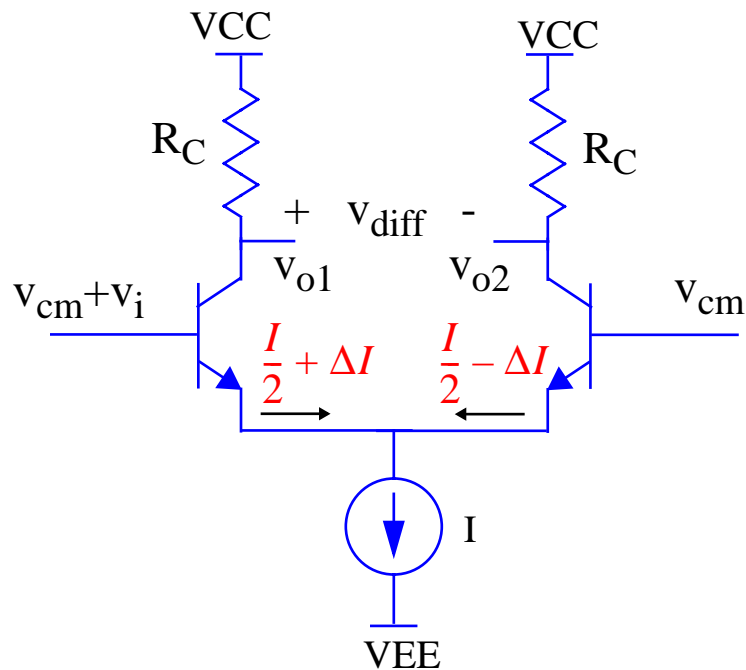


dc Characteristic



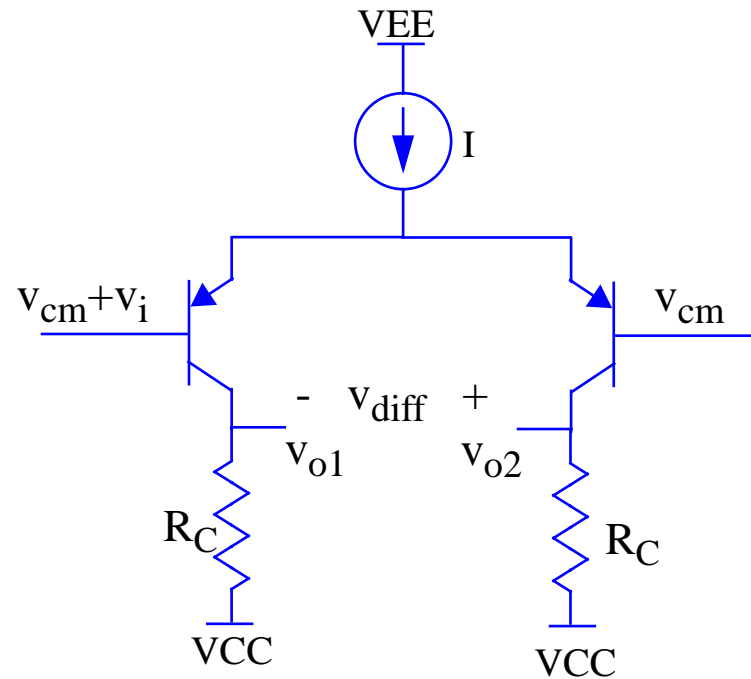
Small Signal Differential Amplifier

- For analog applications we use the differential amplifier in a small signal sense



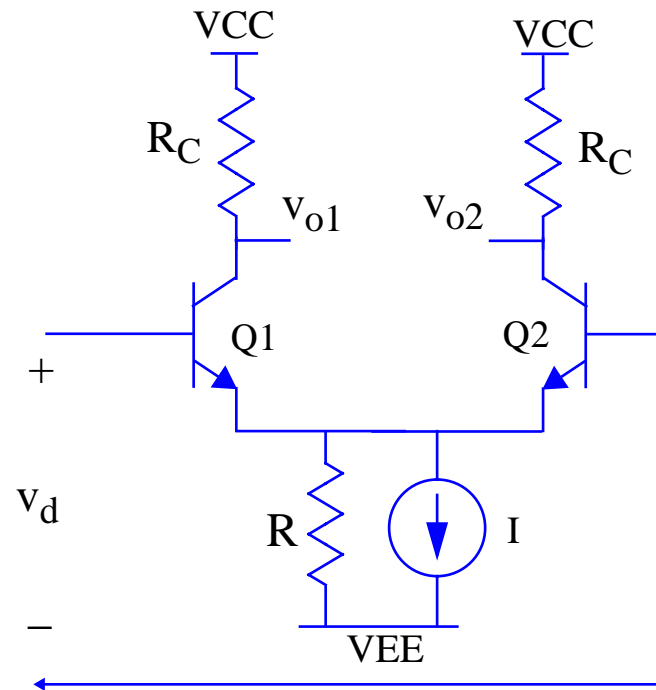
PNP Differential Amplifier

- Works the same way, but VEE is more positive than VCC



Small Signal Differential Amplifier

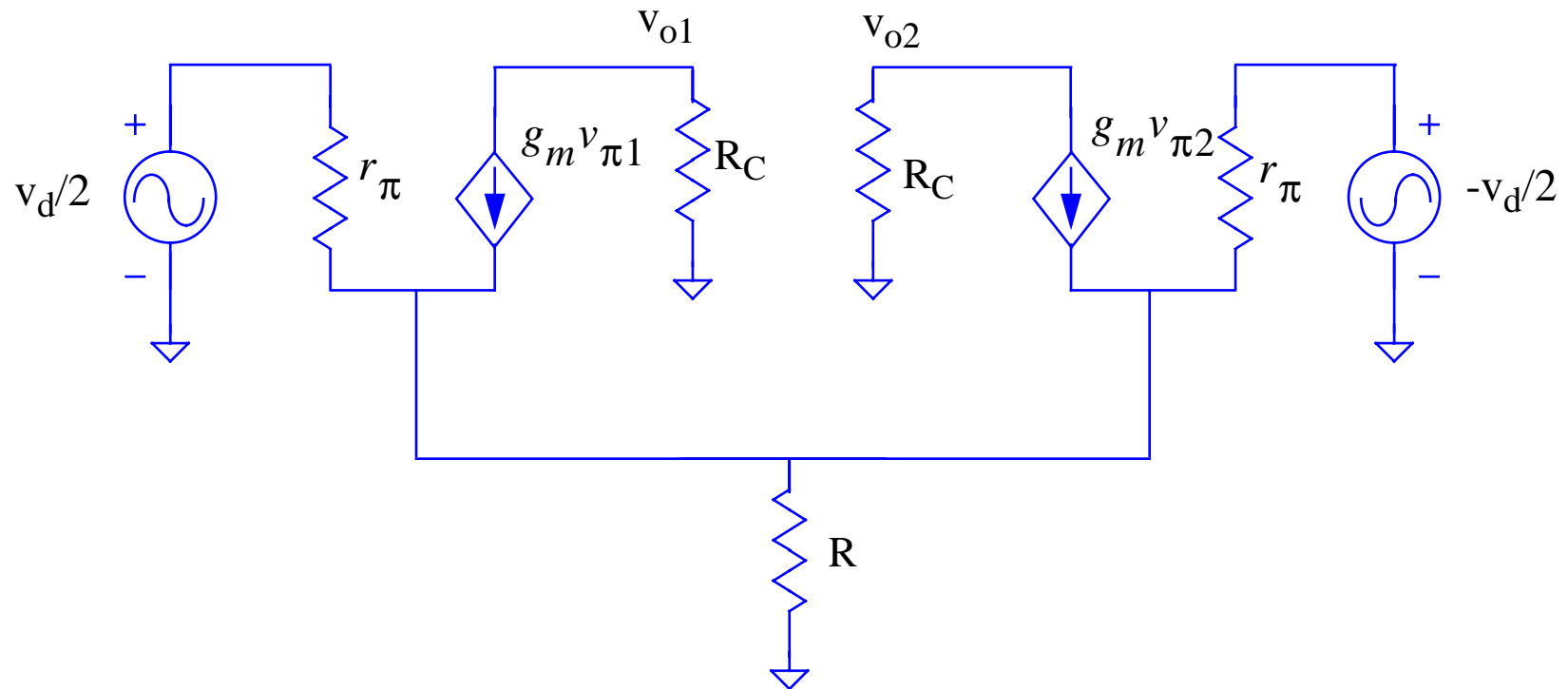
- Assume that the common mode signal has been used for biasing and the input is a small signal differential input



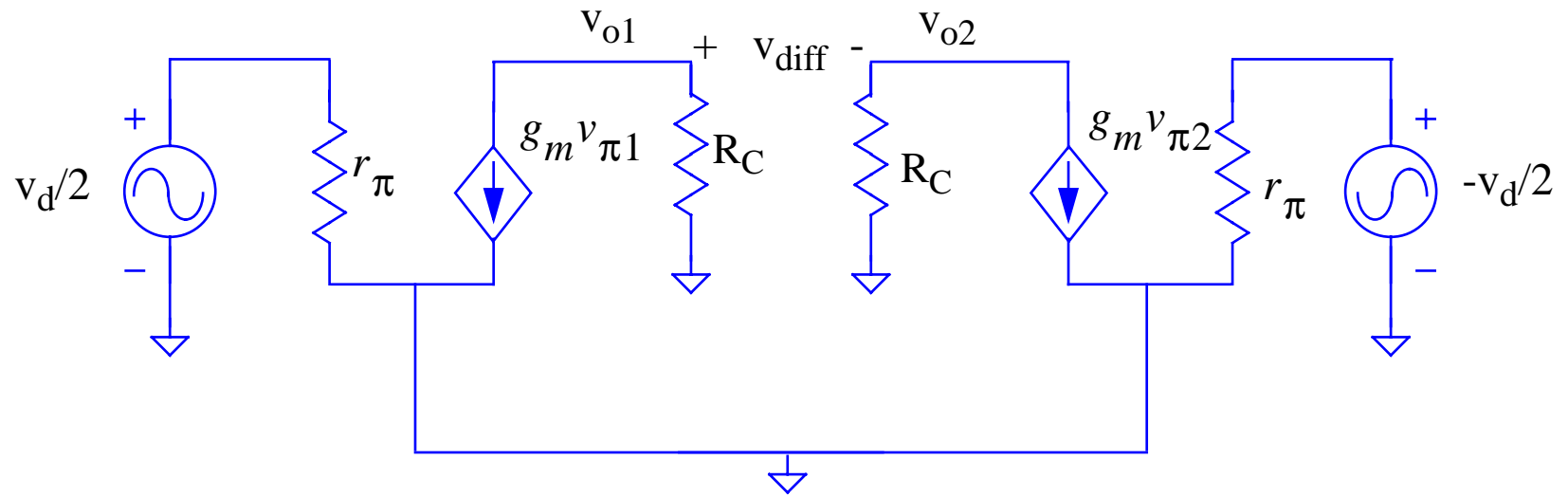
What is the added resistor modeling?

Small Signal Model of Diff Amp

- Establish small signal model the same way as we did for other amplifiers
- Fabricated very carefully for **perfect matching** of parameters

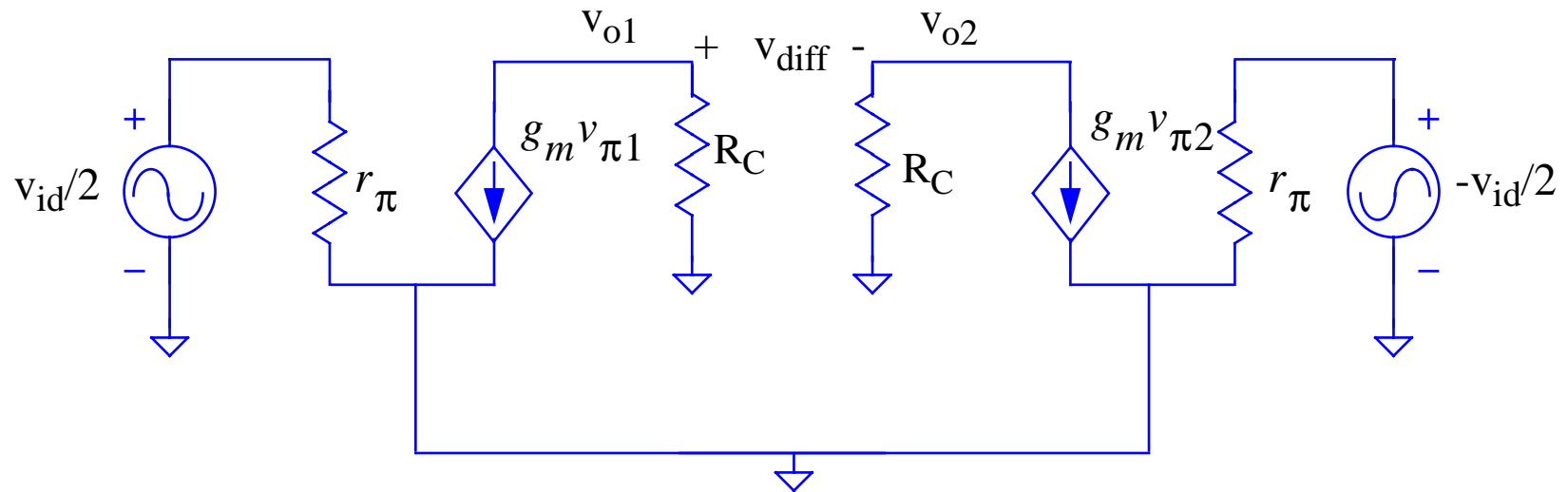


Calculate Gain



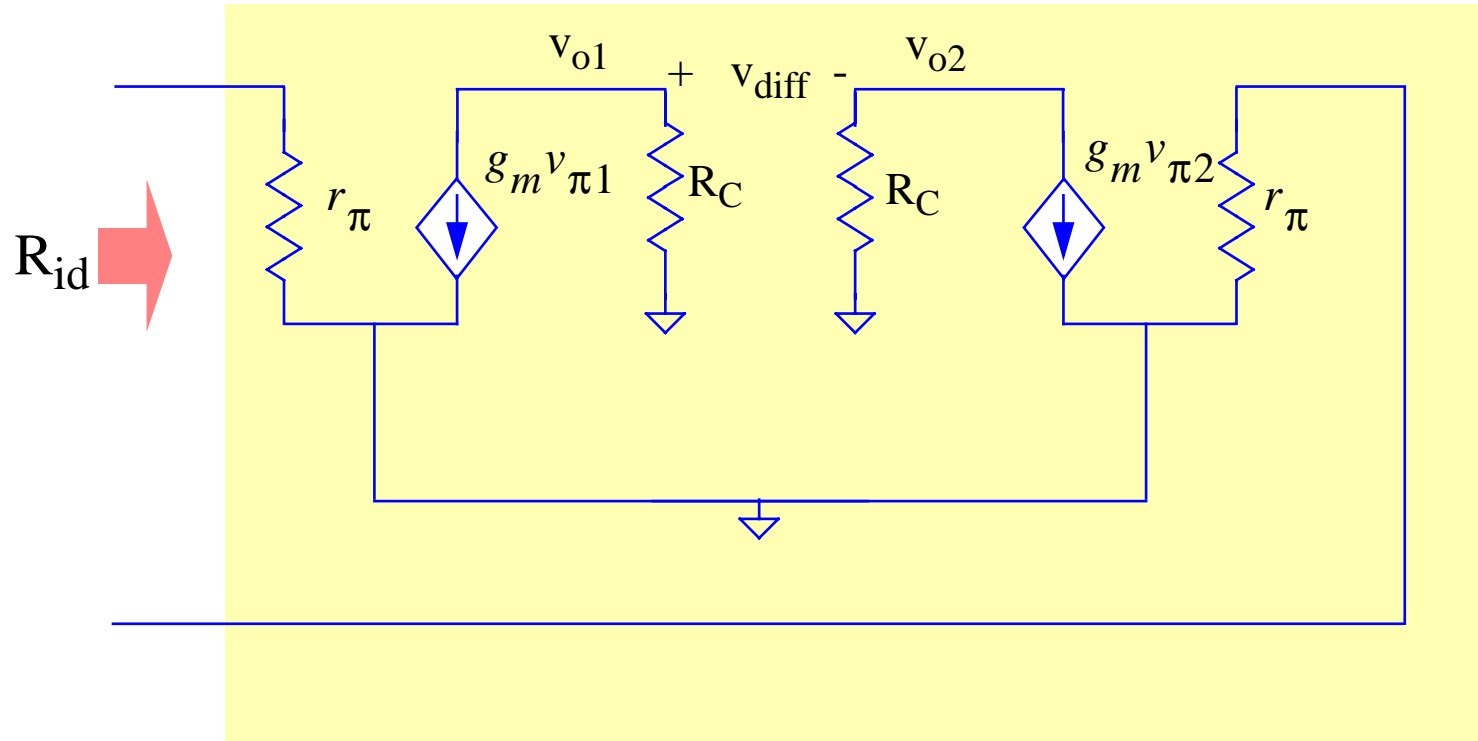
Calculate Gain

- What is the impact of r_o ?

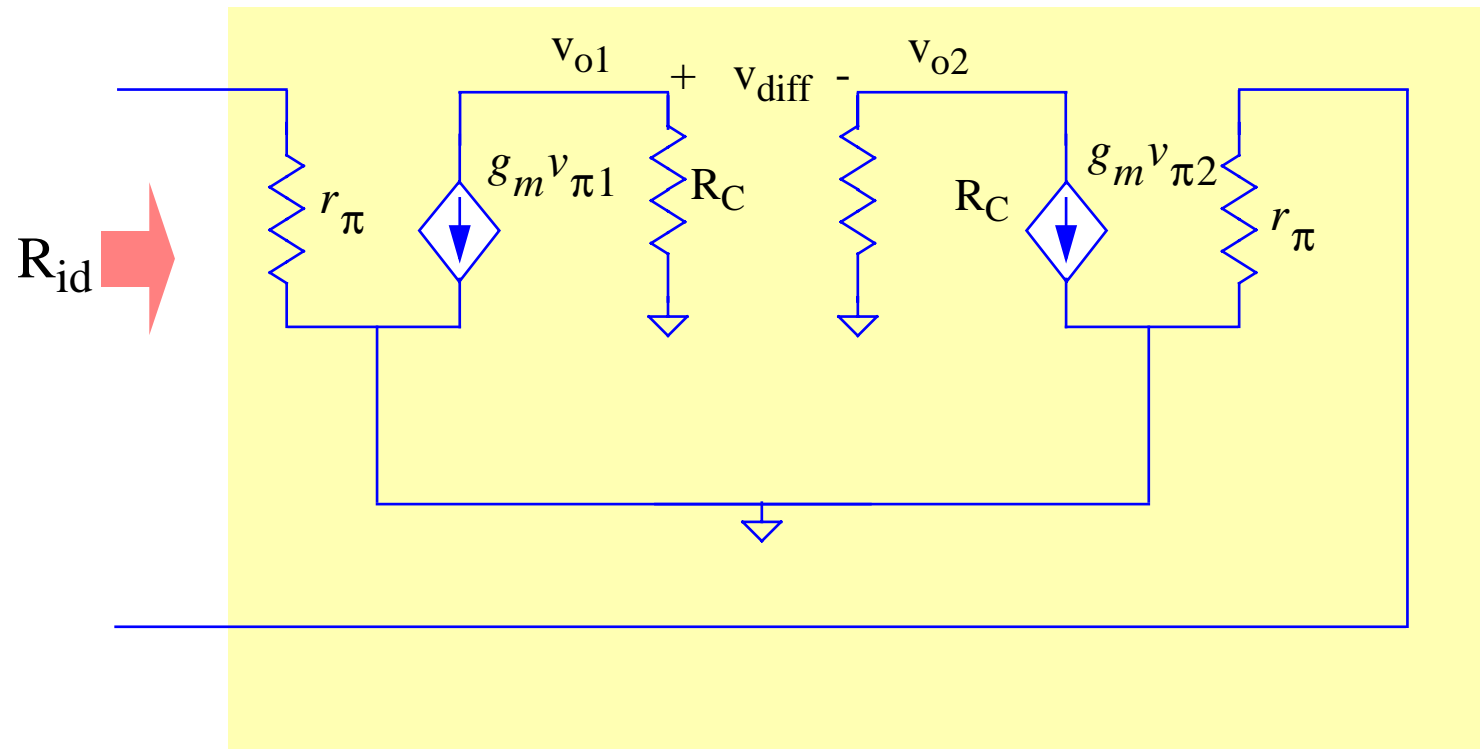


Differential Input Resistance

- The differential input resistance is huge

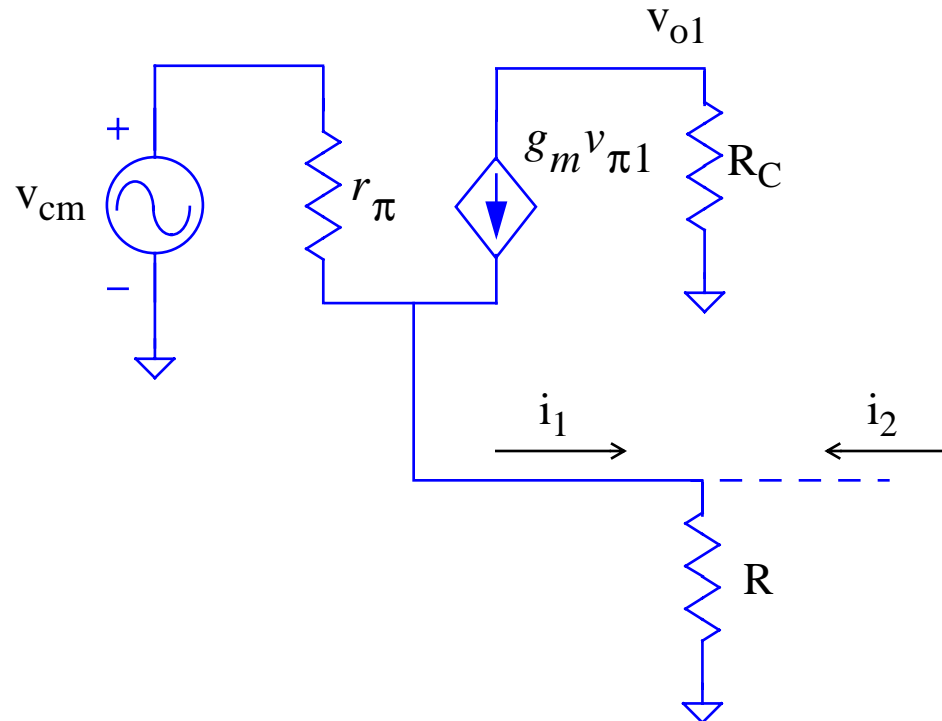


Differential Input Resistance



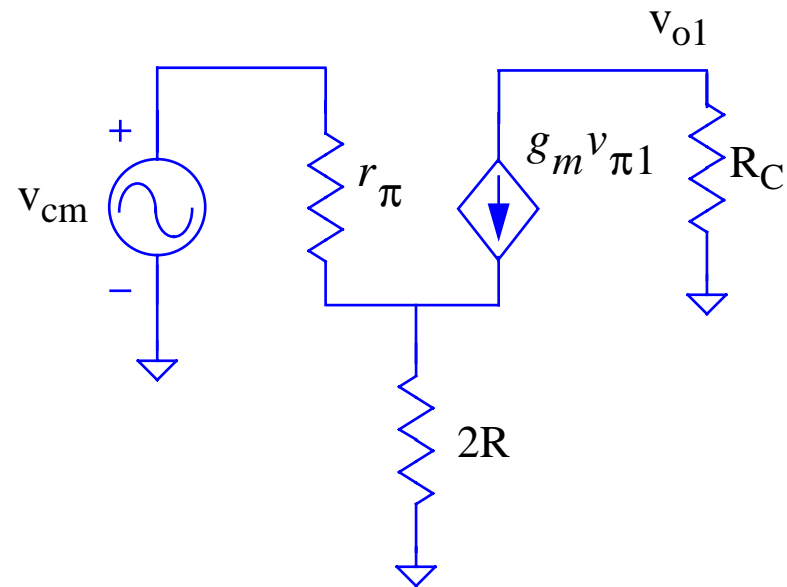
Common Mode Gain

- Just consider the common component of the input signal
- By symmetry arguments we only have to look at half of the ckt

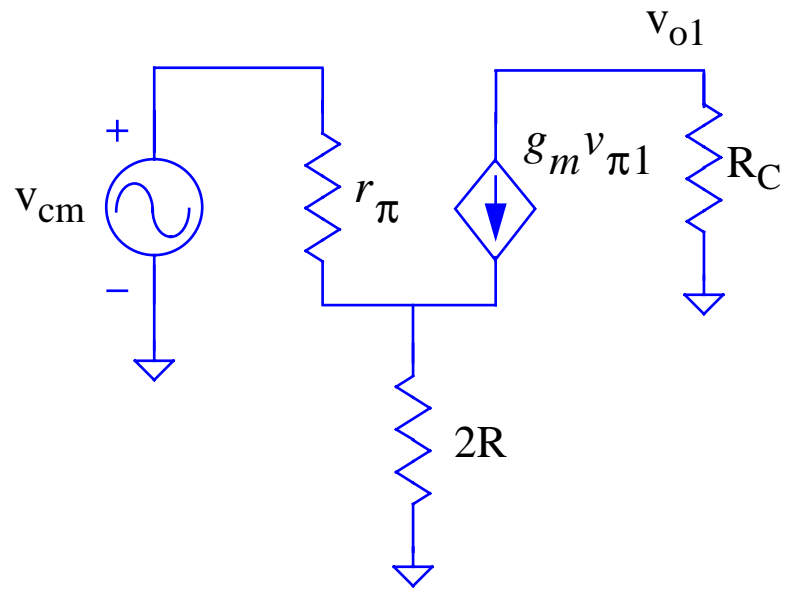


Common Mode Gain

- “Looks” like a common emitter amplifier with an emitter resistor



Common Mode Gain



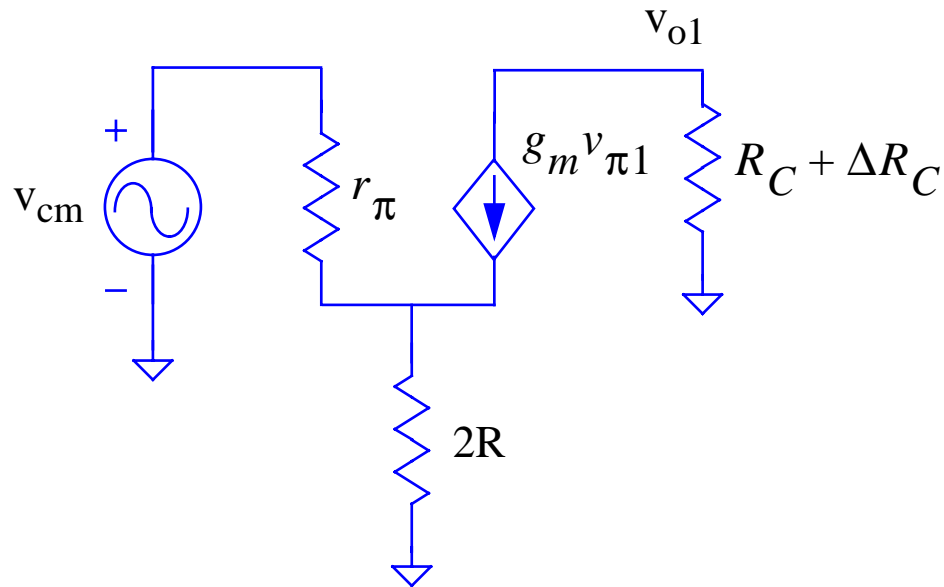
Common Mode Rejection Ratio

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

- If output is taken differentially, then the CMRR is apparently infinite
- But for a single sided output response is has a finite value

Common Mode Rejection Ratio

- More importantly, due to mismatch in parameters even the differential output CMRR is not infinite
- Assume one side has a variation in R_C

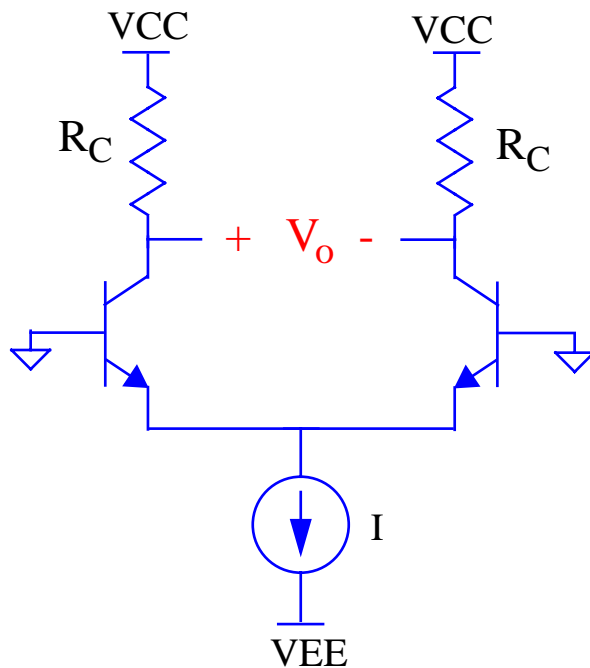


Common Mode and Differential Gain

- Process is controlled as tightly as possible to minimize A_{cm}

$$v_o = A_d(v_1 - v_2) + A_{cm}\left(\frac{v_1 + v_2}{2}\right)$$

- Mismatch in transistors Q1 and Q2 creates a dc offset voltage



Common Mode Characteristics

- Differential inputs (like opamps) have a common mode input resistance too --
- see derivation in the book
- Also, there is an input bias current to both inputs

- When the transistors are not perfectly matched there will be a slight offset in these values