Eric S. Chung

Curriculum Vitae—March 2011

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Research Interests

Application-specific computing with FPGAs, FPGA memory architecture, computer architecture, high-level synthesis, simulation methodology

Education

PhD in Electrical and Computer Engineering, 2004—2011 (expected)
Carnegie Mellon University – Pittsburgh, PA
Advisor: *Professor James C. Hoe*
Dissertation: *CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing*

B.S. in Electrical Engineering and Computer Science, Aug 2001—May 2004
University of California Berkeley – Berkeley, CA

Personal

- Date of Birth: March 6, 1984
- Citizenship: USA
- Languages: English, Mandarin

Awards and Achievements

- Best Paper Award, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (2011)
- John and Claire Bertucci Fellowship (2011)
- Microsoft Research Fellowship (2009-2010)
- Carnegie Mellon Laboratory for Computer Systems Fellowship (2004)
- Department Honors, University of California Berkeley, 2004
- Eta Kappa Nu: Berkeley Mu Chapter (top 25% in UCB EECS dept)
- Golden Key International Honor Society (top 15% at UC Berkeley)
- National Collegiate Inventors & Innovators Alliance Advanced E-Team Award (2004)
- World Journal Scholarship (2001-2004)
- Silicon Valley Scholars Award (2000)

Experiences

- **Research Intern, May—Aug 2008,** *Microsoft Research SVC, Computer Architecture Group*, Mountain View, CA, Mentors: Chuck Thacker, John Davis
- **Research Assistant, Oct 2002—May 2004,** *Group for User Interface Research at UC Berkeley*, Berkeley, CA, Mentors: Prof. James Landay, Prof. Jason Hong, Jimmy Lin
- **Co-founder, 2003—2005,** *Berkeley Innovation* – Berkeley, CA
- **Intern, Jun 2002 – Aug 2002,** *Dynamic Creation, LLC* – Cupertino, CA

Professional Service

- Student member of IEEE and ACM
- Member of Eta Kappa Nu Electrical Engineering Honor Society
- External reviewer for MICRO'10, HPCA'10, HIPEAC'10, MICRO'09, ASPLOS'08, PACT'05

Referred Journal and Conference Publications

1. Eric S. Chung, James C. Hoe, and Ken Mai. "CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing." *Proceedings of ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, February 27—March 1, 2011.
(Best Paper Award)

2. Eric S. Chung, Peter A. Milder, James C. Hoe, and Ken Mai. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO),* Atlanta, GA, December 4-8, 2010.

3. Eric S. Chung, James C. Hoe. "High-Level Design and Validation of the BlueSPARC Multithreaded Processor." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.29, no.10, pp.1459-1470,* October, 2010.

4. Eric S. Chung, James C. Hoe. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, July 13-15, 2009.

5. Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs." *ACM Transactions on Reconfigurable Technology and Systems (TRETS), Volume 2, Issue 2,* June 2009.

6. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations using FPGAs." *International Symposium on Field-Programmable Gate Arrays,* Monterey, CA, February 24-26, 2008.

7. Brian T. Gold, Jared C. Smolens, Jangwoo Kim, Eric S. Chung, Vasileios Liaskovitis, Eriko Nurvitadhi, Babak Falsafi, James C. Hoe, Andreas G. Nowatzyk. "TRUSS: Reliable, Scalable Server Architecture." *IEEE Micro, Special Issue on Reliability-Aware Microarchitectures,* November-December, 2005.

8. Eric S. Chung, Jason I. Hong, James Lin, Madhu K. Prabaker, James A. Landay, Alan L. Liu. "Design Patterns for Ubiquitous Computing." *Proceedings of Designing Interactive Systems,* Cambridge, Massachusetts, August 1-4, 2004.

Workshops, Posters and Technical Reports

9. Eric S. Chung, James C. Hoe, and Ken Mai. "Connected RAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *First Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, December 5, 2010.

10. Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi, Ken Mai. "The Open-Source ProtoFlex Simulator." *RAMP retreat*, Santa Cruz, CA, January 29, 2010. Poster.

11. Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi, and Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs." *Center for Circuit and System Solutions (C2S2) Annual Review*, 2009. Poster and abstract.

12. Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation." *RAMP Retreat*, Palo Alto, CA, August 20, 2008. Poster.

13. Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "An MP Architectural Exploration Vehicle Using Complexity-Effective FPGA-accelerated Simulation."

Proceedings of International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Seattle, WA, March 2, 2008. Poster and abstract.

14. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 9, 2007.

15. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "ProtoFlex: FPGA-Accelerated Hybrid Functional Simulator." *Workshop on the NSF Next Generation Software Program (NSFNGS)*, March 26-30, 2007.

16. Eric S. Chung, James C. Hoe, Babak Falsafi. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, February 12, 2006.

17. Jangwoo Kim, Eriko Nurvitadhi, Eric S. Chung. "Opportunity of Hardware-based Optimistic Concurrency in OLTP." *Selected Project Reports from Advanced OS & Distributed Systems, Spring 2005. Technical report CMU-CS-05-138.*

Talks and Invited Lectures

18. "CoRAM: An In-Fabric Memory Architecture for FPGA-Based Computing." *Invited talk at Altera, Inc.*, San Jose, CA, March 3, 2011.

19. "CoRAM: An In-Fabric Memory Architecture for FPGA-Based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 28, 2011.

20. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *International Symposium on Microarchitecture (MICRO)*, Atlanta, GA, December 6, 2010.

21. "CoRAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, December 5, 2010.

22. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, July 14, 2009.

23. "Open Source Protoflex Simulator." *RAMP retreat*, Austin, TX, June 25, 2009.

24. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, February 25, 2008.

25. "Usability Challenges for RAMP2." *RAMP retreat*, Berkeley, CA, January 15, 2009.

26. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *Invited talk at SUN Microsystems*, Santa Clara, CA, January 17, 2008.

27. "ProtoFlex Status Update and Design Experiences." *RAMP retreat*, Berkeley, CA, January 17, 2008.

28. "Accelerating Architectural-Level Full-System Simulations Using FPGAs." Invited talk at Microsoft Research, Redmond, CA, October 24, 2007.

29. "Architectural Emulation on FPGAs Made Easy with Bluespec." *Bluespec Workshop*, Boston, MA, August 13, 2007.

30. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 9, 2007.

31. "Protoflex: An FPGA-Accelerated Hybrid Functional Simulator." *RAMP retreat*, Berkeley, CA, January 11, 2007.

32. "Combining Simulators and FPGAs: An Out-of-Body Experience." *RAMP retreat*, Boston, MA, June 22, 2006.

33. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, February 12, 2006.

Tutorials

34. Derek Chiou, Eric S. Chung, Michael K. Papamichael, Hari Angepat, Angshuman Parashar, Zhangi Tan. "RAMP Simulator Tutorial: Protoflex, FAST, HAsim, and RAMP-Gold." *Tutorial at ISPASS-2010*, March 28, 2010.

35. Eric S. Chung, Mike Ferdman, and Michael K. Papamichael. "SimFlex and ProtoFlex." *Tutorial at MICRO-42*, December 12, 2009.

36. Eric S. Chung, Michael K. Papamichael. "ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation." *Tutorial at IISWC-2009*, October 4, 2008.

37. Eric S. Chung, Michael K. Papamichael. "ProtoFlex Tutorial: Full-System MP Simulations Using FPGAs." *Tutorial at ASPLOS-13*, March 2, 2008.

38. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "RAMP tutorial: ProtoFlex." *Tutorial at ISCA-34*, San Diego, CA, June 10, 2007.

Grant Writing Experience

39. CCF-SHF: Rethinking the Architecture of FPGAs as First-Class Computing Devices (NSF; CCF-1012851; J. Hoe—PI, K. Mai—Co-PI; $1,000,000, 2010-2014)

40. CPA-CSA: Accelerating Architectural-level, Full-system Multiprocessor Simulations Using FPGAs (NSF; CCF-0811702; J. Hoe—PI, $314,000, 2008-2011)

Teaching Experience

- **Fundamentals of Computer Engineering** at CMU with Prof. James Hoe (2006, TA rating: 4.5/5.0)
- **Advanced Computer Architecture** at CMU with Prof. James Hoe (2005, TA rating: 4.7/5.0)
- **Design Techniques for Digital Systems** at UCB with Prof. Randy Katz (2004, TA rating: 4.1/5.0)
- **Intro to Digital Electronics** at UCB with Prof. Andrew Neureuther (2003, TA rating: 4.8/5.0)