Staged Memory Scheduling

Rachata Ausavarungnirun, Kevin Chang, Lavanya Subramanian, Gabriel H. Loh, Onur Mutlu
“Staged Memory Scheduling: Achieving High Performance and Scalability in Heterogeneous Systems”
39th International Symposium on Computer Architecture (ISCA 2012),
Portland, OR, June 2012
Executive Summary

- **Observation:** Heterogeneous CPU-GPU systems require memory schedulers with large request buffers.

- **Problem:** Existing monolithic application-aware memory scheduler designs are hard to scale to large request buffer sizes.

- **Solution:** Staged Memory Scheduling (SMS) decomposes the memory controller into three simple stages:
  1. Batch formation: maintains row buffer locality
  2. Batch scheduler: reduces interference between applications
  3. DRAM command scheduler: issues requests to DRAM

- Compared to state-of-the-art memory schedulers:
  - SMS is significantly simpler and more scalable
  - SMS provides higher performance and fairness
Outline

- Background
- Motivation
- Our Goal
- Observations
- Staged Memory Scheduling
  1) Batch Formation
  2) Batch Scheduler
  3) DRAM Command Scheduler
- Results
- Conclusion
All cores contend for limited off-chip bandwidth
  - Inter-application interference degrades system performance
  - The memory scheduler can help mitigate the problem

How does the memory scheduler deliver good performance and fairness?
Three Principles of Memory Scheduling

- Prioritize row-buffer-hit requests [Rixner+, ISCA’00]
  - To maximize memory bandwidth

- Prioritize latency-sensitive applications [Kim+, HPCA’10]
  - To maximize system throughput

- Ensure that no application is starved [Mutlu and Moscibroda, MICRO’07]
  - To minimize unfairness

<table>
<thead>
<tr>
<th>Application</th>
<th>Memory Intensity (MPKI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
</tr>
</tbody>
</table>
Outline

- Background
- Motivation: CPU-GPU Systems
- Our Goal
- Observations
- Staged Memory Scheduling
  1) Batch Formation
  2) Batch Scheduler
  3) DRAM Command Scheduler
- Results
- Conclusion
Memory Scheduling for CPU-GPU Systems

- Current and future systems integrate a GPU along with multiple cores
- GPU shares the main memory with the CPU cores
- GPU is much more (4x-20x) memory-intensive than CPU
- How should memory scheduling be done when GPU is integrated on-chip?
Introducing the GPU into the System

- GPU occupies a significant portion of the request buffers
  - Limits the MC’s visibility of the CPU applications’ differing memory behavior → can lead to a **poor scheduling decision**
Naïve Solution: Large Monolithic Buffer

Memory Scheduler

To DRAM
Problems with Large Monolithic Buffer

- A large buffer requires more complicated logic to:
  - Analyze memory requests (e.g., determine row buffer hits)
  - Analyze application characteristics
  - Assign and enforce priorities

- This leads to high complexity, high power, large die area

- More Complex Memory Scheduler
Our Goal

- Design a new memory scheduler that is:
  - **Scalable** to accommodate a large number of requests
  - Easy to implement
  - Application-aware
  - Able to provide high performance and fairness, especially in heterogeneous CPU-GPU systems
Outline

- Background
- Motivation: CPU-GPU Systems
- Our Goal
- Observations
  - Staged Memory Scheduling
    1) Batch Formation
    2) Batch Scheduler
    3) DRAM Command Scheduler
- Results
- Conclusion
Key Functions of a Memory Controller

- Memory controller must consider three different things concurrently when choosing the next request:
  
  1) Maximize row buffer hits
     - Maximize memory bandwidth
  2) Manage contention between applications
     - Maximize system throughput and fairness
  3) Satisfy DRAM timing constraints

- Current systems use a *centralized memory controller design* to accomplish these functions
  - Complex, especially with large request buffers
Key Idea: Decouple Tasks into Stages

- **Idea:** Decouple the functional tasks of the memory controller
  - Partition tasks across several simpler HW structures (stages)

1) Maximize row buffer hits
   - **Stage 1:** Batch formation
   - Within each application, groups requests to the same row into batches

2) Manage contention between applications
   - **Stage 2:** Batch scheduler
   - Schedules batches from different applications

3) Satisfy DRAM timing constraints
   - **Stage 3:** DRAM command scheduler
   - Issues requests from the already-scheduled order to each bank
Outline

- Background
- Motivation: CPU-GPU Systems
- Our Goal
- Observations
- Staged Memory Scheduling
  1) Batch Formation
  2) Batch Scheduler
  3) DRAM Command Scheduler
- Results
- Conclusion
SMS: Staged Memory Scheduling
SMS: Staged Memory Scheduling

Stage 1
Batch Formation

Stage 2
Batch Scheduler

Stage 3
DRAM Command Scheduler

To DRAM
Stage 1: Batch Formation

- **Goal:** *Maximize row buffer hits*

- At each core, we want to **batch requests that access the same row within a limited time window**

- A batch is ready to be scheduled under two conditions
  1) When the next request accesses a different row
  2) When the time window for batch formation expires

- Keep this stage simple by using **per-core FIFOs**
Stage 1: Batch Formation Example

Stage 1

Batch Formation

Core 1
Row A

Core 2
Row C
Row B

Core 3
Row E

Core 4
Row F

To Stage 2 (Batch Scheduling)
SMS: Staged Memory Scheduling

Stage 1
Batch Formation

Stage 2
Batch Scheduler

Stage 3
DRAM Command Scheduler

Core 1 → Core 2 → Core 3 → Core 4 → GPU

To DRAM
Stage 2: Batch Scheduler

- **Goal:** Minimize interference between applications

- Stage 1 forms batches *within each application*
- Stage 2 schedules batches *from different applications*
  - Schedules the oldest batch from each application

- Question: Which application’s batch should be scheduled next?

- **Goal:** Maximize system performance and fairness
  - To achieve this goal, the batch scheduler chooses between two different policies
Stage 2: Two Batch Scheduling Algorithms

- **Shortest Job First (SJF)**
  - Prioritize the applications with the fewest outstanding memory requests because they make fast forward progress
  - **Pro:** Good system performance and fairness
  - **Con:** GPU and memory-intensive applications get deprioritized

- **Round-Robin (RR)**
  - Prioritize the applications in a round-robin manner to ensure that memory-intensive applications can make progress
  - **Pro:** GPU and memory-intensive applications are treated fairly
  - **Con:** GPU and memory-intensive applications significantly slow down others
Stage 2: Batch Scheduling Policy

- The importance of the GPU varies between systems and over time → Scheduling policy needs to adapt to this

- **Solution**: Hybrid Policy
- At every cycle:
  - With probability $p$: Shortest Job First → Benefits the CPU
  - With probability $1-p$: Round-Robin → Benefits the GPU

- System software can configure $p$ based on the importance/weight of the GPU
  - Higher GPU importance → Lower $p$ value
SMS: Staged Memory Scheduling

Stage 1
Batch Formation

Stage 2
Batch Scheduler

Stage 3
DRAM Command Scheduler

To DRAM
Stage 3: DRAM Command Scheduler

- High level policy decisions have already been made by:
  - Stage 1: Maintains row buffer locality
  - Stage 2: Minimizes inter-application interference

- Stage 3: No need for further scheduling
- Only goal: service requests while satisfying DRAM timing constraints

- Implemented as simple per-bank FIFO queues
Putting Everything Together

Stage 1:
Batch Formation

Stage 2:
Batch Scheduler

Stage 3:
DRAM Command Scheduler

Current Batch Scheduling Policy
RR
Complexity

- Compared to a row hit first scheduler, SMS consumes:
  - 66% less area
  - 46% less static power

- Reduction comes from:
  - Monolithic scheduler $\rightarrow$ stages of simpler schedulers
  - Each stage has a simpler scheduler (considers fewer properties at a time to make the scheduling decision)
  - Each stage has simpler buffers (FIFO instead of out-of-order)
  - Each stage has a portion of the total buffer size (buffering is distributed across stages)

* Based on a Verilog model using 180nm library
Outline

- Background
- Motivation: CPU-GPU Systems
- Our Goal
- Observations
- Staged Memory Scheduling
  1) Batch Formation
  2) Batch Scheduler
  3) DRAM Command Scheduler
- Results
- Conclusion
Methodology

- Simulation parameters
  - 16 OoO CPU cores, 1 GPU modeling AMD Radeon™ 5870
  - DDR3-1600 DRAM 4 channels, 1 rank/channel, 8 banks/channel

- Workloads
  - CPU: SPEC CPU 2006
  - GPU: Recent games and GPU benchmarks
  - 7 workload categories based on the memory-intensity of CPU applications
    - Low memory-intensity (L)
    - Medium memory-intensity (M)
    - High memory-intensity (H)
Comparison to Previous Scheduling Algorithms

- **FR-FCFS [Rixner+, ISCA’00]**
  - Prioritizes row buffer hits
  - Maximizes DRAM throughput
  - Low multi-core performance → Application unaware

- **ATLAS [Kim+, HPCA’10]**
  - Prioritizes latency-sensitive applications
  - Good multi-core performance
  - Low fairness → Deprioritizes memory-intensive applications

- **TCM [Kim+, MICRO’10]**
  - Clusters low and high-intensity applications and treats each separately
  - Good multi-core performance and fairness
  - Not robust → Misclassifies latency-sensitive applications
Evaluation Metrics

- CPU performance metric: Weighted speedup
  \[ CPU_{WS} = \sum \frac{IPC_{Shared}}{IPC_{ Alone}} \]

- GPU performance metric: Frame rate speedup
  \[ GPU_{Speedup} = \frac{FrameRate_{Shared}}{FrameRate_{ Alone}} \]

- CPU-GPU system performance: CPU-GPU weighted speedup
  \[ CGWS = CPU_{WS} + GPU_{Speedup} \times GPU_{Weight} \]
Evaluated System Scenarios

- CPU-focused system
- GPU-focused system
Evaluated System Scenario: CPU Focused

- GPU has low weight (weight = 1)

\[ CGWS = \text{CPU}_{WS} + \text{GPU}_{Speedup} \times \text{GPU}_{Weight} \]

- Configure SMS such that \( \rho \), SJF probability, is set to 0.9
  - Mostly uses SJF batch scheduling \( \rightarrow \) prioritizes latency-sensitive applications (mainly CPU)
SJF batch scheduling policy allows latency-sensitive applications to get serviced as fast as possible.

Performance: CPU-Focused System

- SMS is much less complex than previous schedulers
- +17.2% over ATLAS

Workload Categories

- L
- ML
- M
- HL
- HML
- HM
- H
- Avg

SMs

SMS

$\rho=0.9$
Evaluated System Scenario: GPU Focused

- GPU has **high** weight (weight = 1000)

\[ CGWS = CPU_{WS} + GPU_{Speedup} \times GPU_{Weight} \]

- Configure SMS such that \( \rho \), SJF probability, is set to 0
  - Always uses **round-robin** batch scheduling \( \rightarrow \) prioritizes memory-intensive applications (GPU)
Performance: GPU-Focused System

- Round-robin batch scheduling policy schedules GPU requests more frequently

---

SMS is much less complex than previous schedulers

+1.6% over FR-FCFS
Performance at Different GPU Weights

![Graph showing system performance vs. GPU weight for different schedulers: ATLAS, TCM, FR-FCFS. The best previous scheduler is highlighted.](image-url)
At every GPU weight, SMS outperforms the best previous scheduling algorithm for that weight.
Additional Results in the Paper

- Fairness evaluation
  - 47.6% improvement over the best previous algorithms

- Individual CPU and GPU performance breakdowns

- CPU-only scenarios
  - Competitive performance with previous algorithms

- Scalability results
  - SMS’ performance and fairness scales better than previous algorithms as the number of cores and memory channels increases

- Analysis of SMS design parameters
Outline

- Background
- Motivation: CPU-GPU Systems
- Our Goal
- Observations
- Staged Memory Scheduling
  1) Batch Formation
  2) Batch Scheduler
  3) DRAM Command Scheduler
- Results
- Conclusion
Conclusion

- **Observation:** Heterogeneous CPU-GPU systems require memory schedulers with **large request buffers**

- **Problem:** Existing monolithic application-aware memory scheduler designs are **hard to scale** to large request buffer size

- **Solution:** Staged Memory Scheduling (SMS) decomposes the memory controller into three simple stages:
  1) Batch formation: maintains row buffer locality
  2) Batch scheduler: reduces interference between applications
  3) DRAM command scheduler: issues requests to DRAM

- Compared to state-of-the-art memory schedulers:
  - **SMS** is significantly simpler and more scalable
  - **SMS** provides higher performance and fairness
Coordinated Control of Multiple Prefetchers in Multi-Core Systems

Eiman Ebrahimi, Onur Mutlu, Chang Joo Lee, Yale N. Patt

“Coordinated Control of Multiple Prefetchers in Multi-Core Systems”

42nd International Symposium on Microarchitecture (HPCA 2009),
New York, NY, December 2009
Motivation

- Aggressive prefetching improves memory latency tolerance of many applications when they run alone

- Prefetching for concurrently-executing applications on a CMP can lead to
  - Significant system performance degradation and bandwidth waste

- Problem:
  Prefetcher-caused inter-core interference
  - Prefetches of one application contend with prefetches and demands of other applications
Potential Performance

System performance improvement of *ideally* removing all prefetcher-caused inter-core interference in shared resources

Exact workload combinations can be found in paper
Outline

- Background
- Shortcoming of Prior Approaches to Prefetcher Control
- Hierarchical Prefetcher Aggressiveness Control
- Evaluation
- Conclusion
Increasing Prefetcher Accuracy

- Increasing prefetcher accuracy can reduce prefetcher-caused inter-core interference
  - Single-core prefetcher aggressiveness throttling (e.g., Srinath et al., HPCA ’07)
  - Filtering inaccurate prefetches (e.g., Zhuang and Lee, ICPP ’03)
  - Dropping inaccurate prefetches at memory controller (Lee et al., MICRO ’08)

All such techniques operate *independently* on the prefetches of each application
Feedback-Directed Prefetching (FDP) (Srinath et al., HPCA ’07)

- Uses prefetcher feedback information local to the prefetcher’s core
  - Prefetch accuracy
  - Prefetch timeliness
  - Prefetch cache pollution
- Dynamically adapts the prefetcher’s aggressiveness
- Stream Prefetcher Aggressiveness
  - Prefetch Distance
  - Prefetch Degree

Shown to perform better than and consume less bandwidth than static aggressiveness configurations
Outline

- Background
- Shortcoming of Prior Approaches to Prefetcher Control
- Hierarchical Prefetcher Aggressiveness Control
- Evaluation
- Conclusion
High Interference caused by Accurate Prefetchers

In a CMP system, accurate prefetchers can cause significant interference with concurrently-executing applications.
Local-only prefetcher control techniques have no mechanism to detect inter-core interference.
Shortcoming of Local-Only Prefetcher Control

4-core workload example: lbm_06 + swim_00 + crafty_00 + bzip2_00

Our Approach: Use both *global* and per-core feedback to determine each prefetcher’s aggressiveness
Outline

- Background
- Shortcoming of Prior Approaches to Prefetcher Control
- Hierarchical Prefetcher Aggressiveness Control
- Evaluation
- Conclusion
Hierarchical Prefetcher Aggressiveness Control (HPAC)

Global Control: accepts or overrides decisions made by local control to improve prefetching performance of core \( i \) independently.

Global Control’s goal: Keep track of and control prefetcher-caused inter-core interference in shared memory system.

Local Control

Pref. \( i \)

Throttling Decision

Accuracy

Local Throttling Decision

Core \( i \)

Final Throttling Decision

Memory Controller

Bandwidth Feedback

Global Control

Cache Pollution Feedback

Shared Cache
Terminology

- Global feedback metrics used in our mechanism:
  - For each core $i$:
    - Core $i$'s prefetcher accuracy – $Acc\ (i)$
    - Core $i$'s prefetcher caused inter-core cache pollution $Pol\ (i)$
      - Demand cache lines of other cores evicted by this core’s prefetches that are requested subsequent to eviction
    - Bandwidth consumed by core $i$ - $BW\ (i)$
      - Accounts for how long requests from this core tie up DRAM banks
    - Bandwidth needed by other cores $j \neq i$ - $BWNO\ (i)$
      - Accounts for how long requests from other cores have to wait for DRAM banks because of requests from this core
Calculating Inter-Core Cache Pollution

Core \( j \) experiences a demand cache miss

\[ \text{Increment Pol (} i \text{)} \]

Hash Function

Pollution Filter of core \( i \)

<table>
<thead>
<tr>
<th>Pollution bit</th>
<th>Core id</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>( j )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

Evicted line’s Address
From core \( j \)
Hierarchical Prefetcher Aggressiveness Control (HPAC)

- High accuracy
- High pollution
- High bandwidth consumed while other cores need bandwidth
Heuristics for Global Control

Classification of global control heuristics based on interference severity

- Severe interference
  - Action: Reduce the aggressiveness of interfering prefetcher

- Borderline interference
  - Action: Prevent prefetcher from transitioning into severe interference:
    - Allow local-control to only throttle-down

- No interference or moderate interference from an accurate prefetcher
  - Action: Allow local control to maximize local benefits from prefetching
## HPAC Control Policies

<table>
<thead>
<tr>
<th>Pol (i)</th>
<th>Acc (i)</th>
<th>BW (i)</th>
<th>BWNO (i)</th>
<th>Interference Class</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Causing Low Pollution</td>
<td></td>
<td></td>
<td>Others’ low BW need</td>
<td>Severe interference</td>
<td>throttle down</td>
</tr>
<tr>
<td></td>
<td>Inaccurate</td>
<td>Low BW Consumption</td>
<td>Others’ high BW need</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others’ low BW need</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Causing High Pollution |          |         | Others’ low BW need                   | Severe interference | throttle down  |
|                       | Inaccurate | Low BW Consumption | Others’ high BW need |                |                |
|                       |          |         | Others’ low BW need                   |                    |                |

| Causing Low Pollution |          |         | Others’ low BW need                   | Severe interference | throttle down  |
|                       | Inaccurate | High BW Consumption | Others’ high BW need |                |                |
|                       |          |         | Others’ low BW need                   |                    |                |

| Causing High Pollution |          |         | Others’ low BW need                   | Severe interference | throttle down  |
|                       | Inaccurate | High BW Consumption | Others’ high BW need |                |                |
|                       |          |         | Others’ low BW need                   |                    |                |
Hardware Cost (4-Core System)

<table>
<thead>
<tr>
<th>Description</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total hardware cost local-control &amp; global control</td>
<td>15.14 KB</td>
</tr>
<tr>
<td>Additional cost on top of FDP</td>
<td>1.55 KB</td>
</tr>
</tbody>
</table>

- **Additional** cost on top of FDP only 1.55 KB

- HPAC does not require any structures or logic that are on the processor’s critical path
Outline

- Background
- Shortcoming of Prior Approaches to Prefetcher Control
- Hierarchical Prefetcher Aggressiveness Control
- Evaluation
- Conclusion
### Evaluation Methodology

- **x86 cycle accurate simulator**

- **Baseline processor configuration**
  - Per core
    - 4-wide issue, out-of-order, 256-entry ROB
    - Stream prefetcher with 32 streams, prefetch degree: 4, prefetch distance: 64
  - Shared
    - 2MB, 16-way L2 cache (4MB, 32-way for 8-core)
    - DDR3 1333Mhz
    - 8B wide core to memory bus
    - 128, 256 L2 MSHRs for 4-, 8-core
    - Latency of 15ns per command (tRP, tRCD, CL)

- **HPAC thresholds used**

<table>
<thead>
<tr>
<th>Acc</th>
<th>BW</th>
<th>Pol</th>
<th>BWNO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6</td>
<td>50k</td>
<td>90</td>
<td>75k</td>
</tr>
</tbody>
</table>
Performance Results

Exact workload combinations can be found in paper
Summary of Other Results

- Further results and analysis are presented in the paper
  - Results with different types of memory controllers
    - Prefetch-Aware DRAM Controllers (PADC)
    - First-Ready First-Come-First-Served (FR-FCFS)
  - Effect of HPAC on system fairness
  - HPAC performance on 8-core systems
  - Multiple types of prefetchers per core and different local-control policies
  - Sensitivity to system parameters
Conclusion

- Prefetcher-caused inter-core interference can destroy potential performance of prefetching
  - When prefetching for concurrently executing applications in CMPs
  - Did not exist in single-application environments

- Develop one low-cost hierarchical solution which throttles different cores’ prefetchers in a coordinated manner

- The key is to take global feedback into account to determine aggressiveness of each core’s prefetcher
  - Improves system performance by 15% compared to no throttling on a 4-core system
  - Enables performance improvement from prefetching that is not possible without it on many workloads
Thank you!

Questions?
Staged Memory Scheduling

Rachata Ausavarungnirun, Kevin Chang, Lavanya Subramanian, Gabriel H. Loh*, Onur Mutlu

Carnegie Mellon University, *AMD Research
June 12th 2012
Row Buffer Locality on Batch Formation

- OoO batch formation improves the performance of the system by:
  - ~3% when the batch scheduler uses SJF policy most of the time
  - ~7% when the batch scheduler uses RR most of the time

- However, OoO batch formation is more complex
  - OoO buffering instead of FIFO queues
  - Need to fine tune the time window of the batch formation based on application characteristics (only 3%-5% performance gain without fine tuning)
Row Buffer Locality on Batch Formation

**CPU-WS**

<table>
<thead>
<tr>
<th>FR-FCFS</th>
<th>SMS-SJF</th>
<th>SMS_SJF-OoO</th>
<th>SMS-RR</th>
<th>SMS-RR-OoO</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>5</td>
<td>6</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

**GPU-Frame Rate**

<table>
<thead>
<tr>
<th>FR-FCFS</th>
<th>SMS-SJF</th>
<th>SMS_SJF-OoO</th>
<th>SMS-RR</th>
<th>SMS-RR-OoO</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>80</td>
<td>80</td>
<td>70</td>
<td>80</td>
</tr>
</tbody>
</table>
Key Differences Between CPU and GPU

Memory Intensity

L2 MPKI

Game01  Game03  Game05  Bench02  gromacs  cactusADM  mcf

Graphic Applications  CPU Applications

~4x difference
MLP and RBL

- Key differences between a CPU application and a GPU application

![Memory Level Parallelism](chart1)

![Row Buffer Locality](chart2)
CPU-GPU Performance Tradeoff

**CPU Performance**

- **weighted speedup**
  - SJF Probability: 1, 0.5, 0.1, 0.05, 0

**GPU Frame Rate**

- **frame rate**
  - SJF Probability: 1, 0.5, 0.1, 0.05, 0
Dealing with Multi-Threaded Applications

- **Batch formation:** Groups requests from each application in a per-thread FIFO.

- **Batch scheduler:** Detects critical threads and prioritizes them over non-critical threads.
  - Previous works have shown how to detect and schedule critical threads:
    1. Bottleneck Identification and Scheduling in MT applications [Joao+, ASPLOS’12]
    2. Parallel Application Memory Scheduling [Ebrahimi, MICRO’11]

- **DRAM command scheduler:** Stays the same.
Dealing with Prefetch Requests

- Previous works have proposed several solutions:
  - Prefetch-Aware Shared-Resource Management for Multi-Core Systems [Ebrahimi+, ISCA’11]
  - Coordinated Control of Multiple Prefetchers in Multi-Core Systems [Ebrahimi+, MICRO’09]
  - Prefetch-aware DRAM Controller [Lee+, MICRO’08]

- Handling Prefetch Requests in SMS:
  - SMS can handle prefetch requests before they enter the memory controller (e.g., source throttling based on prefetch accuracy)
  - SMS can handle prefetch requests by prioritizing/deprioritizing prefetch batch at the batch scheduler (based on prefetch accuracy)
Fairness Evaluation

Unfairness (Lower is better)
Performance at Different Buffer Sizes
CPU and GPU Performance Breakdowns

CPU WS

Frame Rate
CPU-Only Results

The chart illustrates the system performance and unfairness for different scenarios and algorithms. The x-axis represents various categories (HL, HML, HM, H, Avg), and the y-axis shows system performance (higher is better) and unfairness (lower is better). The bars represent different algorithms: FR-FCFS, ATLAS, TCM, and SMS.
Scalability to Number of Cores

CPU Weighted Speedup (Higher is Better)

GPU Frame Rate (Higher is Better)

Unfairness (Lower is Better)
Scalability to Number of Memory Controllers

CPU Weighted Speedup (Higher is Better)

GPU Frame Rate (Higher is Better)

Unfairness (Lower is Better)
## Detailed Simulation Methodology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of cores</td>
<td>16</td>
<td>GPU Max throughput</td>
<td>1600 ops/cycle</td>
</tr>
<tr>
<td>Number of GPU</td>
<td>1</td>
<td>GPU Texture/Z/Color units</td>
<td>80/128/32</td>
</tr>
<tr>
<td>CPU reorder buffers</td>
<td>128 entries</td>
<td>DRAM Bus</td>
<td>64 bits/channel</td>
</tr>
<tr>
<td>L1 (private) cache size</td>
<td>32KB, 4 ways</td>
<td>DRAM row buffer size</td>
<td>2KB</td>
</tr>
<tr>
<td>L2 (shared) cache size</td>
<td>8MB, 16 ways</td>
<td>MC Request buffer size</td>
<td>300 entries</td>
</tr>
<tr>
<td>ROB Size</td>
<td>128 entries</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Analysis to Different SMS Parameters

**Threshold Age**

- 0%
- 50%
- 100%
- 200%
- 300%

**DCS FIFO Size**

- 5
- 10
- 15
- 20

**Normalized Value**

- CPU-Perf.
- Unfairness
- FrameRate
Global Bypass

- What if the system is lightly loaded?
  - Batching will increase the latency of requests

- Global Bypass
  - Disable the batch formation when the number of total requests is lower than a threshold