15-740/18-740 Computer Architecture Homework 5

Due Friday, November 11, at 12:00 PM

1. Cache Organization

A very small, in-order embedded processor has a five-bit physical address space and a physically-addressed cache. Memory is byte addressable and the cache uses perfect LRU replacement. Assume the cache initially contains no valid data.

Suppose a program generates the following access stream and you observe the hit/miss outcome of the cache for each access as follows:

Address	Outcome
5	Miss
2	Miss
0	Miss
4	Hit
25	Miss
9	Miss
1	Hit
25	Hit
16	Miss
9	Miss
1	Miss

Hint: For the following questions, keep in mind your answers need not be powers of two.

- (a) What is the size of a cache block in bytes?
- (b) What is the associativity of the cache?
- (c) How much storage (in bytes) is required for the data portion of the cache?
- (d) What is the minimal amount of storage (in bytes) required for the tag portion of the cache (hint: this includes the address tag, modified data, valid data, and age information)?

2. Cache Hierarchy

For this question, assume there are two systems, A and B, each with two levels of on-chip cache. The systems are identical in every way except that system A employs an inclusive caching policy for its on-chip caches while system B uses an exclusive caching policy.

- (a) You run a program on system A and find that it runs more slowly than when run on system B. Why might this be the case?
- (b) You run a program on system B and find that it runs more slowly than when run on system A. Why might this be the case?