



## Carnegie Mellon University Course Syllabus

### 18-447: Introduction to Computer Architecture

Spring Semester, 2015

<http://www.ece.cmu.edu/~ece447/>

#### Course Personnel:

##### *Instructor:*

- Onur Mutlu  
Collaborative Innovation Center (CIC) 4105 (4<sup>th</sup> floor), 412-268-1186  
<http://users.ece.cmu.edu/~omutlu/>  
[omutlu@gmail.com](mailto:omutlu@gmail.com), [onur@cmu.edu](mailto:onur@cmu.edu)  
Office Hours: Wednesdays 2:30PM-3:30PM, or by appointment

##### *Teaching Assistants:*

	Email	Office Hours (CIC 4 <sup>th</sup> Floor)
• Rachata Ausavarungnirun	<a href="mailto:rachata@cmu.edu">rachata@cmu.edu</a>	Tue 3-4 PM
• Kevin Chang	<a href="mailto:kevincha@cmu.edu">kevincha@cmu.edu</a>	Mon 3-4 PM
• Albert Cho	<a href="mailto:aycho@andrew.cmu.edu">aycho@andrew.cmu.edu</a>	Fri 2:30-3:30 PM
• Jeremie Kim	<a href="mailto:jeremiek@andrew.cmu.edu">jeremiek@andrew.cmu.edu</a>	Wed 3:30-4:30 PM
• Clement Loh	<a href="mailto:changshl@andrew.cmu.edu">changshl@andrew.cmu.edu</a>	Thu 4:30-5:30 PM

##### *Course Management Assistant:*

- Zara Collier  
Hamerschlag Hall 1112

---

#### Course Description:

Computer architecture is the science and art of selecting and interconnecting hardware components to create a computer that meets functional, performance and cost goals. This course introduces the basic hardware structure of a modern programmable computer, including the basic laws underlying performance evaluation. We will learn, for example, how to design the control and data path hardware for a MIPS-like processor, how to make machine instructions execute simultaneously through pipelining and simple superscalar execution, and how to design fast memory and storage systems. The principles presented in the lecture are reinforced in the laboratory through the design and simulation of a register transfer (RT) implementation of a MIPS-like pipelined processor in System Verilog. In addition, we will develop a cycle-accurate simulator of this processor in C, and we will use this simulator to explore processor design options. Learning to design programmable systems requires that you already have the knowledge of building RT systems as is taught in the prerequisite 18-240, the knowledge of the behavior storage hierarchies (e.g., cache memories) and virtual memory as is taught in the prerequisite 15-213, and the knowledge of assembly language programming as is taught in the prerequisites.

**Prerequisites:** 18-240 and (15-213 or 18-243) and (18-340 or 18-341 or 18-348 or 18-349 or 18-320)

**Prerequisite for:** 18-545, 18-725, 18-740

**Undergraduate Area:** Computer Hardware

**Undergraduate Designation:** Coverage, Depth

**Course Schedule:**

- **Lecture:**  
Mon., Wed., and Fri.: 12:30p.m. – 2:20 p.m., Hamerschlag Hall (HH) 1107
- **Recitations:**

Section A	T: 10:30 a.m. – 1:20 p.m.	Hamerschlag Hall (HH) 1303
Section B	Th: 1:30 p.m. – 4:20 p.m.	HH 1303
Section C	F: 6:30 p.m. – 9:20 p.m.	HH 1303

Recitations will cover lecture material, homework, lab assignments, and the TAs will conduct them. You can attend any recitation, regardless of which one you are registered for.

**Recommended Readings and Textbooks:**

- Lecture slides, videos, readings, homework, and exams from Spring 2014, Spring 2013, and past incarnations of the course:  
<http://www.ece.cmu.edu/~ece447/s14/>  
<http://www.ece.cmu.edu/~ece447/s13/>

**There is no required textbook.** I recommend several textbooks below which may be helpful supplements to the material covered in the lectures, labs, and homework assignments. You can place orders for these books at the CMU bookstore.

- *Computer Organization and Design: The Hardware/Software Interface, Fourth Edition* by Patterson and Hennessy, Morgan Kaufmann/ Elsevier, 2009.
- *HDL Compiler for Verilog Reference Manual* by Synopsys, Inc.  
<http://www.ece.cmu.edu/~ece447/s15/lib/exe/fetch.php?media=hdlcv.pdf>
- *Introduction to Computing Systems: From Bits and Gates to C and Beyond, Second Edition* by Patt and Patel, McGraw-Hill.
- *Computer Organization* by Hamacher, Vranesic, and Zaky, McGraw-Hill.
- *Computer Architecture and Implementation* by Harvey Cragon, Cambridge University Press.
- *Structured Computer Organization* by Andrew Tanenbaum, Prentice Hall.

**Course Website:** Course announcements, lecture notes, handouts, and other material will be posted on the course website at <http://www.ece.cmu.edu/~ece447/>. Please check the course website daily for announcements and handouts.

**Course Blackboard:** To access the course blackboard, go to the login page at: <http://www.cmu.edu/blackboard/>.

**Grading Algorithm:**

14%	Homework + Reading Summaries
40%	Labs
12%	Midterm 1
12%	Midterm 2
22%	Final
5%	Teaching Team's Evaluation of Your Performance (Participation)

We keep grades on Blackboard. Please review your scores periodically. You have one week after a graded item is returned to request a grade correction.

**Homework assignments** are due at the start of class on the date due. **No late homework accepted.** Discussions about homework in small groups are encouraged. However, homeworks must be written up **individually** and **independently**.

**Lab assignments** will be done individually unless otherwise specified.

You can get your labs checked off in any of the recitation sections, regardless of which section you are officially registered in. You will have a total of **five lab late days** for the semester that you may use however you wish to turn in late labs. For example, you could turn in one lab five days late, or you could be one day late on five labs. Weekend days are included in this count.

The TAs are available during recitation sessions to assist you in completing your assignment, but, unlike in 18-240, the length of 18-447 labs and projects are not designed to fit completely within just the recitation hours. You will need to spend a lot of outside time. On the week a lab is due, you should come to a recitation with the milestones completed and ready for check-off. Labs are due on Fridays, unless otherwise specified.

**Recitation sessions** are designed to enhance your understanding of the lecture material, help you with homework assignments, exams, and labs, and get one-on-one help from the TAs on the labs. You can attend any recitation session.

**Compile-Time Course Calendar:**

Please see the course website (<http://www.ece.cmu.edu/~ece447/>) to view the most current schedule and to download lecture notes and handouts. You can view the past schedule and course topics/lectures/videos from Spring 2014 and Spring 2013 at <http://www.ece.cmu.edu/~ece447/s14/doku.php?id=schedule> <http://www.ece.cmu.edu/~ece447/s13/doku.php?id=schedule>

Week	Date	Topic	Readings	Lab	HW
1	1/12	Introduction			HW 0 Out
	1/14			Lab1 Out	HW 1 Out

	1/16				HW 0 Due
2	1/19	No Lecture (MLK Day)			
	1/21			Lab2 Out	
	1/23			Lab1 Due	
3	1/26				
	1/28				HW 1 Due HW 2 Out
	1/30				
4	2/2				
	2/4			Lab 3 Out	
	2/6			Lab 2 Due	
5	2/9				
	2/11				HW 2 Due HW 3 Out
	2/13				
6	2/16				
	2/18			Lab 4 Out	
	2/20			Lab 3 Due	
7	2/23				
	2/25				HW 3 Due HW 4 Out
	2/27				
8	3/2				
	3/4	Midterm 1		Lab 5 Out	
	3/6			Lab 4 Due	
9		No Class (Spring Break)			
10	3/16				
	3/18			Lab 6 out	HW 4 Due HW 5 Out
	3/20			Lab 5 due	
11	3/23				
	3/25				HW 6 Out
	3/27				HW 5 Due
12	3/30				
	4/1			Lab 7 Out	
	4/3			Lab 6 Due	
13	4/6				
	4/8				HW 6 Due HW 7 Out
	4/10	No Class (Spring Carnival)			
14	4/13				
	4/15			Lab 8 Out	
	4/17			Lab 7 Due	
15	4/20				
	4/22	Midterm 2			
	4/24				
16	4/27				
	4/29				HW 7 Due

	5/1	Last Day of Classes		Lab 8 Due	
	TBD	Final Exam			

### **Tentative Topics:**

MIPS ISA, Fundamental Concepts and ISA, ISA Tradeoffs, More ISA Tradeoffs and Single-Cycle Microarchitectures, Single-Cycle Microarchitectures, Multi-Cycle Microarchitectures, Microprogrammed Microarchitectures, Microprogramming and Pipelined Microarchitectures, Pipelining and Related Issues, Data and Control Dependence Handling in Pipelined Microarchitectures, Control Flow Handling, Control Flow and Exceptions, Out-of-Order Execution, Approaches to Concurrency (OoO, DataFlow, Vector, VLIW), Approaches to Concurrency (SIMD and VLIW), Memory Hierarchy and Caches, Caches and Main Memory, Main Memory, Memory Scheduling and Virtual Memory, Virtual Memory, Tolerating Memory Latency, Runahead and Multiprocessing, Multiprocessor Correctness and Cache Coherence, Interconnects, etc.

### **Education Objectives (Relationship of Course to Program Outcomes):**

(a) an ability to apply knowledge of mathematics, science, and engineering: The students will apply classroom knowledge in a series of hands-on lab projects.

(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability: The students will create designs to meet the design specifications of the lab projects.

(d) an ability to function on multi-disciplinary teams: The students are encouraged to collaborate on homework assignments (but write up and submit their own individual solutions).

(e) an ability to identify, formulate, and solve engineering problems: The students will develop original solutions to open-end design specifications in the lab projects.

(f) an understanding of professional and ethical responsibility.

(g) an ability to communicate effectively: The students will provide written reports with each lab project. Interactive discussions planned into the lectures will encourage the students to communicate questions and answers verbally.

(h) a knowledge of contemporary issues: The students will be introduced to contemporary developments and topics in the computer architecture field.

(i) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice: The students will use industry-standard design tools and methodologies in the lab projects.

**Academic Integrity Policy (<http://www.ece.cmu.edu/student/integrity.html>):**

The Department of Electrical and Computer Engineering adheres to the academic integrity policies set forth by Carnegie Mellon University and by the College of Engineering. ECE students should review fully and carefully Carnegie Mellon University's policies regarding *Cheating and Plagiarism*; *Undergraduate Academic Discipline*; and *Graduate Academic Discipline*. ECE graduate students should further review the *Penalties for Graduate Student Academic Integrity Violations* in CIT outlined in the CIT Policy on *Graduate Student Academic Integrity Violations*. In addition to the above university and college-level policies, it is ECE's policy that an ECE graduate student may not drop a course in which a disciplinary action is assessed or pending without the course instructor's explicit approval. Further, an ECE course instructor may set his/her own course-specific academic integrity policies that do not conflict with university and college-level policies; course-specific policies should be made available to the students in writing in the first week of class.

*In 18-447, discussions about homework in small groups are encouraged. However, homeworks must be written up individually and independently. Labs are to be completed individually unless otherwise specified.*

Carnegie Mellon University's Policy on Cheating and Plagiarism (<http://www.cmu.edu/policies/documents/Cheating.html>) states the following,

Students at Carnegie Mellon are engaged in preparation for professional activity of the highest standards. Each profession constrains its members with both ethical responsibilities and disciplinary limits. To assure the validity of the learning experience a university establishes clear standards for student work.

In any presentation, creative, artistic, or research, it is the ethical responsibility of each student to identify the conceptual sources of the work submitted. Failure to do so is dishonest and is the basis for a charge of cheating or plagiarism, which is subject to disciplinary action.

*Cheating* includes but is not necessarily limited to:

1. Plagiarism, explained below.
2. Submission of work that is not the student's own for papers, assignments or exams.
3. Submission or use of falsified data.
4. Theft of or unauthorized access to an exam.
5. Use of an alternate, stand-in or proxy during an examination.
6. Use of unauthorized material including textbooks, notes or computer programs in the preparation of an assignment or during an examination.
7. Supplying or communicating in any way unauthorized information to another student for the preparation of an assignment or during an examination.
8. Collaboration in the preparation of an assignment. Unless specifically permitted or required by the instructor, collaboration will usually be viewed by the university as cheating. Each student, therefore, is responsible for understanding the policies of the department offering any course as they refer to the amount of help and collaboration permitted in preparation of assignments.

9. Submission of the same work for credit in two courses without obtaining the permission of the instructors beforehand.

*Plagiarism* includes, but is not limited to, failure to indicate the source with quotation marks or footnotes where appropriate if any of the following are reproduced in the work submitted by a student:

1. A phrase, written or musical.
2. A graphic element.
3. A proof.
4. Specific language.
5. An idea derived from the work, published or unpublished, of another person.

*This policy applies, in all respects, to 18-447.*