Agenda for Today

- Deep dive into ISA and its tradeoffs
Upcoming Readings

- Next Week (More ISA Tradeoffs + Your Lab + Homework):
  - MIPS ISA Tutorial
  - P&P Chapter 5: LC-3 ISA
  - P&P, revised Appendix A – LC3b ISA

- The Week After (Microarchitecture):
  - P&H, Chapter 4, Sections 4.1-4.4
  - P&P, revised Appendix C – LC3b datapath and microprogrammed operation

- We have provided example critical reviews for you to see, on the course website
Last Lecture Recap

- Levels of Transformation
  - Algorithm, ISA, Microarchitecture
- Moore’s Law
- What is Computer Architecture
- Why Study Computer Architecture
- Fundamental Concepts
- Von Neumann Model
- Dataflow Model
- ISA vs. Microarchitecture

Assignments: HW0 (today!), Lab1 (Jan 23), HW1 (Jan 28)
Review: ISA vs. Microarchitecture

- **ISA**
  - Agreed upon interface between software and hardware
    - SW/compiler assumes, HW promises
  - What the software writer needs to know to write and debug system/user programs

- **Microarchitecture**
  - Specific implementation of an ISA
  - Not visible to the software

- **Microprocessor**
  - **ISA, uarch, circuits**
  - “Architecture” = ISA + microarchitecture
Review: ISA

- Instructions
  - Opcodes, Addressing Modes, Data Types
  - Instruction Types and Formats
  - Registers, Condition Codes

- Memory
  - Address space, Addressability, Alignment
  - Virtual memory management

- Call, Interrupt/Exception Handling

- Access Control, Priority/Privilege

- I/O: memory-mapped vs. instr.

- Task/thread Management

- Power and Thermal Management

- Multi-threading support, Multiprocessor support
Microarchitecture

- Implementation of the ISA under specific design constraints and goals
- Anything done in hardware without exposure to software
  - Pipelining
  - In-order versus out-of-order instruction execution
  - Memory access scheduling policy
  - Speculative execution
  - Superscalar processing (multiple instruction issue?)
  - Clock gating
  - Caching? Levels, size, associativity, replacement policy
  - Prefetching?
  - Voltage/frequency scaling?
  - Error correction?
Property of ISA vs. Uarch?

- ADD instruction’s opcode
- Number of general purpose registers
- Number of ports to the register file
- Number of cycles to execute the MUL instruction
- Whether or not the machine employs pipelined instruction execution

Remember
- Microarchitecture: Implementation of the ISA under specific design constraints and goals
Design Point

- A set of design considerations and their importance
  - leads to tradeoffs in both ISA and uarch

Considerations

- Cost
- Performance
- Maximum power consumption
- Energy consumption (battery life)
- Availability
- Reliability and Correctness
- Time to Market

Design point determined by the “Problem” space (application space), the intended users/market
Application Space

- Dream, and they will appear...

Other examples of the application space that continue to drive the need for unique design points are the following:

1) scientific applications such as those whose computations control nuclear power plants, determine where to drill for oil, and predict the weather;
2) transaction-based applications such as those that handle ATM transfers and e-commerce business;
3) business data processing applications, such as those that handle inventory control, payrolls, IRS activity, and various personnel record keeping, whether the personnel are employees, students, or voters;
4) network applications, such as high-speed routing of Internet packets, that enable the connection of your home system to take advantage of the Internet;
5) guaranteed delivery (a.k.a. real time) applications that require the result of a computation by a certain critical deadline;
6) embedded applications, where the processor is a component of a larger system that is used to solve the (usually) dedicated application;
7) media applications such as those that decode video and audio files;
8) random software packages that desktop users would like to run on their PCs.

Each of these application areas has a very different set of characteristics. Each application area demands a different set of tradeoffs to be made in specifying the microprocessor to do the job.
Tradeoffs: Soul of Computer Architecture

- ISA-level tradeoffs
- Microarchitecture-level tradeoffs
- System and Task-level tradeoffs
  - How to divide the labor between hardware and software

*Computer architecture is the science and art of making the appropriate trade-offs to meet a design point*
  - Why art?
We do not (fully) know the future (applications, users, market)
And, the future is not constant (it changes)!
Analogue from Macro-Architecture

- Future is not constant in macro-architecture, either

- Example: Can a power plant boiler room be later used as a classroom?
At the west end of campus was a small structure that housed the boiler room that functioned as the school’s power plant. Below, in the rain beside the railroad tracks, a farmer’s goat grazed and occasionally wandered up to eat the grass of this yet untamed end of campus.

Over a 20 month period from 1912 - 1914, Machinery Hall was built on top of that boiler room. The massive tower, which has become a symbol of Carnegie Mellon, was designed to disguise the smokestack. Architect Henry Hornbostel had created a “temple of technology” that would become one of the most renowned buildings of the Beaux Arts style in the country.

Early course catalogs described the boiler room as a classroom where students learned about power generating machinery. The tower continued to belch smoke until 1975, but in 1979 the boiler room became the cleanest room on campus with the construction of the Nanofabrication Facility. The coal bin area became the offices and computer room of the D-level.
How Can We Adapt to the Future

- This is part of the task of a good computer architect

- Many options (bag of tricks)
  - Keen insight and good design
  - Good use of fundamentals and principles
    - Efficient design
    - Heterogeneity
    - Reconfigurability
    - ...
  - Good use of the underlying technology
  - ...


ISA Principles and Tradeoffs
Many Different ISAs Over Decades

- x86
- PDP-x: Programmed Data Processor (PDP-11)
- VAX
- IBM 360
- CDC 6600
- SIMD ISAs: CRAY-1, Connection Machine
- VLIW ISAs: Multiflow, Cydrome, IA-64 (EPIC)
- PowerPC, POWER
- RISC ISAs: Alpha, MIPS, SPARC, ARM

What are the fundamental differences?
- E.g., how instructions are specified and what they do
- E.g., how complex are the instructions
Instruction

- Basic element of the HW/SW interface
- Consists of
  - opcode: what the instruction does
  - operands: who it is to do it to

- Example from the Alpha ISA:
### MIPS

<table>
<thead>
<tr>
<th>0</th>
<th>rs</th>
<th>rt</th>
<th>rd</th>
<th>shamt</th>
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#### R-type

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#### I-type

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### Figure 4-1: ARM instruction set formats

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<th>Cond</th>
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<th>Opcode</th>
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<th>Rn</th>
<th>Rd</th>
<th>Operand 2</th>
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<td>Rd</td>
<td>Rn</td>
<td>Rs</td>
<td>1 0 0 1</td>
<td>Rm</td>
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<tr>
<td>Cond</td>
<td>0 0 0 0 1 U A S</td>
<td>RdHi</td>
<td>RdLo</td>
<td>Rn</td>
<td>1 0 0 1</td>
<td>Rm</td>
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<tr>
<td>Cond</td>
<td>0 0 0 1 0 B 0 0</td>
<td>Rn</td>
<td>Rd</td>
<td>0 0 0 1 0 0 1</td>
<td>Rm</td>
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<tr>
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<td>Rn</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cond</td>
<td>0 0 0 P U 0 W L</td>
<td>Rn</td>
<td>Rd</td>
<td>0 0 0 1 S H 1</td>
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<td>Rd</td>
<td>Offset</td>
<td>1 S H 1 Offset</td>
<td></td>
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<td>Rd</td>
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<td>Cond</td>
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</tr>
</tbody>
</table>

**Data Processing / PSR Transfer**

- Multiply
- Multiply Long
- Single Data Swap
- Branch and Exchange
- Halfword Data Transfer: register offset
- Halfword Data Transfer: immediate offset
- Single Data Transfer
- Undefined
- Block Data Transfer
- Branch
- Coprocessor Data Transfer
- Coprocessor Data Operation
- Coprocessor Register Transfer
- Software Interrupt

*Ignored by processor*
Set of Instructions, Encoding, and Spec

- Example from LC-3b ISA
  - [Example link](http://www.ece.utexas.edu/~patt/11s.460N/handouts/new_byte.pdf)
- x86 Manual
- Why unused instructions?
- Aside: concept of “bit steering”
  - A bit in the instruction determines the interpretation of other bits

### Instruction Set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Opcode</th>
<th>Fields</th>
<th>Notes</th>
</tr>
</thead>
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<tr>
<td>ADD*</td>
<td>0001</td>
<td>DR SR1 A</td>
<td>op.spec</td>
</tr>
<tr>
<td>AND*</td>
<td>0101</td>
<td>DR SR1 A</td>
<td>op.spec</td>
</tr>
<tr>
<td>BR</td>
<td>0000</td>
<td>n z p PCoffset19</td>
<td></td>
</tr>
<tr>
<td>JMP</td>
<td>1100</td>
<td>000 BaseR 00000000</td>
<td></td>
</tr>
<tr>
<td>JSR(R)</td>
<td>0100</td>
<td>A operand specifier</td>
<td></td>
</tr>
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<td>LDB*</td>
<td>0010</td>
<td>DR BaseR offset6</td>
<td></td>
</tr>
<tr>
<td>LDW*</td>
<td>0110</td>
<td>DR BaseR offset6</td>
<td></td>
</tr>
<tr>
<td>LEA*</td>
<td>1110</td>
<td>DR PCoffset19</td>
<td></td>
</tr>
<tr>
<td>RTI</td>
<td>1000</td>
<td>000000000000</td>
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<td>1101</td>
<td>DR SR A D amount4</td>
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</tr>
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<td>STB</td>
<td>0011</td>
<td>SR BaseR offset6</td>
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<tr>
<td>STW</td>
<td>0111</td>
<td>SR BaseR offset6</td>
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<td>TRAP</td>
<td>1111</td>
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<tr>
<td>XOR*</td>
<td>1001</td>
<td>DR SR1 A</td>
<td>op.spec</td>
</tr>
</tbody>
</table>

### Not Used
- 1010
- 1011

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22
Bit Steering in Alpha

If bit <12> of the instruction is 0, the Rb field specifies a source register operand.

If bit <12> of the instruction is 1, an 8-bit zero-extended literal constant is formed by bits <20:13> of the instruction. The literal is interpreted as a positive integer between 0 and 255 and is zero-extended to 64 bits. Symbolically, the integer Rbv operand is formed as follows:
What Are the Elements of An ISA?

- **Instruction sequencing model**
  - Control flow vs. data flow
  - Tradeoffs?

- **Instruction processing style**
  - Specifies the number of “operands” an instruction “operates” on and how it does so
  - 0, 1, 2, 3 address machines
    - 0-address: stack machine (op, push A, pop A)
    - 1-address: accumulator machine (op ACC, ld A, st A)
    - 2-address: 2-operand machine (op S,D; one is both source and dest)
    - 3-address: 3-operand machine (op S1,S2,D; source and dest separate)
  - Tradeoffs? See your homework question
    - Larger operate instructions vs. more executed operations
    - Code size vs. execution time vs. on-chip memory space
An Example: Stack Machine

+ Small instruction size (no operands needed for operate instructions)
  - Simpler logic
  - Compact code

+ Efficient procedure calls: all parameters on stack
  - No additional cycles for parameter passing

-- Computations that are not easily expressible with “postfix notation” are difficult to map to stack machines
  - Cannot perform operations on many values at the same time (only top N values on the stack at the same time)
  - Not flexible
An Example: Stack Machine (II)


Figure 3.1 -- The canonical stack machine.
An Example: Stack Machine Operation

http://www.ece.cmu.edu/~koopman/stack_computers/sec3_2.html

Figure 3.2 -- An example stack machine.
Other Examples

- PDP-11: A 2-address machine
  - PDP-11 ADD: 4-bit opcode, 2 6-bit operand specifiers
  - Why? Limited bits to specify an instruction
  - Disadvantage: One source operand is always clobbered with the result of the instruction
    - *How do you ensure you preserve the old value of the source?*

- X86: A 2-address (memory/memory) machine
- Alpha: A 3-address (load/store) machine
- MIPS?
- ARM?
What Are the Elements of An ISA?

- **Instructions**
  - Opcode
  - Operand specifiers (addressing modes)
    - How to obtain the operand?
  - Why are there different addressing modes?

- **Data types**
  - Definition: Representation of information for which there are instructions that operate on the representation
  - Integer, floating point, character, binary, decimal, BCD
  - Doubly linked list, queue, string, bit vector, stack
    - VAX: INSQUEUE and REMQUEUE instructions on a doubly linked list or queue; FINDFIRST
    - X86: SCAN opcode operates on character strings; PUSH/PUSH
Data Type Tradeoffs

- What is the benefit of having more or high-level data types in the ISA?
- What is the disadvantage?

- Think compiler/programmer vs. microarchitect

- Concept of semantic gap
  - Data types coupled tightly to the semantic level, or complexity of instructions

- Example: Early RISC architectures vs. Intel 432
  - Early RISC: Only integer data type
  - Intel 432: Object data type, capability based machine
An Example: BCD

- Each decimal digit is encoded with a fixed number of bits
What Are the Elements of An ISA?

- **Memory organization**
  - Address space: How many uniquely identifiable locations in memory
  - Addressability: How much data does each uniquely identifiable location store
    - Byte addressable: most ISAs, characters are 8 bits
    - Bit addressable: Burroughs 1700. Why?
    - 64-bit addressable: Some supercomputers. Why?
    - 32-bit addressable: First Alpha
  - Food for thought
    - How do you add 2 32-bit numbers with only byte addressability?
    - How do you add 2 8-bit numbers with only 32-bit addressability?
    - **Big endian vs. little endian?** MSB at low or high byte.

- Support for virtual memory
Some Historical Readings

- If you want to dig deeper
What Are the Elements of An ISA?

- **Registers**
  - How many
  - Size of each register

- **Why is having registers a good idea?**
  - Because programs exhibit a characteristic called *data locality*
  - A recently produced/accessed value is likely to be used more than once (temporal locality)
    - Storing that value in a register eliminates the need to go to memory each time that value is needed
Programmer Visible (Architectural) State

|------|------|------|------|------|--------|

Memory
array of storage locations
indexed by an address

Registers
- given special names in the ISA
  (as opposed to addresses)
- general vs. special purpose

Program Counter
memory address
of the current instruction

Instructions (and programs) specify how to transform
the values of programmer visible state
Aside: Programmer Invisible State

- Microarchitectural state
- Programmer cannot access this directly

- E.g. cache state
- E.g. pipeline registers
Evolution of Register Architecture

- **Accumulator**
  - a legacy from the “adding” machine days

- **Accumulator + address registers**
  - need register indirection
  - initially address registers were special-purpose, i.e., can only be loaded with an address for indirection
  - eventually arithmetic on addresses became supported

- **General purpose registers (GPR)**
  - all registers good for all purposes
  - grew from a few registers to 32 (common for RISC) to 128 in Intel IA-64
Instruction Classes

- Operate instructions
  - Process data: arithmetic and logical operations
  - Fetch operands, compute result, store result
  - Implicit sequential control flow

- Data movement instructions
  - Move data between memory, registers, I/O devices
  - Implicit sequential control flow

- Control flow instructions
  - Change the sequence of instructions that are executed
What Are the Elements of An ISA?

- **Load/store vs. memory/memory architectures**
  - **Load/store architecture**: operate instructions operate only on registers
    - E.g., MIPS, ARM and many RISC ISAs
  - **Memory/memory architecture**: operate instructions can operate on memory locations
    - E.g., x86, VAX and many CISC ISAs
What Are the Elements of An ISA?

- **Addressing modes** specify how to obtain the operands
  - **Absolute**: \( \text{LW rt, 10000} \)
    use immediate value as address
  - **Register Indirect**: \( \text{LW rt, } (r_{\text{base}}) \)
    use \( GPR[r_{\text{base}}] \) as address
  - **Displaced or based**: \( \text{LW rt, } \text{offset}(r_{\text{base}}) \)
    use offset+\( GPR[r_{\text{base}}] \) as address
  - **Indexed**: \( \text{LW rt, } (r_{\text{base}}, r_{\text{index}}) \)
    use \( GPR[r_{\text{base}}]+GPR[r_{\text{index}}] \) as address
  - **Memory Indirect**: \( \text{LW rt, } ((r_{\text{base}})) \)
    use value at \( M[GPR[r_{\text{base}}]] \) as address
  - **Auto inc/decrement**: \( \text{LW Rt, } (r_{\text{base}}) \)
    use \( GPR[r_{\text{base}}] \) as address, but inc. or dec. \( GPR[r_{\text{base}}] \) each time
What Are the Benefits of Different Addressing Modes?

- Another example of programmer vs. microarchitect tradeoff

- Advantage of more addressing modes:
  - Enables better mapping of high-level constructs to the machine: some accesses are better expressed with a different mode → reduced number of instructions and code size
    - Think array accesses (autoincrement mode)
    - Think indirection (pointer chasing)
    - Sparse matrix accesses

- Disadvantage:
  - More work for the compiler
  - More work for the microarchitect
ISA Orthogonality

- Orthogonal ISA:
  - All addressing modes can be used with all instruction types
  - Example: VAX
    - (~13 addressing modes) x (>300 opcodes) x (integer and FP formats)

- Who is this good for?
- Who is this bad for?
Is the LC-3b ISA Orthogonal?
LC-3b: Addressing Modes of ADD

### Encodings

![Diagram showing encodings for ADD modes](image)

### Operation

```c
if (bit[5] == 0)
    DR = SR1 + SR2;
else
    DR = SR1 + SEXT(imm5);
setcc();
```
LC-3b: Addressing Modes of JSR(R)

**Encodings**

For JSR:
- Bit 15: 0100
- Bit 11: 1
- Bit 10 to 0: PC offset 11

For JSRR:
- Bit 15: 0100
- Bit 10 to 8: 00
- Bit 6 to 0: BaseR
- Bit 0: 000000

**Operation**

```plaintext
R7 = PC;
if (bit[11] == 0)
    PC = BaseR;
else
    PC = PC + LSHF(SEXT(PC offset 11), 1);
```

**Description**

First, the incremented PC is saved in R7. This is the linkage back to the calling routine. Then, the PC is loaded with the address of the first instruction of the subroutine, causing an unconditional jump to that address. The address of the subroutine is obtained from the base register (if bit[11] is 0), or the address is computed by sign-extending bits [10:0] to 16 bits, left-shifting the result one bit, and then adding this value to the incremented PC (if bit[11] is 1).
What Are the Elements of An ISA?

- How to interface with I/O devices
  - Memory mapped I/O
    - A region of memory is mapped to I/O devices
    - I/O operations are loads and stores to those locations
  - Special I/O instructions
    - IN and OUT instructions in x86 deal with ports of the chip
- Tradeoffs?
  - Which one is more general purpose?
What Are the Elements of An ISA?

- **Privilege modes**
  - User vs supervisor
  - Who can execute what instructions?

- **Exception and interrupt handling**
  - What procedure is followed when something goes wrong with an instruction?
  - What procedure is followed when an external device requests the processor?
  - Vectored vs. non-vectored interrupts (early MIPS)

- **Virtual memory**
  - Each program has the illusion of the entire memory space, which is greater than physical memory

- **Access protection**

- **We will talk about these later**
Another Question or Two

- Does the LC-3b ISA contain complex instructions?
- How complex can an instruction be?
Complex vs. Simple Instructions

- **Complex instruction:** An instruction does a lot of work, e.g. many operations
  - Insert in a doubly linked list
  - Compute FFT
  - String copy

- **Simple instruction:** An instruction does small amount of work, it is a primitive using which complex operations can be built
  - Add
  - XOR
  - Multiply
Complex vs. Simple Instructions

- Advantages of Complex instructions
  + Denser encoding → smaller code size → better memory utilization, saves off-chip bandwidth, better cache hit rate (better packing of instructions)
  + Simpler compiler: no need to optimize small instructions as much

- Disadvantages of Complex Instructions
  - Larger chunks of work → compiler has less opportunity to optimize (limited in fine-grained optimizations it can do)
  - More complex hardware → translation from a high level to control signals and optimization needs to be done by hardware
ISA-level Tradeoffs: Semantic Gap

- **Where to place the ISA?** Semantic gap
  - Closer to high-level language (HLL) → Small semantic gap, complex instructions
  - Closer to hardware control signals? → Large semantic gap, simple instructions

- **RISC vs. CISC machines**
  - RISC: Reduced instruction set computer
  - CISC: Complex instruction set computer
    - FFT, QUICKSORT, POLY, FP instructions?
    - VAX INDEX instruction (array access with bounds checking)
ISA-level Tradeoffs: Semantic Gap

- Some tradeoffs (for you to think about)

- Simple compiler, complex hardware vs. complex compiler, simple hardware
  - Caveat: Translation (indirection) can change the tradeoff!

- Burden of backward compatibility

- Performance? Energy Consumption?
  - Optimization opportunity: Example of VAX INDEX instruction: who (compiler vs. hardware) puts more effort into optimization?
  - Instruction size, code size
An instruction operates on a string
- Move one string of arbitrary length to another location
- Compare two strings

Enabled by the ability to specify repeated execution of an instruction (in the ISA)
- Using a “prefix” called REP prefix

Example: REP MOVES instruction
- Only two bytes: REP prefix byte and MOVES opcode byte (F2 A4)
- Implicit source and destination registers pointing to the two strings (ESI, EDI)
- Implicit count register (ECX) specifies how long the string is
X86: Small Semantic Gap: String Operations

REP MOVES (DEST SRC)

IF AddressSize = 16
    THEN
        Use CX for CountReg;
    ELSE IF AddressSize = 64 and REX.W used
        THEN Use RCX for CountReg; F1;
    ELSE
        Use ECX for CountReg;
    F1;
WHILE CountReg ≠ 0
    DO
        Service pending interrupts (if any);
        Execute associated string instruction;
        CountReg ← (CountReg - 1);
        IF CountReg = 0
            THEN exit WHILE loop; F1;
        IF (Repeat prefix is REPZ or REPE) and (ZF = 0)
            or (Repeat prefix is REPNZ or REPNE) and (ZF = 1)
                THEN exit WHILE loop; F1;
    OD;

How many instructions does this take in MIPS?
Small Semantic Gap Examples in VAX

- **FIND FIRST**
  - Find the first set bit in a bit field
  - Helps OS resource allocation operations

- **SAVE CONTEXT, LOAD CONTEXT**
  - Special context switching instructions

- **INSQUEUE, REMQUEUE**
  - Operations on doubly linked list

- **INDEX**
  - Array access with bounds checking

- **STRING Operations**
  - Compare strings, find substrings, ...

- **Cyclic Redundancy Check Instruction**

- **EDITPC**
  - Implements editing functions to display fixed format output

CISC vs. RISC
- Complex instruction set computer $\rightarrow$ complex instructions
  - Initially motivated by “not good enough” code generation
- Reduced instruction set computer $\rightarrow$ simple instructions
  - John Cocke, mid 1970s, IBM 801
  - Goal: enable better compiler control and optimization

RISC motivated by
- Memory stalls (no work done in a complex instruction when there is a memory stall?)
  - When is this correct?
- Simplifying the hardware $\rightarrow$ lower cost, higher frequency
- Enabling the compiler to optimize the code better
  - Find fine-grained parallelism to reduce stalls
An Aside

- An Historical Perspective on RISC Development at IBM
How High or Low Can You Go?

- **Very large semantic gap**
  - Each instruction specifies the complete set of control signals in the machine
  - Compiler generates control signals
  - Open microcode (John Cocke, circa 1970s)
    - Gave way to optimizing compilers

- **Very small semantic gap**
  - ISA is (almost) the same as high-level language
  - Java machines, LISP machines, object-oriented machines, capability-based machines
A Note on ISA Evolution

- ISAs have evolved to reflect/satisfy the concerns of the day

- Examples:
  - Limited on-chip and off-chip memory size
  - Limited compiler optimization technology
  - Limited memory bandwidth
  - Need for specialization in important applications (e.g., MMX)

- Use of translation (in HW and SW) enabled underlying implementations to be similar, regardless of the ISA
  - Concept of dynamic/static interface: translation/interpretation
  - Contrast it with hardware/software interface
Effect of Translation

- One can translate from one ISA to another ISA to change the semantic gap tradeoffs
  - ISA (virtual ISA) → Implementation ISA

Examples

- Intel’s and AMD’s x86 implementations translate x86 instructions into programmer-invisible microoperations (simple instructions) in hardware
- Transmeta’s x86 implementations translated x86 instructions into “secret” VLIW instructions in software (code morphing software)

Think about the tradeoffs
Hardware-Based Translation

**Figure 2.** Conventional superscalar out-of-order CPUs use hardware to create and dispatch micro-ops that can execute in parallel.

Software-Based Translation

Figure 5. The Code Morphing software mediates between x86 software and the Crusoe processor.

We did not cover the following slides in lecture. These are for your preparation for the next lecture.
ISA-level Tradeoffs: Instruction Length

**Fixed length:** Length of all instructions the same

- Easier to decode single instruction in hardware
- Easier to decode multiple instructions concurrently
- Wasted bits in instructions *(Why is this bad?)*
- Harder-to-extend ISA (how to add new instructions?)

**Variable length:** Length of instructions different (determined by opcode and sub-opcode)

- Compact encoding *(Why is this good?)*
  - Intel 432: Huffman encoding (sort of). 6 to 321 bit instructions. *How?*
- More logic to decode a single instruction
- Harder to decode multiple instructions concurrently

**Tradeoffs**

- Code size (memory space, bandwidth, latency) vs. hardware complexity
- ISA extensibility and expressiveness vs. hardware complexity
- Performance? Smaller code vs. ease of decode
Uniform decode: Same bits in each instruction correspond to the same meaning
- Opcode is always in the same location
- Ditto operand specifiers, immediate values, ...
- Many “RISC” ISAs: Alpha, MIPS, SPARC
  + Easier decode, simpler hardware
  + Enables parallelism: generate target address before knowing the instruction is a branch
  -- Restricts instruction format (fewer instructions?) or wastes space

Non-uniform decode
- E.g., opcode can be the 1st-7th byte in x86
  + More compact and powerful instruction format
  -- More complex decode logic
x86 vs. Alpha Instruction Formats

x86:

<table>
<thead>
<tr>
<th>Instruction Prefixes</th>
<th>Opcode</th>
<th>ModR/M</th>
<th>SIB</th>
<th>Displacement</th>
<th>Immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Up to four prefixes of 1 byte each (optional)</td>
<td>1-, 2-, or 3-byte opcode</td>
<td>1 byte (if required)</td>
<td>1 byte (if required)</td>
<td>Address displacement of 1, 2, or 4 bytes or none</td>
<td>Immediate data of 1, 2, or 4 bytes or none</td>
</tr>
</tbody>
</table>

Alpha:

<table>
<thead>
<tr>
<th>PALcode Format</th>
<th>Branch Format</th>
<th>Memory Format</th>
<th>Operate Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opcode</td>
<td>Number</td>
<td>Opcode</td>
<td>RA</td>
</tr>
<tr>
<td>Opcode</td>
<td>RA</td>
<td>RB</td>
<td>Function</td>
</tr>
</tbody>
</table>
MIPS Instruction Format

- R-type, 3 register operands

<table>
<thead>
<tr>
<th>0</th>
<th>rs</th>
<th>rt</th>
<th>rd</th>
<th>shamt</th>
<th>funct</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-bit</td>
<td>5-bit</td>
<td>5-bit</td>
<td>5-bit</td>
<td>5-bit</td>
<td>6-bit</td>
</tr>
</tbody>
</table>

- I-type, 2 register operands and 16-bit immediate operand

<table>
<thead>
<tr>
<th>opcode</th>
<th>rs</th>
<th>rt</th>
<th>immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-bit</td>
<td>5-bit</td>
<td>5-bit</td>
<td>16-bit</td>
</tr>
</tbody>
</table>

- J-type, 26-bit immediate operand

<table>
<thead>
<tr>
<th>opcode</th>
<th>immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-bit</td>
<td>26-bit</td>
</tr>
</tbody>
</table>

- Simple Decoding
  - 4 bytes per instruction, regardless of format
  - must be 4-byte aligned (2 lsb of PC must be 2b’00)
  - format and fields easy to extract in hardware
Figure 4-1: ARM instruction set formats
A Note on Length and Uniformity

- Uniform decode usually goes with fixed length

- In a variable length ISA, uniform decode can be a property of instructions of the same length
  - It is hard to think of it as a property of instructions of different lengths
A Note on RISC vs. CISC

- Usually, ...

- RISC
  - Simple instructions
  - Fixed length
  - Uniform decode
  - Few addressing modes

- CISC
  - Complex instructions
  - Variable length
  - Non-uniform decode
  - Many addressing modes
ISA-level Tradeoffs: Number of Registers

- **Affects:**
  - Number of bits used for encoding register address
  - Number of values kept in fast storage (register file)
  - (uarch) Size, access time, power consumption of register file

- **Large number of registers:**
  + Enables better register allocation (and optimizations) by compiler → fewer saves/restores
  -- Larger instruction size
  -- Larger register file size
ISA-level Tradeoffs: Addressing Modes

- Addressing mode specifies how to obtain an operand of an instruction
  - Register
  - Immediate
  - Memory (displacement, register indirect, indexed, absolute, memory indirect, autoincrement, autodecrement, ...)

- More modes:
  + help better support programming constructs (arrays, pointer-based accesses)
  -- make it harder for the architect to design
  -- too many choices for the compiler?
    - Many ways to do the same thing complicates compiler design
x86 vs. Alpha Instruction Formats

- x86:

  ![x86 Instruction Formats Diagram]

- Alpha:

  ![Alpha Instruction Formats Diagram]
### x86

**Table 2-2. 32-Bit Addressing Forms with the ModR/M Byte**

<table>
<thead>
<tr>
<th>Effective Address</th>
<th>Mod</th>
<th>R/M</th>
<th>Value of ModR/M Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[EAX]</td>
<td>00</td>
<td>00</td>
<td>00 0B 18 20 28 30 38</td>
</tr>
<tr>
<td>[ECX]</td>
<td>00</td>
<td>01</td>
<td>01 09 11 19 21 29 31 39</td>
</tr>
<tr>
<td>[EDX]</td>
<td>01</td>
<td>02</td>
<td>02 0A 12 1A 22 2A 32 3A</td>
</tr>
<tr>
<td>[EBX]</td>
<td>01</td>
<td>03</td>
<td>03 0B 13 1B 23 2B 33 3B</td>
</tr>
<tr>
<td>[-][-]disp8</td>
<td>01</td>
<td>04</td>
<td>04 0C 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>[ESI]</td>
<td>01</td>
<td>05</td>
<td>05 0D 15 1D 25 2D 35 3D</td>
</tr>
<tr>
<td>[EDI]</td>
<td>01</td>
<td>06</td>
<td>06 0E 16 1E 26 2E 36 3E</td>
</tr>
<tr>
<td>[EAX]+disp8</td>
<td>01</td>
<td>07</td>
<td>07 0F 17 1F 27 2F 37 3F</td>
</tr>
<tr>
<td>[ECX]+disp8</td>
<td>01</td>
<td>08</td>
<td>08 10 18 20 28 30 38</td>
</tr>
<tr>
<td>[EDX]+disp8</td>
<td>01</td>
<td>09</td>
<td>09 11 19 21 29 31 39</td>
</tr>
<tr>
<td>[EBX]+disp8</td>
<td>01</td>
<td>0A</td>
<td>0A 12 1B 22 2A 3A 3B</td>
</tr>
<tr>
<td>[-][-]disp32</td>
<td>01</td>
<td>0B</td>
<td>0B 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>[ESI]+disp8</td>
<td>01</td>
<td>0C</td>
<td>0C 16 1E 26 2E 36 3E</td>
</tr>
<tr>
<td>[EDI]+disp8</td>
<td>01</td>
<td>0D</td>
<td>0D 18 1F 28 2F 38 3F</td>
</tr>
<tr>
<td>[EAX]+disp32</td>
<td>01</td>
<td>0E</td>
<td>0E 10 18 20 28 30 38</td>
</tr>
<tr>
<td>[ECX]+disp32</td>
<td>01</td>
<td>0F</td>
<td>0F 11 19 21 29 31 39</td>
</tr>
<tr>
<td>[EDX]+disp32</td>
<td>01</td>
<td>10</td>
<td>10 12 1A 22 2A 32 3A</td>
</tr>
<tr>
<td>[EBX]+disp32</td>
<td>01</td>
<td>11</td>
<td>11 13 1B 23 2B 33 3B</td>
</tr>
<tr>
<td>[-][-]disp32</td>
<td>01</td>
<td>12</td>
<td>12 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>[ESI]+disp32</td>
<td>01</td>
<td>13</td>
<td>13 16 1E 26 2E 36 3E</td>
</tr>
<tr>
<td>[EDI]+disp32</td>
<td>01</td>
<td>14</td>
<td>14 18 1F 28 2F 38 3F</td>
</tr>
</tbody>
</table>

**NOTES:**

1. The [-][-] nomenclature means a SIB follows the ModR/M byte.
2. The disp32 nomenclature denotes a 32-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is added to the index.
3. The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is sign-extended and added to the index.

Table 2-3 is organized to give 256 possible values of the SIB byte (in hexadecimal). General purpose registers used as a base are indicated across the top of the table.
## Table 2.3. 32-Bit Addressing Forms with the SIB Byte

<table>
<thead>
<tr>
<th>Scaled Index</th>
<th>SS Index</th>
<th>Value of SIB Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[EAX] 000</td>
<td>000</td>
<td>00 01 02 03 04 05 06 07</td>
</tr>
<tr>
<td>[ECX] 001</td>
<td>001</td>
<td>08 09 0A 0B 0C 0D 0E 0F</td>
</tr>
<tr>
<td>[EDX] 010</td>
<td>010</td>
<td>10 11 12 13 14 15 16 17</td>
</tr>
<tr>
<td>[EBX] 011</td>
<td>011</td>
<td>18 19 1A 1B 1C 1D 1E 1F</td>
</tr>
<tr>
<td>none 100</td>
<td>100</td>
<td>20 21 22 23 24 25 26 27</td>
</tr>
<tr>
<td>[EBP] 101</td>
<td>101</td>
<td>28 29 2A 2B 2C 2D 2E 2F</td>
</tr>
<tr>
<td>[ESI] 110</td>
<td>110</td>
<td>30 31 32 33 34 35 36 37</td>
</tr>
<tr>
<td>[EDI] 111</td>
<td>111</td>
<td>38 39 3A 3B 3C 3D 3E 3F</td>
</tr>
<tr>
<td>[EAX+2] 000</td>
<td>000</td>
<td>40 41 42 43 44 45 46 47</td>
</tr>
<tr>
<td>[ECX+2] 001</td>
<td>001</td>
<td>48 49 4A 4B 4C 4D 4E 4F</td>
</tr>
<tr>
<td>[EDX+2] 010</td>
<td>010</td>
<td>50 51 52 53 54 55 56 57</td>
</tr>
<tr>
<td>[EBX+2] 011</td>
<td>011</td>
<td>58 59 5A 5B 5C 5D 5E 5F</td>
</tr>
<tr>
<td>none 100</td>
<td>100</td>
<td>60 61 62 63 64 65 66 67</td>
</tr>
<tr>
<td>[EBP+2] 101</td>
<td>101</td>
<td>68 69 6A 6B 6C 6D 6E 6F</td>
</tr>
<tr>
<td>[ESI+2] 110</td>
<td>110</td>
<td>70 71 72 73 74 75 76 77</td>
</tr>
<tr>
<td>[EDI+2] 111</td>
<td>111</td>
<td>78 79 7A 7B 7C 7D 7E 7F</td>
</tr>
<tr>
<td>[EAX+4] 100</td>
<td>100</td>
<td>80 81 82 83 84 85 86 87</td>
</tr>
<tr>
<td>[ECX+4] 101</td>
<td>101</td>
<td>88 89 8A 8B 8C 8D 8E 8F</td>
</tr>
<tr>
<td>[EDX+4] 110</td>
<td>110</td>
<td>90 91 92 93 94 95 96 97</td>
</tr>
<tr>
<td>none 100</td>
<td>100</td>
<td>A0 A1 A2 A3 A4 A5 A6 A7</td>
</tr>
<tr>
<td>[EBP+4] 101</td>
<td>101</td>
<td>A8 A9 AA AB AC AD AE AF</td>
</tr>
<tr>
<td>[ESI+4] 110</td>
<td>110</td>
<td>B0 B1 B2 B3 B4 B5 B6 B7</td>
</tr>
<tr>
<td>[EDI+4] 111</td>
<td>111</td>
<td>B8 B9 BA BB BC BD BE BF</td>
</tr>
<tr>
<td>[EAX+8] 110</td>
<td>110</td>
<td>C0 C1 C2 C3 C4 C5 C6 C7</td>
</tr>
<tr>
<td>[ECX+8] 111</td>
<td>111</td>
<td>C8 C9 CA CB CC CD CE CF</td>
</tr>
<tr>
<td>[EDX+8] 110</td>
<td>110</td>
<td>D0 D1 D2 D3 D4 D5 D6 D7</td>
</tr>
<tr>
<td>[EBX+8] 111</td>
<td>111</td>
<td>D8 D9 DA DC DD DE DF</td>
</tr>
<tr>
<td>none 100</td>
<td>100</td>
<td>E0 E1 E2 E3 E4 E5 E6 E7</td>
</tr>
<tr>
<td>[EBP+8] 110</td>
<td>110</td>
<td>E8 EA EB EC ED EE EF</td>
</tr>
<tr>
<td>[ESI+8] 111</td>
<td>111</td>
<td>F0 F1 F2 F3 F4 F5 F6 F7</td>
</tr>
<tr>
<td>[EDI+8] 111</td>
<td>111</td>
<td>F8 F9 FA FB FC FD FE FF</td>
</tr>
</tbody>
</table>

### NOTES:
1. The [*] nomenclature means a disp32 with no base if the MOD is 00B. Otherwise, [*] means disp8 or disp32 + [EBP]. This provides the following address modes:

<table>
<thead>
<tr>
<th>MOD bits</th>
<th>Effective Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>[scaled index] + disp32</td>
</tr>
<tr>
<td>01</td>
<td>[scaled index] + disp8 + [EBP]</td>
</tr>
<tr>
<td>10</td>
<td>[scaled index] + disp32 + [EBP]</td>
</tr>
</tbody>
</table>
X86 SIB-D Addressing Mode

![Diagram of X86 SIB-D Addressing Mode](image)

**Figure 3-11. Offset (or Effective Address) Computation**

Offset = Base + (Index * Scale) + Displacement

---

x86 Manual Vol. 1, page 3-22 -- see course resources on website
Also, see Section 3.7.3 and 3.7.5
The following addressing modes suggest uses for common combinations of address components.

- **Displacement** — A displacement alone represents a direct (uncomputed) offset to the operand. Because the displacement is encoded in the instruction, this form of an address is sometimes called an absolute or static address. It is commonly used to access a statically allocated scalar operand.

- **Base** — A base alone represents an indirect offset to the operand. Since the value in the base register can change, it can be used for dynamic storage of variables and data structures.

- **Base + Displacement** — A base register and a displacement can be used together for two distinct purposes:
  - As an index into an array when the element size is not 2, 4, or 8 bytes—The displacement component encodes the static offset to the beginning of the array. The base register holds the results of a calculation to determine the offset to a specific element within the array.
  - To access a field of a record: the base register holds the address of the beginning of the record, while the displacement is a static offset to the field.

An important special case of this combination is access to parameters in a procedure activation record. A procedure activation record is the stack frame created when a procedure is entered. Here, the EBP register is the best choice for the base register, because it automatically selects the stack segment. This is a compact encoding for this common function.
(Index * Scale) + Displacement — This address mode offers an efficient way to index into a static array when the element size is 2, 4, or 8 bytes. The displacement locates the beginning of the array, the index register holds the subscript of the desired array element, and the processor automatically converts the subscript into an index by applying the scaling factor.

Base + Index + Displacement — Using two registers together supports either a two-dimensional array (the displacement holds the address of the beginning of the array) or one of several instances of an array of records (the displacement is an offset to a field within the record).

Base + (Index * Scale) + Displacement — Using all the addressing components together allows efficient indexing of a two-dimensional array when the elements of the array are 2, 4, or 8 bytes in size.
Other Example ISA-level Tradeoffs

- Condition codes vs. not
- VLIW vs. single instruction
- Precise vs. imprecise exceptions
- Virtual memory vs. not
- Unaligned access vs. not
- Hardware interlocks vs. software-guaranteed interlocking
- Software vs. hardware managed page fault handling
- Cache coherence (hardware vs. software)
- ...

...
Back to Programmer vs. (Micro)architect

- Many ISA features designed to aid programmers
- But, complicate the hardware designer’s job

- Virtual memory
  - vs. overlay programming
  - Should the programmer be concerned about the size of code blocks fitting physical memory?

- Addressing modes

- Unaligned memory access
  - Compile/programmer needs to align data
MIPS: Aligned Access

- LW/SW alignment restriction: 4-byte word-alignment
  - not designed to fetch memory bytes not within a word boundary
  - not designed to rotate unaligned bytes into registers
- Provide separate opcodes for the “infrequent” case

- LWL/LWR is slower
- Note LWL and LWR still fetch within word boundary
X86: Unaligned Access

- LD/ST instructions automatically align data that spans a “word” boundary
- Programmer/compiler does not need to worry about where data is stored (whether or not in a word-aligned location)

4.1.1 Alignment of Words, Doublewords, Quadwords, and Double Quadwords

Words, doublewords, and quadwords do not need to be aligned in memory on natural boundaries. The natural boundaries for words, double words, and quadwords are even-numbered addresses, addresses evenly divisible by four, and addresses evenly divisible by eight, respectively. However, to improve the performance of programs, data structures (especially stacks) should be aligned on natural boundaries whenever possible. The reason for this is that the processor requires two memory accesses to make an unaligned memory access; aligned accesses require only one memory access. A word or doubleword operand that crosses a 4-byte boundary or a quadword operand that crosses an 8-byte boundary is considered unaligned and requires two separate memory bus cycles for access.
X86: Unaligned Access
What About ARM?

- [https://www.scss.tcd.ie/~waldroj/3d1/arm_arm.pdf](https://www.scss.tcd.ie/~waldroj/3d1/arm_arm.pdf)
  - Section A2.8
Aligned vs. Unaligned Access

- Pros of having no restrictions on alignment

- Cons of having no restrictions on alignment

- Filling in the above: an exercise for you...