Lecture 10: Branch Handling and Branch Prediction (II)

Prof. Onur Mutlu
Carnegie Mellon University
Spring 2014, 2/5/2014
Announcements

- No office hours today for me

- Review Session and Recitation Friday during lecture – please bring questions and problems

- Homework 1 and Lab 1 grades posted

- Lab 2 due this Friday (Feb 7)
  - Do not forget the extra credit!
  - Suggestion: Be frugal with your late days

- Homework 2 due next Wednesday (Feb 12)

- Lab 3 available online (due Feb 21)
Readings for Next Few Lectures (I)

- P&H Chapter 4.9-4.11
  - More advanced pipelining
  - Interrupt and exception handling
  - Out-of-order and superscalar execution concepts
Review: More Sophisticated Direction Prediction

- Compile time (static)
  - Always not taken
  - Always taken
  - BTFN (Backward taken, forward not taken)
  - Profile based (likely direction)
  - Program analysis based (likely direction)

- Run time (dynamic)
  - Last time prediction (single-bit)
  - Two-bit counter based prediction
  - Two-level prediction (global vs. local)
  - Hybrid
Review: Importance of The Branch Problem

- Assume a 5-wide *superscalar* pipeline with 20-cycle branch resolution latency

- How long does it take to fetch 500 instructions?
  - Assume 1 out of 5 instructions is a branch
  - 100% accuracy
    - 100 cycles (all instructions fetched on the correct path)
    - No wasted work
  - 99% accuracy
    - 100 (correct path) + 20 (wrong path) = 120 cycles
    - 20% extra instructions fetched
  - 98% accuracy
    - 100 (correct path) + 20 * 2 (wrong path) = 140 cycles
    - 40% extra instructions fetched
  - 95% accuracy
    - 100 (correct path) + 20 * 5 (wrong path) = 200 cycles
    - 100% extra instructions fetched
Can We Do Better?

- Last-time and 2BC predictors exploit only “last-time” predictability for a given branch

Realization 1: A branch’s outcome can be correlated with other branches’ outcomes
  - Global branch correlation

Realization 2: A branch’s outcome can be correlated with past outcomes of the same branch (in addition to the outcome of the branch “last-time” it was executed)
  - Local branch correlation
Global Branch Correlation (I)

- Recently executed branch outcomes in the execution path is correlated with the outcome of the next branch

    if (cond1)
    ...
    if (cond1 AND cond2)

- If first branch not taken, second also not taken

    branch Y: if (cond1) a = 2;
    ...
    branch X: if (a == 0)

- If first branch taken, second definitely not taken
Global Branch Correlation (II)

branch Y: if (cond1)
...
branch Z: if (cond2)
...
branch X: if (cond1 AND cond2)

- If Y and Z both taken, then X also taken
- If Y or Z not taken, then X also not taken
Global Branch Correlation (III)

- Eqntott, SPEC 1992

```c
if (aa==2) ;; B1
    aa=0;
if (bb==2) ;; B2
    bb=0;
if (aa!=bb) {
    ;; B3
    ....
}
```

If B1 is not taken (i.e., aa==0@B3) and B2 is not taken (i.e. bb=0@B3) then B3 is certainly taken.
Capturing Global Branch Correlation

- Idea: Associate branch outcomes with “global T/NT history” of all branches
- Make a prediction based on the outcome of the branch the last time the same global branch history was encountered

Implementation:
- Keep track of the “global T/NT history” of all branches in a register → Global History Register (GHR)
- Use GHR to index into a table that recorded the outcome that was seen for each GHR value in the recent past → Pattern History Table (table of 2-bit counters)

Global history/branch predictor
- Uses two levels of history (GHR + history at that GHR)
Two Level Global Branch Prediction

- **First level**: Global branch history register (N bits)
  - The direction of last N branches
- **Second level**: Table of saturating counters for each history entry
  - The direction the branch took the last time the same history was seen

How Does the Global Predictor Work?

Intel Pentium Pro Branch Predictor

- 4-bit global history register
- Multiple pattern history tables (of 2 bit counters)
  - Which pattern history table to use is determined by lower order bits of the branch address
Improving Global Predictor Accuracy

- Idea: Add more context information to the global predictor to take into account which branch is being predicted
  - **Gshare predictor**: GHR hashed with the Branch PC
    + More context information
    + Better utilization of PHT
    -- Increases access latency

Review: One-Level Branch Predictor

Direction predictor (2-bit counters)

Program Counter

Address of the current instruction

Cache of Target Addresses (BTB: Branch Target Buffer)

Next Fetch Address

PC + inst size

hit?

taken?
Two-Level Global History Branch Predictor

- Which direction earlier branches went
- Global branch history
- Program Counter
- Address of the current instruction
- Direction predictor (2-bit counters)
- Cache of Target Addresses (BTB: Branch Target Buffer)
- Next Fetch Address

Which direction earlier branches went
Global branch history
Program Counter
Address of the current instruction
Direction predictor (2-bit counters)
Next Fetch Address
Cache of Target Addresses (BTB: Branch Target Buffer)

PC + inst size

hit?
taken?
Two-Level Gshare Branch Predictor

Which direction earlier branches went

Global branch history

Program Counter

Address of the current instruction

Direction predictor (2-bit counters)

XOR

taken?

PC + inst size

hit?

Next Fetch Address

target address

Cache of Target Addresses (BTB: Branch Target Buffer)
Can We Do Better?

- Last-time and 2BC predictors exploit only “last-time” predictability for a given branch

- Realization 1: A branch’s outcome can be correlated with other branches’ outcomes
  - Global branch correlation

- Realization 2: A branch’s outcome can be correlated with past outcomes of the same branch (in addition to the outcome of the branch “last-time” it was executed)
  - Local branch correlation
Local Branch Correlation

```c
for (i=1; i<=4; i++) { }
```

If the loop test is done at the end of the body, the corresponding branch will execute the pattern $(1110)^n$, where 1 and 0 represent taken and not taken respectively, and $n$ is the number of times the loop is executed. Clearly, if we knew the direction this branch had gone on the previous three executions, then we could always be able to predict the next branch direction.

Capturing Local Branch Correlation

- **Idea:** Have a per-branch history register
  - Associate the predicted outcome of a branch with “T/NT history” of the same branch
- Make a prediction based on the outcome of the branch the last time the same local branch history was encountered

- Called the local history/branch predictor
- Uses two levels of history (Per-branch history register + history at that history register value)
Two Level Local Branch Prediction

- First level: A set of local history registers (N bits each)
  - Select the history register based on the PC of the branch
- Second level: Table of saturating counters for each history entry
  - The direction the branch took the last time the same history was seen

Pattern History Table (PHT)

Two-Level Local History Branch Predictor

Which directions earlier instances of *this branch* went

Direction predictor (2-bit counters)

Program Counter

Address of the current instruction

Cache of Target Addresses (BTB: Branch Target Buffer)

Next Fetch Address

Next Fetch Address

PC + inst size

taken? hit?

target address
Hybrid Branch Predictors

- **Idea:** Use more than one type of predictor (i.e., multiple algorithms) and select the “best” prediction
  - E.g., hybrid of 2-bit counters and global predictor

- **Advantages:**
  + Better accuracy: different predictors are better for different branches
  + Reduced *warmup* time (faster-warmup predictor used until the slower-warmup predictor warms up)

- **Disadvantages:**
  -- Need “meta-predictor” or “selector”
  -- Longer access latency

Alpha 21264 Tournament Predictor

- Minimum branch penalty: 7 cycles
- Typical branch penalty: 11+ cycles
- 48K bits of target addresses stored in I-cache
- Predictor tables are reset on a context switch

Branch Prediction Accuracy (Example)

- Bimodal: table of 2bc indexed by branch address

Figure 13: Combined Predictor Performance by Benchmark
Biased Branches

- Observation: Many branches are biased in one direction (e.g., 99% taken)

- Problem: These branches pollute the branch prediction structures → make the prediction of other branches difficult by causing “interference” in branch prediction tables and history registers

- Solution: Detect such biased branches, and predict them with a simpler predictor

Some Other Branch Predictor Types

- Loop branch detector and predictor
  - Works well for loops with small number of iterations, where iteration count is predictable

- Perceptron branch predictor
  - Learns the *direction correlations* between individual branches
  - Assigns weights to correlations

- Geometric history length predictor

- Your predictor?
How to Handle Control Dependences

- Critical to keep the pipeline full with correct sequence of dynamic instructions.

- Potential solutions if the instruction is a control-flow instruction:
  - **Stall** the pipeline until we know the next fetch address
  - Guess the next fetch address (**branch prediction**)
  - Employ delayed branching (**branch delay slot**)
  - Do something else (**fine-grained multithreading**)
  - Eliminate control-flow instructions (**predicated execution**)
  - Fetch from both possible paths (if you know the addresses of both possible paths) (**multipath execution**)
Review: Predicate Combining (not Predicated Execution)

- Complex predicates are converted into multiple branches
  - if ((a == b) && (c < d) && (a > 5000))  { ... }
    - 3 conditional branches

- Problem: This increases the number of control dependencies

- Idea: Combine predicate operations to feed a single branch instruction
  - Predicates stored and operated on using condition registers
  - A single branch checks the value of the combined predicate

  + Fewer branches in code → fewer mipredictions/stalls

  -- Possibly unnecessary work
    -- If the first predicate is false, no need to compute other predicates

- Condition registers exist in IBM RS6000 and the POWER architecture
Predication (Predicated Execution)

- **Idea:** Compiler converts control dependence into data dependence $\rightarrow$ branch is eliminated
  - Each instruction has a predicate bit set based on the predicate computation
  - Only instructions with TRUE predicates are committed (others turned into NOPs)

(normal branch code)  
```plaintext
if (cond) {
    b = 0;
} else {
    b = 1;
}
```

(predicated code)  
```plaintext
if (cond) {
    p1 = (cond);
    branch p1, TARGET
}
else {
    p1 = (!p1);
    mov b, 1
    jmp JOIN
}
TARGET:
mov b, 0
add x, b, 1
add x, b, 1
```
Conditional Move Operations

- Very limited form of predicated execution

- CMOV R1 ← R2
  - R1 = (ConditionCode == true) ? R2 : R1
  - Employed in most modern ISAs (x86, Alpha)
Review: CMOV Operation

- Suppose we had a Conditional Move instruction...
  - CMOV condition, R1 ← R2
  - R1 = (condition == true) ? R2 : R1
  - Employed in most modern ISAs (x86, Alpha)

- Code example with branches vs. CMOVs
  if (a == 5) {b = 4;} else {b = 3;}

CMPEQ condition, a, 5;
CMOV condition, b ← 4;
CMOV !condition, b ← 3;
Predicated execution can be high performance and energy-efficient.

Predicated Execution
Fetch Decode Rename Schedule RegisterRead Execute

Branch Prediction
Fetch Decode Rename Schedule RegisterRead Execute

Pipeline flush!!
Predicated Execution (III)

- **Advantages:**
  - Eliminates mispredictions for hard-to-predict branches
  - No need for branch prediction for some branches
  - Good if misprediction cost > useless work due to predication
  - Enables code optimizations hindered by the control dependency
  - Can move instructions more freely within predicated code

- **Disadvantages:**
  - Causes useless work for branches that are easy to predict
    - Reduces performance if misprediction cost < useless work
    - Adaptivity: Static predication is not adaptive to run-time branch behavior. Branch behavior changes based on input set, program phase, control-flow path.
  - Additional hardware and ISA support
  - Cannot eliminate all hard to predict branches
  - Loop branches
Predicated Execution in Intel Itanium

- Each instruction can be separately predicated
- 64 one-bit predicate registers
  - each instruction carries a 6-bit predicate field
- An instruction is effectively a NOP if its predicate is false

```
cmp
br
else1
else2
br
then1
then2
join1
join2
```
Conditional Execution in the ARM ISA

- Almost all ARM instructions can include an optional condition code.

- An instruction with a condition code is executed only if the condition code flags in the CPSR meet the specified condition.
### Conditional Execution in ARM ISA

<table>
<thead>
<tr>
<th>Cond</th>
<th>Opcode</th>
<th>S</th>
<th>Rn</th>
<th>Rd</th>
<th>Operand2</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>000</td>
<td>000000</td>
<td>A</td>
<td>S</td>
<td></td>
<td>Rn</td>
</tr>
<tr>
<td>000</td>
<td>000101</td>
<td>B</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>000000</td>
<td>I</td>
<td>W</td>
<td></td>
<td>Offset</td>
</tr>
<tr>
<td>100</td>
<td>000000</td>
<td>I</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>000</td>
<td>000100</td>
<td>B</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>000000</td>
<td>I</td>
<td></td>
<td></td>
<td>Offset</td>
</tr>
<tr>
<td>001</td>
<td>000100</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>000000</td>
<td>U</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>000000</td>
<td>O</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>000000</td>
<td>L</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Instruction type
- Data processing / PSR Transfer
- Multiply
- Long Multiply  (v3M / v4 only)
- Swap
- Load/Store Byte/Word
- Load/Store Multiple
- Halfword transfer: Immediate offset  (v4 only)
- Halfword transfer: Register offset  (v4 only)
- Branch
- Branch Exchange  (v4T only)
- Coprocessor data transfer
- Coprocessor data operation
- Coprocessor register transfer
- Software interrupt
Conditional Execution in ARM ISA

<table>
<thead>
<tr>
<th>Cond Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>EQ - Z set (equal)</td>
</tr>
<tr>
<td>0001</td>
<td>NE - Z clear (not equal)</td>
</tr>
<tr>
<td>0010</td>
<td>HS / CS - C set (unsigned higher or same)</td>
</tr>
<tr>
<td>0011</td>
<td>LO / CC - C clear (unsigned lower)</td>
</tr>
<tr>
<td>0100</td>
<td>MI - N set (negative)</td>
</tr>
<tr>
<td>0101</td>
<td>PL - N clear (positive or zero)</td>
</tr>
<tr>
<td>0110</td>
<td>VS - V set (overflow)</td>
</tr>
<tr>
<td>0111</td>
<td>VC - V clear (no overflow)</td>
</tr>
<tr>
<td>1000</td>
<td>HI - C set and Z clear (unsigned higher)</td>
</tr>
<tr>
<td>1001</td>
<td>LS - C clear or Z (set unsigned lower or same)</td>
</tr>
<tr>
<td>1010</td>
<td>GE - N set and V set, or N clear and V clear (&gt;=)</td>
</tr>
<tr>
<td>1011</td>
<td>LT - N set and V clear, or N clear and V set (&gt;</td>
</tr>
<tr>
<td>1100</td>
<td>GT - Z clear, and either N set and V set, or N clear and V set (&gt;</td>
</tr>
<tr>
<td>1101</td>
<td>LE - Z set, or N set and V clear, or N clear and V set (&lt; or =)</td>
</tr>
<tr>
<td>1110</td>
<td>AL - always</td>
</tr>
<tr>
<td>1111</td>
<td>NV - reserved</td>
</tr>
</tbody>
</table>

The ARM Instruction Set - ARM University Program - V1.0
Conditional Execution in ARM ISA

* To execute an instruction conditionally, simply postfix it with the appropriate condition:
  - For example an add instruction takes the form:
    - ADD r0,r1,r2 ; r0 = r1 + r2 (ADDLAL)
  - To execute this only if the zero flag is set:
    - ADDEQ r0,r1,r2 ; If zero flag set then...
      ; ... r0 = r1 + r2

* By default, data processing operations do not affect the condition flags (apart from the comparisons where this is the only effect). To cause the condition flags to be updated, the S bit of the instruction needs to be set by postfixing the instruction (and any condition code) with an “S”.
  - For example to add two numbers and set the condition flags:
    - ADDS r0,r1,r2 ; r0 = r1 + r2
      ; ... and set flags
Conditional Execution in ARM ISA

* Convert the GCD algorithm given in this flowchart into
  1) “Normal” assembler, where only branches can be conditional.
  2) ARM assembler, where all instructions are conditional, thus improving code density.

* The only instructions you need are CMP, B and SUB.
Conditional Execution in ARM ISA

“Normal” Assembler

```
gcd    cmp  r0, r1 ;reached the end?
    beq  stop
    blt  less ;if r0 > r1
    sub  r0, r0, r1 ;subtract r1 from r0
    bal  gcd

less  sub  r1, r1, r0 ;subtract r0 from r1
    bal  gcd

stop
```

ARM Conditional Assembler

```
gcd    cmp  r0, r1 ;if r0 > r1
    subgt r0, r0, r1 ;subtract r1 from r0
    sublt r1, r1, r0 ;else subtract r0 from r1
    bne  gcd ;reached the end?
```
Idealism

- Wouldn’t it be nice
  - If the branch is eliminated (predicated) only when it would actually be mispredicted
  - If the branch were predicted when it would actually be correctly predicted

- Wouldn’t it be nice
  - If predication did not require ISA support
Improving Predicated Execution

- Three major limitations of predication
  1. **Adaptivity**: non-adaptive to branch behavior
  2. **Complex CFG**: inapplicable to loops/complex control flow graphs
  3. **ISA**: Requires large ISA changes

- **Wish Branches** [Kim+, MICRO 2005]
  - Solve 1 and partially 2 (for loops)

- **Dynamic Predicated Execution**
  - **Diverge-Merge Processor** [Kim+, MICRO 2006]
    - Solves 1, 2 (partially), 3
Wish Branches

- The **compiler** generates code (with wish branches) that can be executed **either** as predicated code **or** non-predicated code (normal branch code)
- The **hardware decides** to execute predicated code or normal branch code at run-time based on the confidence of branch prediction
- **Easy to predict: normal branch code**
- **Hard to predict: predicated code**

Wish Jump/Join

A

T

N

C

D

B

p1 = (cond)
branch p1, TARGET

mov b, 1
jmp JOIN

TARGET:
mov b, 0

normal branch code

not-taken

A

B

C

D

A

p1 = (cond)

B

(!p1) mov b,1

C

(p1) mov b,0

predicated code

High Confidence

A

A

A

B

B

B

C

C

C

D

D

D

JOIN:
mov b,0

JOIN:
mov b,0

wish jump/join code

nop

wished join
Wish Branches vs. Predicated Execution

Advantages compared to predicated execution

- Reduces the overhead of predication
- Increases the benefits of predicated code by allowing the compiler to generate more **aggressively-predicated code**
- Makes predicated code less dependent on machine configuration (e.g. branch predictor)

Disadvantages compared to predicated execution

- Extra branch instructions use machine resources
- Extra branch instructions increase the contention for branch predictor table entries
- Constrains the compiler’s scope for **code optimizations**
How to Handle Control Dependences

- Critical to keep the pipeline full with correct sequence of dynamic instructions.

- Potential solutions if the instruction is a control-flow instruction:
  - **Stall** the pipeline until we know the next fetch address
  - Guess the next fetch address (**branch prediction**)
  - Employ delayed branching (**branch delay slot**)
  - Do something else (**fine-grained multithreading**)
  - Eliminate control-flow instructions (**predicated execution**)
  - Fetch from both possible paths (if you know the addresses of both possible paths) (**multipath execution**)
Multi-Path Execution

- **Idea:** Execute both paths after a conditional branch
  - For a hard-to-predict branch: Use dynamic confidence estimation

- **Advantages:**
  + Improves performance if misprediction cost > useless work
  + No ISA change needed

- **Disadvantages:**
  -- What happens when the machine encounters another hard-to-predict branch? Execute both paths again?
    -- Paths followed quickly become exponential
  -- Each followed path requires its own context (registers, PC, GHR)
  -- Wasted work (and reduced performance) if paths merge
Dual-Path Execution versus Predication

Hard to predict

Dual-path

Predicated Execution

Path 1

Path 2

Path 1

Path 2