

CMU 18-447 INTRODUCTION TO COMPUTER ARCHITECTURE, SPRING 2012
HANDOUT 5/ HW 3: MICROPROGRAMMING AND PIPELINING

Prof. Onur Mutlu, Instructor
Chris Fallin, Lavanya Subramanian, Abeer Agrawal, TAs

Given: Monday, Feb 13, 2012
Due: **Monday, Feb 27, 2012**

1 LC-3b Microcode

We wrote the microcode for the LDW instruction of the LC-3b in class. In this homework, you will complete the microcode for all states of the LC-3b.

Refer to Appendix C of Patt and Patel for the LC-3b state machine and datapath and Appendix A of Patt and Patel for the LC-3b ISA description.

Fill out the microcode in the microcode.csv file handed out with this homework. Enter a 1 or a 0 or an X as appropriate for the microinstructions corresponding to states. You do not need to fill out states 8, 10 and 11. We fill out state 18 as an example. Please turn in this CSV file electronically along with your homework.

2 Adding the REP MOVSB Instruction to the LC-3b

We wish to use the unused opcode **1010** to implement the x86 instruction REP MOVSB, (which you wrote MIPS assembly for in homework 1) in the LC-3b.

The specification of REP MOVSB for LC-3b that we want you to implement is as follows:

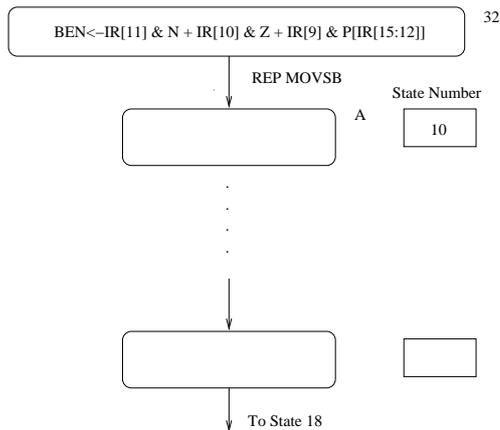
REPMOVSB SR1, SR2, DR

This is encoded as follows in LC-3b machine code:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1010				DR				SR1			0	0	0	SR2		

The REP MOVSB instruction uses three registers: SR1 (count), SR2 (source) and DR (destination). It moves a byte from memory at address SR2 to memory at address DR, and then increments both pointers by one. This is repeated SR1 times. Thus, the instruction copies SR1 bytes from address SR2 to address DR. Assume that the value in SR1 is greater than or equal to zero.

- (a) Complete the state diagram shown below, using the notation of the LC-3b state diagram. Describe inside each bubble what happens in each state and assign each state an appropriate state number. Add additional states not present in the original LC-3b design as you see fit.



- (b) Add to the LC-3b datapath any additional structures and any additional control signals needed to implement REP MOVSB. Clearly label your additional control signals with descriptive names. Describe what value each control signal would take to control the datapath in a particular way.
- (c) Describe any changes you need to make to the LC-3b microsequencer. Add any additional logic and control signals you need. Clearly describe the purpose and function of each signal and the values it would take to control the microsequencer in a particular way.
- (d) The processing in each state is controlled by asserting or negating each control signal. Enter a 1 or a 0 or an X as appropriate for the microinstructions corresponding to the new states you added, in the repmovsb.csv file handed out with this homework. Add all your additional control signals at the end of the control word.

3 Pipelining

Given the following code:

```
MUL R3, R1, R2
ADD R5, R4, R3
ADD R6, R4, R1
MUL R7, R8, R9
ADD R4, R3, R7
MUL R10, R5, R6
```

Note: Each instruction is specified with the destination register first.

Calculate the number of cycles it takes to execute the given code on the following models:

- (a) A non-pipelined machine
- (b) A pipelined machine with scoreboarding and five adders and five multipliers without data forwarding
- (c) A pipelined machine with scoreboarding and five adders and five multipliers with data forwarding.
- (d) A pipelined machine with scoreboarding and one adder and one multiplier without data forwarding

(e) A pipelined machine with scoreboarding and one adder and one multiplier with data forwarding

Note: For all machine models, use the basic instruction cycle as follows:

- Fetch (one clock cycle)
- Decode (one clock cycle)
- Execute (MUL takes 6, ADD takes 4 clock cycles). The multiplier and the adder are not pipelined.
- Write-back (one clock cycle)

Do not forget to list any assumptions you make about the pipeline structure (e.g., how is data forwarding done between pipeline stages).