CARNEGIE MELLON UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

18-322 DIGITAL INTEGRATED CIRCUITS FALL 2002

Final Examination, Monday Dec. 16, 2002

NAME: ____________________________  SECTION: ____________

Time: 180 minutes
Closed books, closed notes.

Good luck!

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<th>P1 (20pts.)</th>
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extra credit

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Problem 1 (20pts) The figure below shows the layout of a CMOS gate.

For this layout:

a) List all the layers, from the top to the bottom, at the drill points X, Y and Z. Include all the CVD oxides up to Metal 2.

   X:                                                   Y:                                                  Z:

   In1                                                  In2                                                  In1
b) Draw the cross-sections along the lines A-B and C-D. Place your solution in Figs. S1 and S2.

![Fig. S1: Cross-section A-B](image1)

![Fig. S2: Cross-section C-D](image2)
Problem 2 (15pts.) Extract the transistor-level circuit diagram from the layout shown above. Specify the Boolean function implemented in this layout.
Problem 3 (15pts.) Consider the CMOS circuit shown in Fig.1. (The W/L ratios for logic gates apply to both NMOS and PMOS transistors.) We want to determine the delay from input X to the output Z. Let us denote by \( \tau = R_n C_n \) the product of the effective on-resistance and gate capacitance of the minimum sized NMOS transistor, i.e. \((W/L)_n = 1/1\). For the minimum sized PMOS transistor, we have \(R_p = 2R_n\). Also, the load at output Z is \(C_L = 10C_n\).

![Fig.1](image-url)

Estimate lower and upper bounds for the rising and falling transitions at output Z in terms of \(\tau\).
Problem 4. (10pts.) A two stage buffer is used to drive a metal wire of length 1 cm. The width of the metal wire is 3.6 µm. The first inverter is a minimum size with an input capacitance $C_i = 10 \text{ fF}$ and a propagation delay $t_{p0} = 175\text{ps}$ when loaded with an identical gate. The sheet resistance of the metal is $0.08 \Omega/\text{sq.}$, the capacitance value is $0.03 \text{ fF}/\mu\text{m}^2$ and the fringing field capacitance is $0.04 \text{ fF}/\mu\text{m}$.

a) Assuming the lumped RC delay model, what is the propagation delay through the metal wire?

b) Compute the optimal size of the second inverter as to minimize the total delay. What is this minimum delay through the buffer (from the input of the first inverter to the end point of the metal wire)?
Problem 5. (20pts.) The circuit given in Fig.2 represents a modified dynamic circuit as an attempt to obtain high performance. Each block L1, L2, L3 is a pull-down (PDN) or pull-up (PUP) circuit as labelled.

Fig.2

a) Assuming that each block (L1, L2, and L3) implements an inverter, fill in the waveforms for nodes $\phi_2, \phi_3, \text{out}1, \text{out}2,$ and $\text{out}$ on the diagram below. Assume that each inverter in the clock chain has a fixed delay $\tau$, and so does each of the logic blocks. Also, the allowed logic values in the operation of this circuit are $\{0, 1, X\}$, where $X$ denotes a value between 0 and 1.
(This is a backup diagram.)

```plaintext
\tau

\text{phi1}:

\text{phi2}:

\text{phi3}:

A

\text{out1}:

\text{out2}:

\text{out}
```
b) Do you observe any particular problem with the power dissipation of this circuit? If yes, describe in detail the conditions that activate the problem and propose a minimal change to this circuit that will eliminate it.
Extra-credit (20pts): In the figure below, we give a more detailed schematic of block L2 in Fig.2. We are given that $C_L = 160\text{fF}$ and $C = 20\text{fF}$. Also, due to high temperature of the chip, it turns out that there is a net leakage current of $5\mu\text{A}$ flowing into node “out2” when it is low. Input B switches soon after the evaluation phase begins. Determine the maximum length of the evaluation period. Assume that $V_{DD} = 2.5\text{V}$ and $V_{Tn} = |V_{Tp}| = 0.4\text{V}$. 

\[ \text{Diagram} \]
Problem 6. (20pts.) Using the Elmore delay model, find the delays indicated in the following circuit. Approximate each transistor with a resistor and label the resistor with the corresponding transistor number (i.e. transistor M1 would be modeled with resistor R1, etc.). Also, ignore transistors capacitances since all the capacitive effects are captured in the capacitors explicitly shown in the figure.

Fig. 3

a) What is the boolean function Y in terms or inputs A, B, C, D?
b) Find the delay from A to Y when B = 1, C = 1, D = 1, and A switches from 0 to 1. (Show the simplified circuit you use to derive the delay.)

c) What is the dynamic power dissipation assuming that the condition in part b) happens every T seconds?
d) Find the delay from D to Y when A = 1, B = 1, C = 1, and D switches from 0 to 1. (Show the simplified circuit you use to derive the delay.)

e) What is the dynamic power dissipation assuming that the condition in part d) happens every T seconds?